

Customer Code: _____

DATASHEET

DAPU P/N: DPA3250M0000EH0GSA0

DAPU			Customer Approval
Drew	Audited	Approved	
Jieshu ZHENG	Jianhua LIN	Gangtao FENG	
Date:	2024/11/6		

Stamp, please! Thanks!

Guangdong Dapu Telecom Technology Co.,Ltd

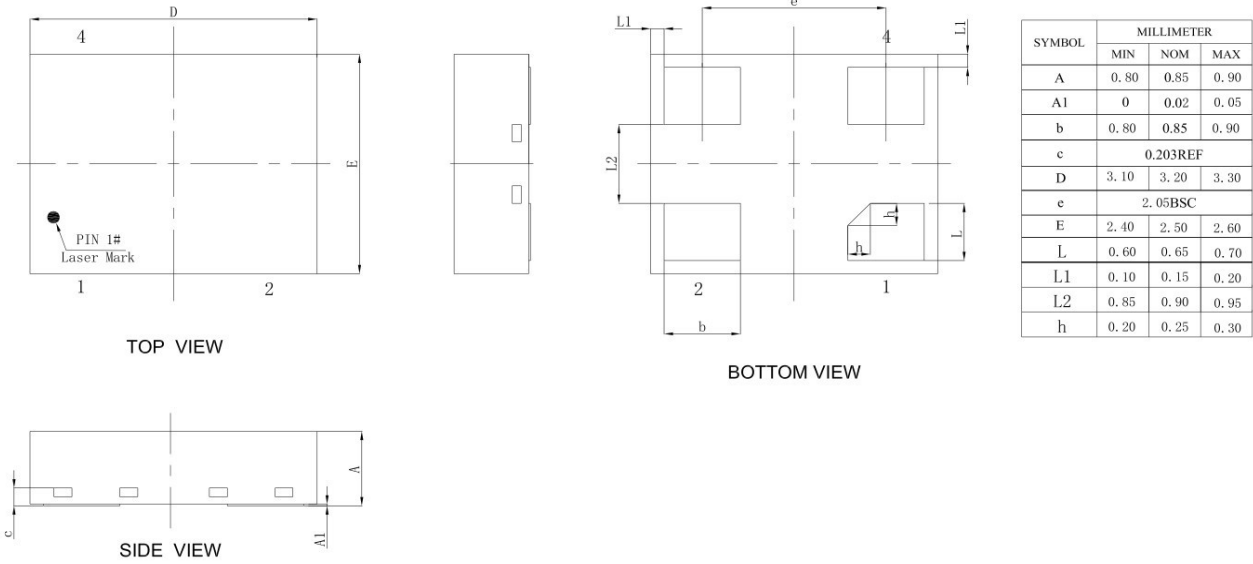
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1、Electrical Parameter

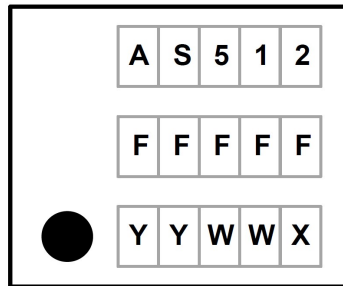
MODEL :		DPA3250M0000EH0GSA0					
No.	Parameters	SYM.	Electrical Spec.				Notes
			Min.	Typ.	Max.	Units	
1	Nominal Frequency	F _L	50.0000			MHz	
2	Frequency Tolerance	F _T	-15		15	ppm	Inclusive of initial frequency tolerance at 25°C, 10-year aging at 25°C, and variations over supply voltage, load and humidity after soldering-reflow shift settles.
3	Frequency Stability	-	-35		35	ppm	-40°C~85°C (Reference 25°C)
4	Operating Temperature	T _{opr}	-40		85	°C	
5	Storage Temperature	T _{stg}	-55		105	°C	
6	Supply Voltage	V _{DD}	1.71		3.63	V	
7	Input Current	I _{cc}		40	55	mA	CMOS (C _L =15 pF)
8	Output Waveform	-	CMOS			-	
9	Output Load	C _L	15			pF	
10	Output Voltage High	V _{OH}	0.83×V _{DD}			V	I _{OH} = 8/6/4 mA for 3.3/2.5/1.8V V _{DD}
11	Output Voltage Low	V _{OL}			0.17×V _{DD}	V	I _{OL} = 8/6/4 mA for 3.3/2.5/1.8V V _{DD}
12	Rise Time	T _r		0.5	1.5	ns	20% to 80% V _{pp}
13	Fall Time	T _f		0.5	1.5	ns	
14	Input Voltage High	V _{IH}	0.7×V _{DD}			V	Frequency select (FS includes a 50 kΩ pull-up to V _{DD} and a 50 kΩ pull-down to GND.)
15	Input Voltage Low	V _{IL}			0.3×V _{DD}	V	
16	Duty Cycle	DC	45~55			%	
17	Powerup Time	T _{OSC}			4	ms	Time from 0.9×V _{DD} until output frequency (F _{CLK}) within spec
18	Phase Jitter (RMS)	Φ _J		350		fs	12kHz - 20MHz
19	Solder Temperature	T _{PEAK}	260			°C	The device is compliant with JEDEC J-STD-020.
	Solder Time at T _{PEAK}	T _P	20~40			sec	
20	Moisture Sensitivity Level 2						

2、 Mechanical Structure

2.1 Dimensions

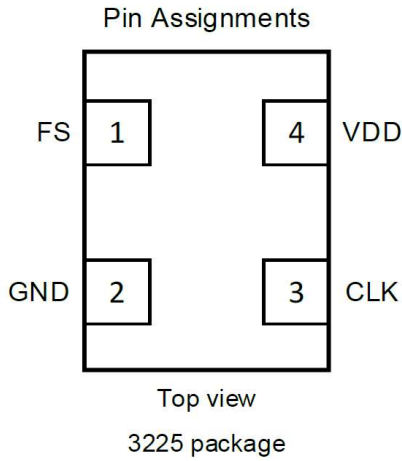


2.2 Marking



Line	Position	Description
1	1-5	Device Name
2	1-5	Unique 5-digit Device Configuration Number
3	Position 1	Pin 1 orientation mark (dot)
	Position 2-3	Year (last two digits of the year), to be assigned by assembly site
	Position 4-5	Calendar Work Week number (1-53), to be assigned by assembly site
	Position 6	Assembly site code

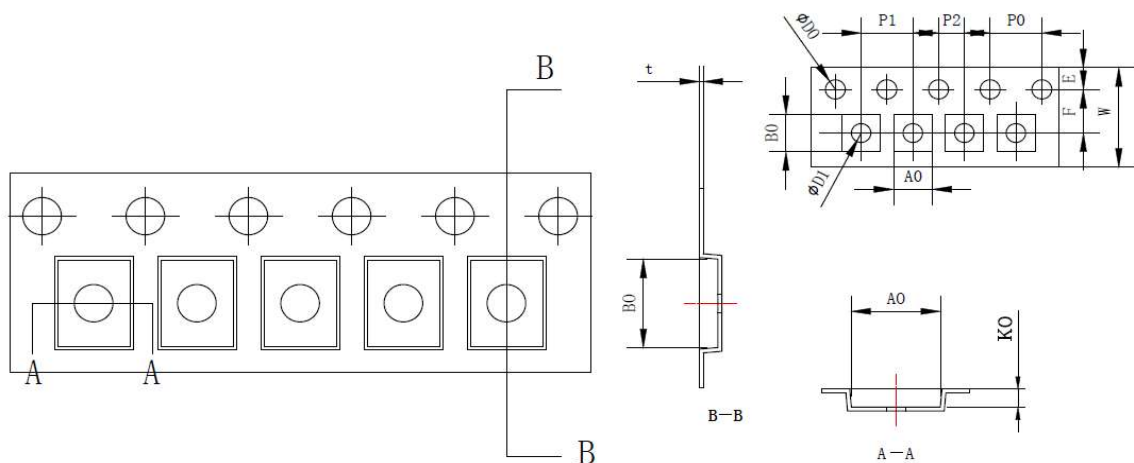
3、 Pin description



Pin#	Name	Description
1	FS	Configuration selector
2	GND	Ground
3	CLK	CMOS clock output
4	VDD	Power supply

FS	Description
Low	Driver stopped, output forced to high impedance
High	CLK output active, center spreading enabled: +/-0.5% Spread profile: Hershey-kiss Modulation frequency: 25 kHz

4、 Package: Tape & Reel (mm)



W	E	F	D0	D1	P0	P2	10P0	P1	A0	A1	B0	B1	KO	K1	t
8.00 ±0.30	1.75 ±0.10	3.50 ±0.05	1.50 +0.10	1.00 +0.10	4.00 ±0.10	2.00 ±0.10	40.00 ±0.20	4.00 ±0.10	2.80 ±0.10	/	3.60 ±0.10	/	1.10 ±0.10	/	0.30 ±0.05