



To Customer: _____

Realtime Clock Module

INS5T8130

Datasheet

Document Version 1.0

Released on September 20, 2023

Ordering Information

| Manufacture Part Number | Product Name | Description |
|-------------------------|--------------|--|
| INS5T8130-5DFX000Y00CA | INS5T8130 | <120ppm @ -20°C~+70°C <5±23ppm @ 25°C |
| | | |
| | | |

Guangdong Dapu Telecom Technology Co., Ltd

Bldg 5, SSL Modern Enterprise Accelerator Zone, Dongguan City, Guangdong Province, PRC China

[TEL:0086-0769-88010888](tel:0086-0769-88010888)

FAX:0086-0769-81800098

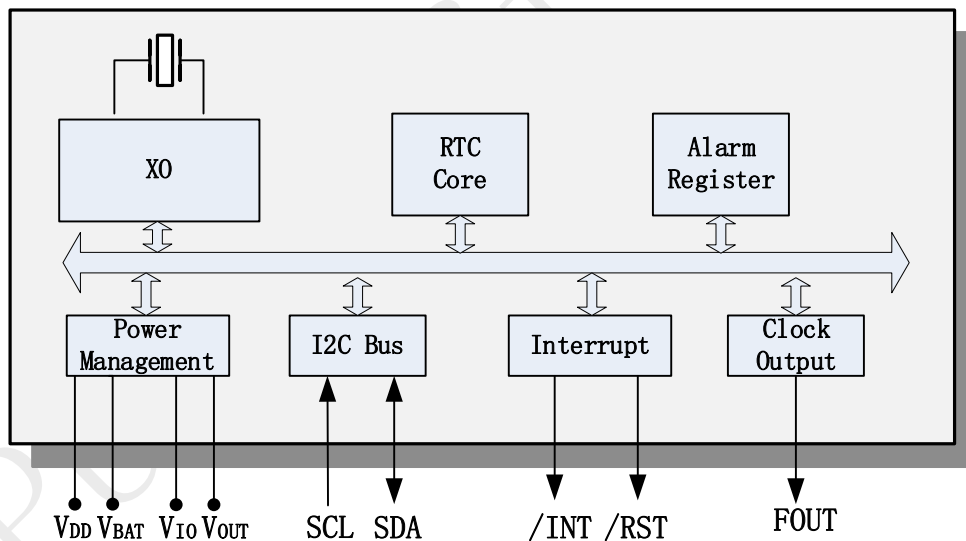


INS5T8130 —Low Power Consumption I²C RTC

Key Features

- Low current consumption: 0.9uA (Typ.)
- High stability:
< 5±23ppm @ +25°C
- Build-in XO: 32.768KHz
- Communication interface: I²C bus
- Power supply voltage: 1.6V~5.5V
- Timekeeper voltage: 1.2V~5.5V
- Operation temperature range: -40°C ~ +85°C
- Leap years autocorrection
- Timer output function with adjustable period
- Package: 3.2mm × 2.5mm × 1.0mm
- Digital offset function

Block Diagram



Overview

INS5T8130 is an I²C bus interface real-time clock with low power consumption and digital offset function. It supports backup battery and embeds a 32.768KHz XO. It supports calendar (year, month, day, hour, minute, second), clock and timer functions etc. The SMD3225 package with only 1.0mm thickness makes it very suitable to be used in portable and small size electronic devices.



Revision History

| Version | Change Contents | Prepared by | Revised Date |
|---------|-----------------|-------------|--------------|
| V1.0 | First Issued | | 2023.09.20 |
| | | | |



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1 Pin definition

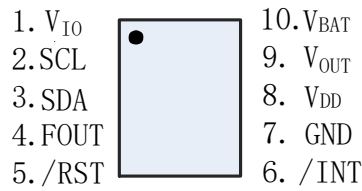


Table1. Pin Definition

| Pin Number | Pin Name | I/O | Description |
|------------|------------------|--------|---|
| 1 | V _{IO} | - | Interface power supply pin. |
| 2 | SCL | In | I ² C clock signal |
| 3 | SDA | In/Out | I ² C data signal |
| 4 | FOUT | Out | Frequency output. Frequency can be set by FSEL bits. |
| 5 | /RST | Out | Reset signal output. After the VDD pressure drop is detected, the pin outputs a negative pulse. |
| 6 | /INT | Out | Timing event interrupt output. Open-Drain. |
| 7 | GND | - | Ground |
| 8 | V _{DD} | - | Power supply |
| 9 | V _{OUT} | - | Internal voltage output pin. Connect capacitor of 1.0uF to Ground |
| 10 | V _{BAT} | - | Backup battery pin. VBAT cannot floating, connect to large-capacity capacitors or a backup battery. Connect to V _{DD} when switchover function is not necessary. |

Note: A 0.1μF bypass capacitor is needed at least between power supply pins and GND pin.

Note: Input pins regardless of V_{IO} applied voltage. It is able to input up to 5.5V.

Note: Open drain pins regardless of V_{IO} applied voltage. It is able to Pull-up to 5.5V

Note: When not use, take the FOUT, /RST, /INT terminals as OPEN



2 Electrical Characteristics

2.1 Absolute Maximum Ratings

Table2. Absolute Maximum Ratings

| Parameter | Symbol | Value | | | Unit | Notes |
|------------------------|-------------------|---------|------|----------------------|------|------------------|
| | | Min. | Typ. | Max. | | |
| Power supply voltage | V _{DD} | -0.3 | | 6.5 | V | |
| Internal voltage | V _{OUT} | -0.3 | | 6.5 | V | |
| Backup battery voltage | V _{BAT} | -0.3 | | 6.5 | V | |
| Interface voltage | V _{IO} | -0.3 | | 6.5 | V | |
| Input voltage | V _{IN} | GND-0.3 | | 6.5 | V | SCL, SDA input |
| Clock output voltage | V _{OUT1} | GND-0.3 | | V _{DD} +0.3 | V | FOUT output |
| Output voltage | V _{OUT2} | GND-0.3 | | 6.5 | V | SDA, /INT output |
| Storage temperature | T _{STG} | -55 | | 125 | °C | |

2.2 Recommended Operating Conditions

Table3. Recommended Operating Conditions

Unless otherwise specified, GND=0V, Ta=-40°C~+85°C

| Parameter | Symbol | Value | | | Unit | Notes |
|---------------------------------------|------------------|-------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Power Supply Voltage (normal mode) | V _{DD} | 1.2 | 3.0 | 5.5 | V | |
| Interface voltage | V _{IO} | 1.6 | 3.0 | 5.5 | V | If INIEN = 1, V _{DD} <V _{DET1} , the interface is disable. |
| Backup Battery | V _{BAT} | 1.2 | 3.0 | 5.5 | V | |
| Operation temperature | T _{OPR} | -40 | 25 | 85 | °C | |

Note 1: To apply Min. value of V_{DD}, V_{DD} need to be supplied with more than 2.5V at least for the oscillation to stabilize (oscillation start time t_{STA}). Please ensure that force the power to V_{DD} rather than V_{BAT} when first power on.

Note 2: Ensure that the power on time from 0 to V_{DD} is less than 100ms



2.3 Frequency Characteristics

Table4. Frequency Characteristics

Unless otherwise specified, GND=0V, Ta=-40°C~+85°C

| Parameter | Symbol | Value | | | Unit | Notes |
|------------------------|------------------|-------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Frequency stability | $\Delta f_1/f$ | 5±23 | | | ppm | V _{DD} =3.0V; @+25°C |
| Frequency stability | $\Delta f_2/f$ | -120 | | +10 | ppm | V _{DD} =3.0V; -20°C ~ +70°C; Reference frequency @ +25°C |
| Oscillation start time | t _{STA} | | | 1 | s | V _{DD} =2.5V~5.5V |
| Year Aging | f _a | | | ±5 | ppm | |
| FOUT duty cycle | t _{w/t} | 40 | 50 | 60 | % | |

2.4 DC Characteristics

Table5. DC Characteristics

Unless otherwise specified, GND=0V, V_{BAT}=V_{DD}=1.2~5.5V, V_{IO}=1.6V ~5.5V, Ta=-40°C~+85°C

| Item | Symbol | Value | | | Unit | Notes |
|---|------------------|-------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Average Current consumption1 | I _{DD1} | | 0.9 | 5.6 | uA | SCL=SDA = 'H', FOUT=OFF, /INT=OFF, V _{DD} =V _{IO} =3.0V,CHGEN=0b or V _{BAT} ≧ VDET3, -40°C~85°C |
| Average Current consumption 2 | I _{DD2} | | 3.4 | 7.8 | uA | SCL=SDA = 'H', FOUT=32.768kHz (FOUT pin CL=15pF), /INT=OFF,V _{DD} =V _{IO} =3.0V, CHGEN=0b or V _{BAT} ≧ VDET3,- 40°C~85°C |
| Average Current consumption 3 | I _{DD3} | | 1.0 | 5.0 | uA | SCL, SDA = 'L', V _{BAT} =3.0V, V _{DD} =V _{IO} =0V, - 40°C~+85°C |
| Detector Threshold voltage1 (V _{DD} rising edge) | +VDET11 | 2.25 | 2.6 | 2.95 | V | /RST releases setting:2.6 V |
| Detector Threshold voltage1 (V _{DD} falling edge) | -VDET11 | 2.20 | 2.55 | 2.90 | V | /RST output setting:2.6 V |
| Detector Threshold voltage2 (V _{DD} rising edge) | +VDET12 | 2.20 | 2.55 | 2.90 | V | /RST releases setting:2.55V |



| Item | Symbol | Value | | | Unit | Notes |
|--|---------|-------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Detector Threshold voltage2 (V _{DD} falling edge) | -VDET12 | 2.15 | 2.5 | 2.85 | V | /RST output setting:2.55 V |
| Detector Threshold voltage3 (V _{DD} rising edge) | +VDET2 | 1.22 | 1.46 | 1.7 | V | Exchange voltage: VBAT to VDD |
| Detector Threshold voltage3 (V _{DD} falling edge) | -VDET2 | 1.2 | 1.44 | 1.68 | V | Exchange voltage: VDD to VBAT |
| Detector Threshold voltage4 (V _{BAT} rising edge) | +VDET31 | 2.77 | 2.97 | 3.17 | V | Stop charging voltage (full charge) BFVSEL=00b |
| Detector Threshold voltage4 (V _{BAT} falling edge) | -VDET31 | 2.68 | 2.90 | 3.12 | V | Recharge voltage. BFVSEL=00b |
| Detector Threshold voltage5 (V _{BAT} rising edge) | +VDET30 | 2.7 | 2.88 | 3.1 | V | Stop charging voltage (full charge) BFVSEL=10b |
| Detector Threshold voltage5 (V _{BAT} falling edge) | -VDET30 | 2.65 | 2.8 | 3.00 | V | Recharge voltage. BFVSEL=10b |
| Detector Threshold voltage6 (V _{BAT} rising edge) | +VDET32 | 2.82 | 3.05 | 3.28 | V | Stop charging voltage (full charge) BFVSEL=01b |
| Detector Threshold voltage6 (V _{BAT} falling edge) | -VDET32 | 2.72 | 2.95 | 3.2 | V | Recharge voltage. BFVSEL=01b |
| V _{BAT} off voltage | -VDET4 | 2.1 | 2.3 | 2.6 | V | Low V _{BAT} detection VBLF = 1b |
| V _{DD} -V _{OUT} Off-leak current | Isw1 | | | 15 | nA | V _{DD} =0V, V _{OUT} =3.0V |
| V _{DD} -V _{OUT} Off-leak current | Isw2 | | | 15 | nA | V _{OUT} =0V, V _{BAT} =3.0V |



| Item | Symbol | Value | | | Unit | Notes |
|----------------------------------|-------------------|----------------------|-------------------------|---------------------|------|---|
| | | Min. | Typ. | Max. | | |
| V _{OUT} output voltage1 | V _{OUT1} | | V _{DD} -0.06V | | V | V _{DD} =3V, I _{OUT} =1mA |
| V _{OUT} output voltage2 | V _{OUT2} | | V _{BAT} -0.02V | | V | V _{BAT} =3.0V, I _{OUT} =0.1mA |
| Input voltage High-level | V _{IH} | 0.8*V _{IO} | | 5.5 | V | SCL, SDA |
| Input voltage Low-level | V _{IL} | GND-0.3 | | 0.2*V _{IO} | V | |
| Output voltage High-level | V _{OH} | V _{IO} -0.5 | | V _{IO} | V | I _{OH} = -1mA FOUT 脚 |
| Output voltage Low-level | V _{OL1} | GND | | GND+0.5 | V | I _{OL} = 1mA FOUT 脚 |
| | V _{OL2} | GND | | GND+0.25 | V | V _{IO} =5.0V, I _{OL} =1mA /RST, |
| | V _{OL3} | GND | | GND+0.4 | V | V _{IO} =3.0V, I _{OL} =1mA /INT |
| | V _{OL4} | GND | | GND+0.4 | V | V _{IO} ≥2.0V, I _{OL} =3mA SDA |

2.5 AC Characteristics

Table6. AC Characteristics

Unless otherwise specified, GND =0V, V_{IO}=1.6V ~ 5.5V; Ta=-40°C ~ +85°C

| Parameter | Symbol | Value | | | Unit |
|--|---------------------|-------|------|------|------|
| | | Min. | Typ. | Max. | |
| SCL clock frequency | f _{SCL} | | | 400 | kHz |
| SCL low level time | t _{LOW} | 1.3 | | | us |
| SCL high level time | t _{HIGH} | 0.6 | | | us |
| Start condition setup time | t _{HD;STA} | 0.6 | | | us |
| Start condition hold time | t _{SU;STA} | 0.6 | | | us |
| Stop condition setup time | t _{SU;STO} | 0.6 | | | us |
| Bus idle time between start condition and stop condition | t _{RCV} | 1.3 | | | us |
| Data setup time | t _{SU;DAT} | 100 | | | ns |
| Data hold time | t _{HD;DAT} | 0 | | | ns |
| SCL, SDA rising time | t _r | | | 0.3 | us |
| SCL, SDA falling time | t _f | | | 0.3 | us |

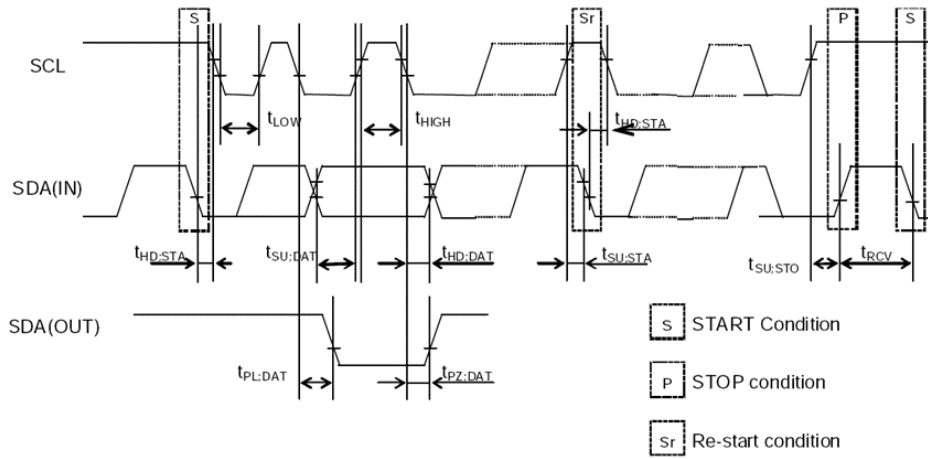


Figure 1. I²C bus Timing Chart



3 Registers

3.1 Register Lists

Address 0x10~0x19: Basic Time and Calendar Registers

Address 0x1A~0x1F: Control、Flags、Extended Register sets

Address 0x20~0x23: RAM register bank

Address 0x30~0x31: Extended register bank 1

Table7. Basic Time and Calendar Registers

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | R/W |
|---------|--------------------|--------------------------------|----------------------------------|--------------------------------|---------------------------------|----------------------------------|---------|---------|---------|-----|
| 0x10 | SEC | ○ | BCD code, Second tens place, 0-5 | | | BCD code, Second ones place, 0-9 | | | | R/W |
| 0x11 | MIN | ○ | BCD code, Minute tens place, 0-5 | | | BCD code, Minute ones place, 0-9 | | | | R/W |
| 0x12 | HOUR | ○ | ○ | BCD code, Hour tens place, 0-2 | | BCD code, Hour ones place, 0-9 | | | | R/W |
| 0x13 | WEEK | ○ | 6 | 5 | 4 | 3 | 2 | 1 | 0 | R/W |
| 0x14 | DAY | ○ | ○ | BCD code, Day tens place, 0-3 | | BCD code, Day ones place, 0-9 | | | | R/W |
| 0x15 | MONTH | ○ | ○ | ○ | BCD code, Month tens place, 0-1 | BCD code, Month ones place, 0-9 | | | | R/W |
| 0x16 | YEAR | BCD code, Year tens place, 0-9 | | | | BCD code, Year ones place, 0-9 | | | | R/W |
| 0x17 | MIN Alarm | AE | BCD code, Minute tens place, 0-5 | | | BCD code, Minute ones place, 0-9 | | | | R |
| 0x18 | HOUR Alarm | AE | ● | BCD code, Hour tens place, 0-2 | | BCD code, Hour ones place, 0-9 | | | | R/W |
| 0x19 | WEEK Alarm | AE | 6 | 5 | 4 | 3 | 2 | 1 | 0 | R/W |
| | DAY Alarm | | ● | BCD code, Day tens place, 0-3 | | BCD code, Day ones place, 0-9 | | | | R/W |
| 0x1A | Timer Counter 0 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | R/W |
| 0x1B | Timer Counter 1 | 32768 | 16384 | 8192 | 4096 | 2048 | 1024 | 512 | 256 | R/W |
| 0x1C | Extension Register | FSEL[1] | FSEL[0] | USEL | TE | WADA | TSEL[2] | TSEL[1] | TSEL[0] | R/W |
| 0x1D | Flag Register | VBLF | ○ | UF | TF | AF | RSF | VLF | VBFF | R/W |
| 0x1E | Control Register | TEST | STOP | UIE | TIE | AIE | TSTP | TBKON | TBKE | R/W |



| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | R/W |
|-------------------|---------------------|-------------|-------------|-------|-------|------|--------|------------|------------|-----|
| 0x1F | Control Register | SMP TSEL[1] | SMP TSEL[0] | CHGEN | INIEN | ○ | RSVSEL | BF VSEL[1] | BF VSEL[0] | R/W |
| 0x20 0x23 | RAM | ● | ● | ● | ● | ● | ● | ● | ● | R/W |
| 0x30 | Digital offset | DTE | L7 | L6 | L5 | L4 | L3 | L2 | L1 | R/W |
| 0x31 | Extension Register1 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | VBLFE | R/W |

Note:

1. After power-up reset or in case VLF bit returns “1”, make sure to initialize all registers to default state before using the RTC.
2. During the initial power-up, below bits will be in the state as below:
 Initial 0: TEST、WADA、USEL、TE、FSEL[1:0]、TSEL[1:0]、UF、TF、AF、UIE、TIE、AIE、TSTP、TBKON、TBKE、DTE、VBLF、VBFF、SMPTSEL[1:0]、CHGEN、INIEN、RSVSEL、BFVSEL[1:0]、VBLFE;
 Initial 1: VLF、RSF、TSEL[2];
3. All other register values are undefined, so make sure to reset the module before using it.
4. The bits marked with “○” can be read out “0” only after initializing.
5. The bits marked with “●” are RAM bits which can be used to write or read any data.
6. Only 0 can be written to UF, TF, AF, VLF bits.
7. Make sure “0” to be written for TEST bits which are used for testing only.

3.2 Details of Registers

3.2.1 Clock counter registers

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|----------------------------------|--------------------------------|------|----------------------------------|------|------|------|---------|
| 0x10 | SEC | ○ | BCD code, Second tens place, 0-5 | | | BCD code, Second ones place, 0-9 | | | | 0x00 |
| 0x11 | MIN | ○ | BCD code, Minute tens place, 0-5 | | | BCD code, Minute ones place, 0-9 | | | | 0x00 |
| 0x12 | HOUR | ○ | ○ | BCD code, Hour tens place, 0-2 | | BCD code, Hour ones place, 0-9 | | | | 0x00 |

SEC: BCD format, Value: 0~59

MIN: BCD format, Value: 0~59

HOUR: BCD format, Value: 0~23

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|------|------|------|------|------|------|---------|
| 0x13 | WEEK | ○ | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x40 |

WEEK: Value 01h, 02h, 04h, 08h, 10h, 20h, 40h. Only one bit can be set to 1 each time, all others must be set to 0.



Table8. WEEK Register

| WEEK | Data | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|-----------|------|------|------|------|------|------|------|------|------|
| Sunday | 01h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Monday | 02h | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Tuesday | 04h | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Wednesday | 08h | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| Thursday | 10h | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Friday | 20h | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| Saturday | 40h | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

Only one bit can be set to 1 each time.

Table9. Daily registers

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|-------------------------------|------|-------------------------------|------|------|------|---------|
| 0x14 | DAY | ○ | ○ | BCD code, Day tens place, 0-3 | | BCD code, Day ones place, 0-9 | | | | 0x01 |

DAY: BCD format, the value range will be adjusted automatically according to the month setting and if a leap year or not.

Table10. DAY Register Value

| Month | Day Value Range |
|-------------------------|-----------------|
| 1, 3, 5, 7, 8, 10, 12 | 1~31 |
| 4, 6, 9, 11 | 1~30 |
| February in normal year | 1~28 |
| February in leap year | 1~29 |

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|--------------------------------|------|------|---------------------------------|---------------------------------|------|------|------|---------|
| 0x15 | MONTH | ○ | ○ | ○ | BCD code, Month tens place, 0-1 | BCD code, Month ones place, 0-9 | | | | 0x01 |
| 0x16 | YEAR | BCD code, Year tens place, 0-9 | | | | BCD code, Year ones place, 0-9 | | | | 0x00 |

MONTH: BCD format, Value1~12

YEAR: BCD format, Value0~99(2000~2099)

Example: 2020/01/01 Wednesday 21:18:36

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------|----------|------|------|------|------|------|------|------|------|
| 0x10 | SEC | ○ | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0x11 | MIN | ○ | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0x12 | HOUR | ○ | ○ | 1 | 0 | 0 | 0 | 0 | 1 |
| 0x13 | WEEK | ○ | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0x14 | DAY | ○ | ○ | 0 | 0 | 0 | 0 | 0 | 1 |
| 0x15 | MONTH | ○ | ○ | ○ | 0 | 0 | 0 | 0 | 1 |
| 0x16 | YEAR | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |



3.2.2 Alarm registers

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|------------|------|----------------------------------|--------------------------------|------|----------------------------------|------|------|------|---------|
| 0x17 | MIN Alarm | AE | BCD code, Minute tens place, 0-5 | | | BCD code, Minute ones place, 0-9 | | | | 0x00 |
| 0x18 | HOUR Alarm | AE | ● | BCD code, Hour tens place, 0-2 | | BCD code, Minute ones place, 0-9 | | | | 0x00 |
| 0x19 | WEEK Alarm | AE | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x00 |
| | DAY Alarm | | ● | BCD code, Day tens place, 0-3 | | BCD code, Day ones place, 0-9 | | | | |

1. Set specific day, week, hour, minute value, cooperate with AIE, AF, WADA, generate alarm interrupt;
2. WEEK Alarm/DAY Alarm: WADA bit control 0x0A is set for daily or weekly Alarm. For details, see 0x1C register bit3;
3. AE (Alarm Enable): Alarm control, 0- Enable. 1 - Disable;
4. AF function bit see 0x1D register bit3;
5. AIE function bit see register 0x1E bit3 for details;

3.2.3 Timer registers

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|-----------------|-------|-------|------|------|------|------|------|------|---------|
| 0x1A | Timer Counter 0 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 0x00 |
| 0x1B | Timer Counter 1 | 32768 | 16384 | 8192 | 4096 | 2048 | 1024 | 512 | 256 | 0x00 |

1. Set a specific timer value, count down to 0, cooperate with TE, TF, TIE, TSEL[2:0], generate alarm interrupt;
2. TE function bit see 0x1C register bit4;
3. TF function bit see 0x1D register bit4;
4. TIE function bit see 0x1E register bit4;
5. TSEL[2:0] function bits see 0x1C register bit2, bit1, bit0 bits;

3.2.4 Extension registers

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|--------------------|----------|----------|------|------|------|----------|----------|----------|---------|
| 0x1C | Extension Register | FSEL [1] | FSEL [0] | USEL | TE | WADA | TSEL [2] | TSEL [1] | TSEL [0] | 0x04 |

1. Alarm function, time update interrupt, Settings, etc. used to specify a specific target;
2. WADA (Week Alarm/Day Alarm) : 0-WEEK Alarm, 1-DAY Alarm;
3. USEL (Update Interrupt Select) : 0-interrupts per second (default), 1-interrupts per minute;
4. TE (Timer Enable) : 0- Disables the Timer interrupt function. 1- enables the Timer interrupt function

FSEL[1], FSEL[0]: FOUT frequency setting:



| FSEL[1] | FSEL[0] | FOUT Frequency |
|---------|---------|---------------------|
| 0 | 0 | 32.768KHz (Default) |
| 0 | 1 | 1024Hz |
| 1 | 0 | 1Hz |
| 1 | 1 | off |

When STOP is to set to 1, the output is 32768Hz and 1024Hz, but not 1Hz.

TSEL[2], TSEL[1], TSEL[0] : timer count clock selection, as shown in the following table:

| TSEL[2] | TSEL[1] | TSEL[0] | Timer clock | Interrupt pulse duration |
|---------|---------|---------|-------------------|--------------------------|
| 0 | 0 | 0 | 4096Hz (244.14us) | 122uS |
| 0 | 0 | 1 | 64Hz (15.625ms) | 7.57mS |
| 0 | 1 | 0 | 1Hz (1 second) | 7.57mS |
| 0 | 1 | 1 | 1/60Hz (1 minute) | 7.57mS |
| 1 | 0 | 0 | 1/3600Hz (1 hour) | 7.57mS |

3.2.5 Flag registers

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|---------------|------|------|------|------|------|------|------|------|---------|
| 0x1D | Flag Register | VBLF | ○ | UF | TF | AF | RSF | VLF | VBFF | 0x06 |

UF (Update Flag): Time update flag bit that changes from "0" to "1" when a time update interrupt event occurs and remains "1" until software writes "0";

TF (Timer Flag): Timer flag bit that changes from "0" to "1" when a fixed periodic interrupt occurs and remains "1" until software writes "0".

AF (Alarm Flag): Alarm flag bit that changes from "0" to "1" when an alarm interrupt occurs and remains "1" until the software writes "0".

VLF (Voltage Low Flag): Voltage low signal, when the voltage is lower than -vdet2, set "1" and keep "1" until software write "0".

VBFF (VBAT Full Charged Flag): Rechargeable battery charging flag. "0" means charging, "1" means charging completed, updated every second.

VBLF (VBAT Low Flag): Battery low voltage indicator. Set "1" when voltage is lower than VDET4 and keep "1" until software writes "0";

RSF (Reset Flag): Reset flag. Set '1' when voltage is below -vdet1 and keep "1" until software writes "0";

Table11. RSF Settings

| RSF | Description | Note |
|-----|--|-----------------|
| 0 | Clear 0 | Write operation |
| 1 | Disallow operations (write 1 is ignored) | |
| 0 | - | Read operation |
| 1 | V _{BAT} lower than -V _{DET} detected | |



Table12. VBLF Settings

| VBLF | Describe | Note |
|------|--|-----------------|
| 0 | Clear 0 | Write operation |
| 1 | Disallow operations (write 1 is ignored) | |
| 0 | - | Read operation |
| 1 | Voltage below V _{DET4} detected | |

3.2.6 Control registers

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|--------------------|-------------|-------------|-------|-------|------|--------|------------|------------|---------|
| 0x1E | Control Register 0 | TEST | STOP | UIE | TIE | AIE | TSTP | TBKON | TBKE | 0x00 |
| 0x1F | Control Register 1 | SMPTSEL [1] | SMPTSEL [0] | CHGEN | INIEN | ○ | RSVSEL | BFVSEL [1] | BFVSEL [0] | 0x00 |

TEST: The manufacturer test bit must be 0 and cannot be modified by users;

UIE: Update Interrupt Enable bit. When UF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).

TIE: Timer Interrupt Enable bit: When TF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).

AIE: Alarm Interrupt Enable bit: When AF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low);

TSTP (Timer Stop): This bit is used to Stop the countdown of a Timer with a fixed period. It is usually used with STOP, TE, and TBKE bits;

CHGEN (Charge Enable): Charge control switch of the standby battery. CHGEN is used for non-rechargeable batteries. The default value is 0. CHGEN position "1" for rechargeable batteries.

INIEN: Control bit of FOUT and IO, when VDD<-VDET1. INIEN=0, FOUT and IO are unavailable. INIEN=1, VDD<-VDET1, FOUT and IO are available;

Table13. INIEN Settings

| INIEN | Describe | Note |
|-------|--|------|
| 0 | 1. I2C and FOUT functions are available; | |
| 1 | 1. When VDD < VDET1, I2C and FOUT functions are unavailable; 2. When VDD is greater than VDET1, I2C and FOUT functions are available; | |

STOP: used to STOP the timing operation. When "STOP=1", all timing updates and calendar operations STOP; Fixed period timer interrupt function partially stops; 32768Hz and 1024Hz can be output, but 1Hz output is disabled;

Table14. Fixed-period timer stop control (TSTP setting)

| TE | STOP | TBKE | TSTP | Note |
|----|------|------|------|---|
| 1 | 0 | 0 | 0 | TSTP writing “0” will restart the timer |



| TE | STOP | TBKE | TSTP | Note |
|----|------|------|------|---|
| | | | | countdown. |
| | | | 1 | TSTP writes “1” to stop the timer |
| | | 1 | x | The TSTP value setting is invalid and the count does not stop even if set in TSTP= “1”. |
| | 1 | x | x | The timer stops when it is set to 64Hz, 1Hz, 1/60Hz or 1/3600Hz. |
| 0 | x | x | x | no counting |

TBKON (Timer Backup On)、TBKE (Timer Backup Enable): which is used to select the working time of the main power supply or the backup power supply. The count value is added.

Table15. Fixed-period timer normal mode/backup mode control

| TBKE | TBKON | Note |
|------|-------|---|
| 1 | 0 | This setting counts it at time of VDD supply mode |
| | 1 | This setting counts it at time of VBAT supply mode |
| 0 | x | This setting counts on VDD supply mode and VBAT supply mode |

SMPTSEL [1:0] (Sampling Time Select), for determining voltage detection period.

Table16. VDET3, VDET4 intermittent detection period

| SMPTSEL [1:0] | VDD work (Battery charging) | VDD work (Battery charging completed) | VDD work (Return from backup mode, VDET1>VDD>VDET2) | Note |
|---------------|-----------------------------|---------------------------------------|---|----------------|
| 00 | 2ms | 2ms | 2ms | The default 00 |
| 01 | 16ms | 16ms | 2ms | |
| 10 | 128ms | 128ms | 2ms | |
| 11 | 256ms | 256ms | 2ms | |

RSVSEL (Reset Voltage Select): Sets VDD pin Voltage detection level. VDET1 voltage level setting. If VDD drops below this level, output /RST signal and stop I/F and FOUT output depending on INIEN bit Settings;

Table17. RSVSEL Settings

| RSVSEL | Describe | Note |
|--------|----------|---------------------|
| 0 | 2.6V | -V _{DET11} |
| 1 | 2.55V | -V _{DET12} |

BFVSEL [1:0]: Setting the full charge detection threshold voltage to stop charging of the backup battery.



Table18. BFVSEL Settings

| BFVSEL [1] | BFVSEL [0] | Describe |
|------------|------------|--------------------------|
| 0 | 0 | +VDET31 |
| 0 | 1 | +VDET32 |
| 1 | 0 | +VDET30 |
| 1 | 1 | Off (unlimited charging) |

3.2.7 Digital offset register

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------------|------|------|------|------|------|------|------|------|---------|
| 0x30 | Digital offset | DTE | L7 | L6 | L5 | L4 | L3 | L2 | L1 | 0x00 |

DTE (Digital offset function Enable): Enables the digital offset adjustment function. If DET is “1”, digital offset adjustment is enabled. DET is “0” to turn off digital offset adjustment; After the digital offset function is enabled, the digital offset register adjusts the sub-second clock according to the value set in the digital offset register. The calibration of the "seconds" register takes place every 10 seconds and the amount of offset set determines the intensity of the calibration. This feature does not affect the 32.768 kHz signal output on the FOUT pin because it does not change the oscillation frequency of the built-in crystal. In the case of 1Hz or 1024Hz signal output on FOUT, the offset correction will cause some jitter on the clock signal. The alarm function and wake timer function (if a source clock less than 4096 Hz is selected) are affected by this function. The following table shows the corresponding offset value from L7 to L1. When L7 bit is “0”, the offset value is positive (the clock runs faster) and when L7 bit is “1” the offset value is negative (the clock runs slower):

Table19. Digital offset registers

| L7 | L6 | L5 | L4 | L3 | L2 | L1 | Offset Value (ppm) |
|-----|-------|----|----|----|----|----|--------------------|
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | +192.26 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | +189.21 |
| ... | | | | | | | ... |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | +6.1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | +3.05 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | ±0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | -3.05 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | -6.1 |
| ... | | | | | | | ... |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | -192.26 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | -195.31 |

Digital offset calculation method is as follows.

When the offset value is positive, $L [7:1] = [\text{Offset Value}] / 3.05$, decimals are discarded.

When the offset value is negative, $L [7:1] = 128 - [\text{Offset Value}] / 3.05$, decimals are discarded.



3.2.8 Extended register 1

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|---------------------|------|------|------|------|------|------|------|-------|---------|
| 0x31 | Extension Register1 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | VBLFE | 0x00 |

VBLFE (VBAT Low Flag Enable) : enables the battery Low voltage detection function;

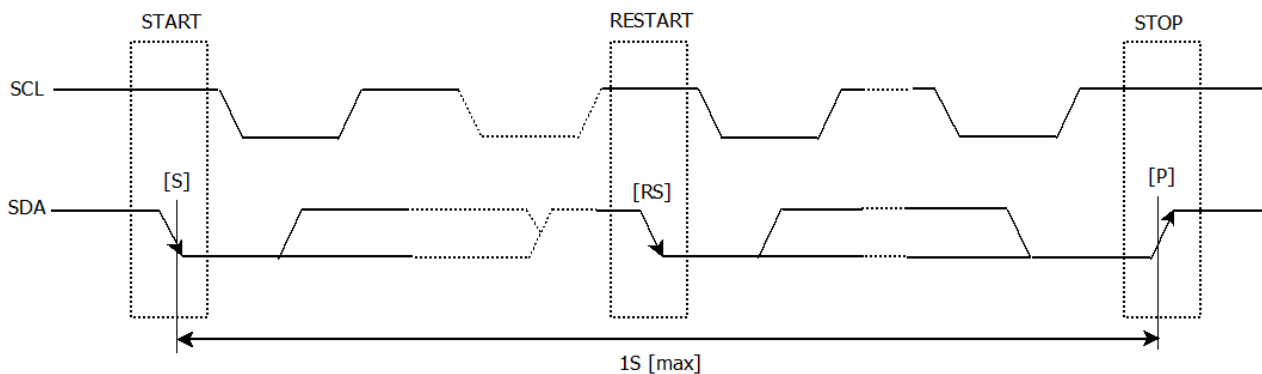
Table20. VBLFE Settings

| Operation | VBLFE | Describe |
|-----------|-------|--|
| Write | 0 | CHGEN:0 VBLF detection not enable CHGEN:1 VBLF detection enable (during normal mode re-chargeable battery charging) |
| | 1 | VBLF detection enable during VDD supply |

If you want to use VBLF detection, the INIEN should be set to 1 in addition to VBLFE bit setting. In VDD drive mode VBAT low voltage (non-rechargeable, rechargeable battery) can be detected. VBLF function is not available in case of backup mode.



4 I²C Bus Interface



I²C bus supports bi-directional communications through a serial clock line SCL and a serial data line SDA. I²C bus device can be defined as “Master” and “Slave”. INS5T8130 can only be used as Slave.

4.1 Cautions

I²C bus includes START, RESTART, STOP conditions, the duration between START and STOP must be less than 1 second just in case the bus to be set to standby mode automatically. A new START condition must be transferred before restarting of any communications.

INS5T8130 I²C bus interface supports single byte read/write operations as well as multiple bytes incremental access. After 0xFF address, the next one will be 0x00.

4.2 Slave Address

Table21. I²C Bus Slave Address

| Transfer data | Slave address | | | | | | | R/W |
|---------------|---------------|------|------|------|------|------|------|-----------|
| | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| 65h (Read) | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 (Read) |
| 64h (Write) | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 (Write) |

INS5T8130 I²C bus Slave Address is [0110 010*].

4.3 I²C bus protocol

It is assumed CPU is master and INS5T8130 is slave in this section.

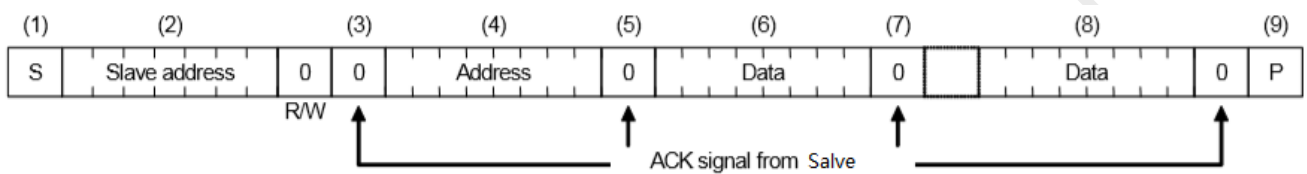
4.3.1 Write process

I²C bus includes an address auto-increment function, once the initial address has been specified, the



INS5T8130 increments (+1) the address automatically after each data is sent, then to write next data.

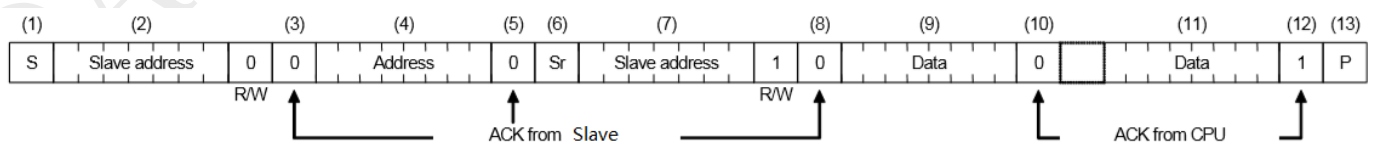
- (1) CPU sends start condition[S]
- (2) CPU sends INS5T8130's slave address with R/W bit to set to write mode
- (3) CPU verifies ACK signal from INS5T8130
- (4) CPU sends write address to INS5T8130
- (5) CPU verifies ACK signal from INS5T8130
- (6) CPU sends write data to the address specified at step (4)
- (7) CPU verifies ACK signal from INS5T8130
- (8) Repeat (6) (7) if multiple bytes need to be written, address will be incremented automatically
- (9) CPU ends stop condition[P]



4.3.2 Read process

Writing the address to be read with write mode firstly, then reading the data with read mode.

- (1) CPU sends start condition[S]
- (2) CPU sends INS5T8130's slave address with R/W bit to set to write mode
- (3) CPU verifies ACK signal from INS5T8130
- (4) CPU sends address for reading from INS5T8130
- (5) CPU verifies ACK signal from INS5T8130
- (6) CPU sends RESTART condition [Sr]
- (7) CPU sends INS5T8130's slave address with R/W bit to set to read mode
- (8) CPU verifies ACK signal from INS5T8130
- (9) CPU reads data from the specified address in step (4)
- (10) CPU sends ACK signal for "0"
- (11) Repeat (9) (10) if multiple bytes need to be read, address will be incremented automatically
- (12) CPU sends ACK signal for "1"
- (13) CPU sends stop condition[P]





5 Reflow Soldering Curve

Standard: IPC/JEDEC J-STD-020

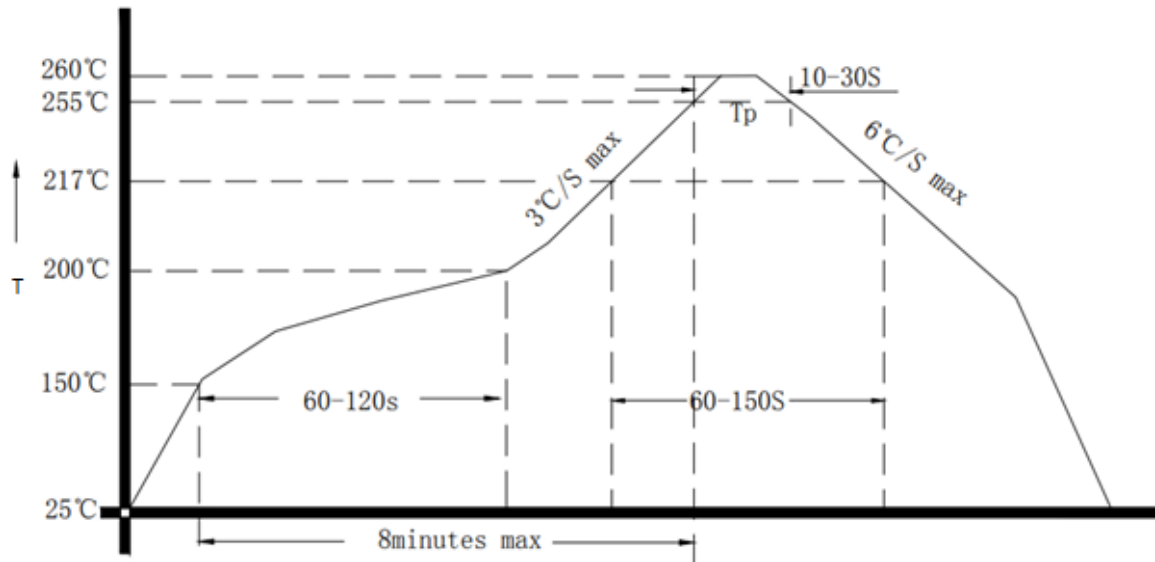


Figure 2. Reflow Soldering Curve

Note: It is suggested to solder IC under the condition shown in the curve above. Must pay attention to the temperature and time when manual soldering, if the temperature over +260°C, or you will make the xo performance bad, even damage it.



6 Dimensions

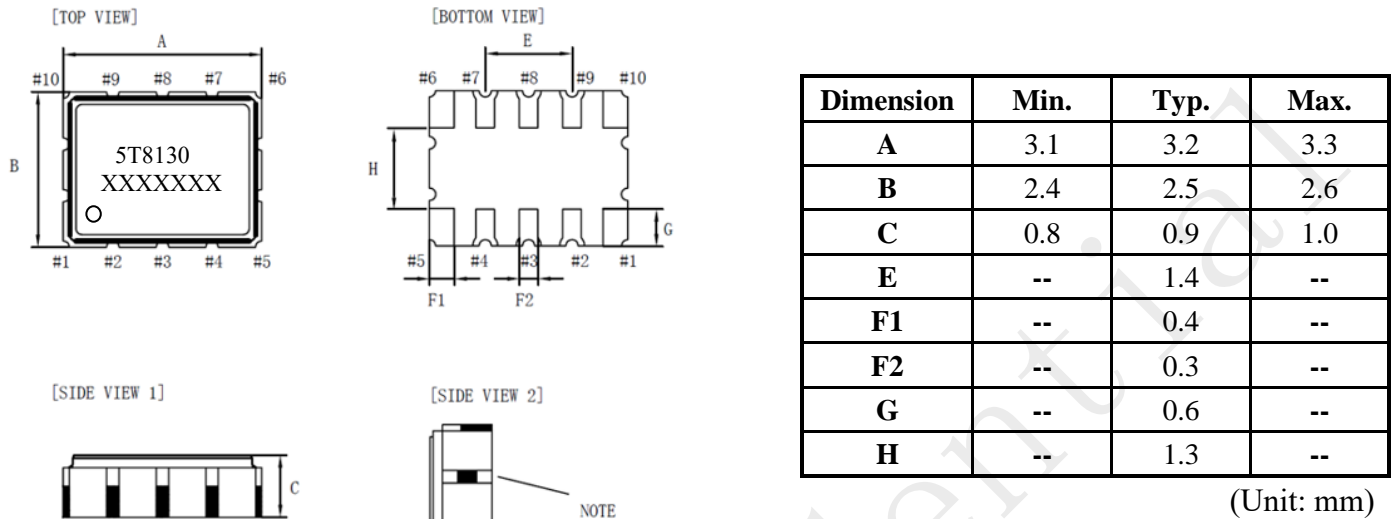
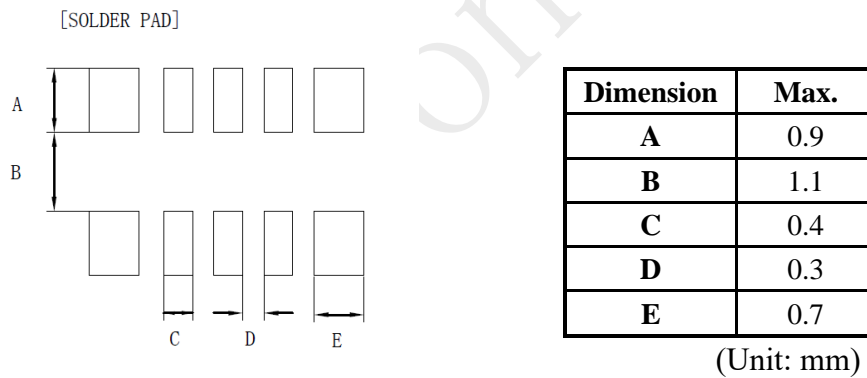


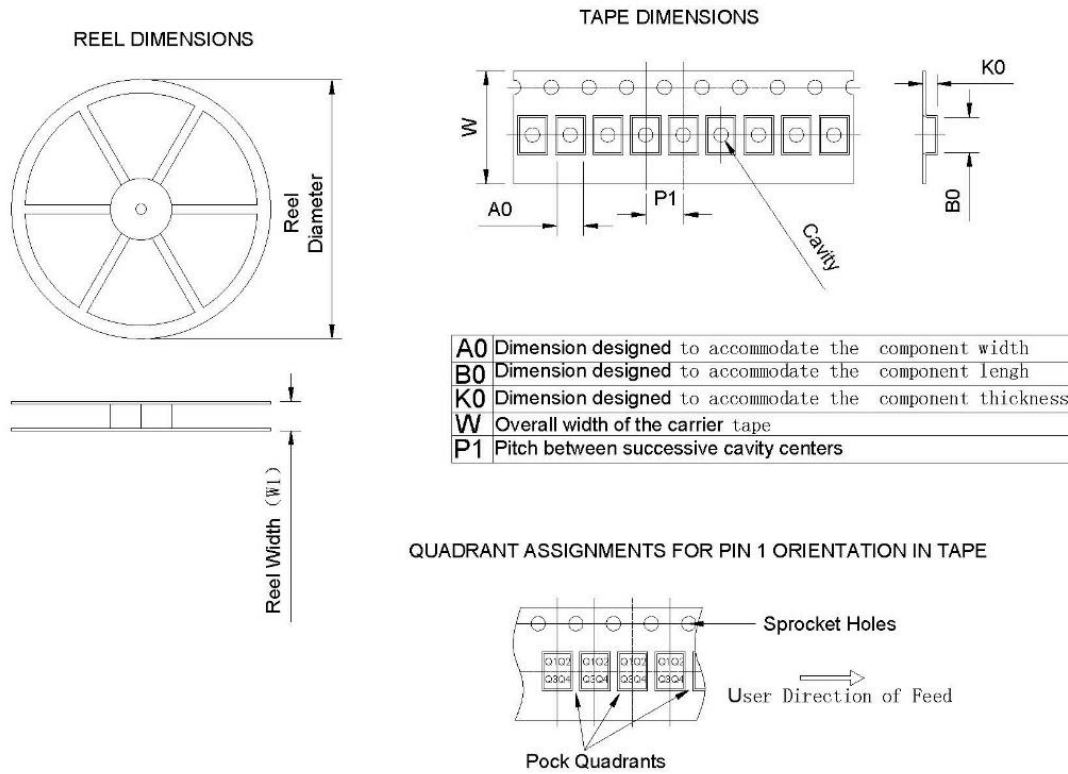
Figure 1. Dimension



Recommended Soldering Pattern



7 Package



| Device | Package Type | Pins | SPQ | Reel Diameter (mm) | Reel Width W1(mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | PIN1 Quadrant |
|-----------|--------------|------|------|--------------------|-------------------|---------|---------|---------|---------|--------|---------------|
| INS5T8130 | LGA | 10 | 3000 | 180 | 11.6±2.0 | 3.00 | 3.70 | 1.50 | 4.00 | 8.00 | Q1 |

Figure 2. Package