

Customer Code: \_\_\_\_\_

# DATASHEET

DAPU P/N: DPZ7548M000033B0

DAPU			Customer Approval
Drew	Audited	Approved	Stamp, please! Thanks!
Jack	David	William	
Date: 2022.04.19			

## Guangdong Dapu Telecom Technology Co.,Ltd

Building 5, No.24, Industrial East Road, Songshanhu Park, Dongguan, Guangdong, P.R. China

TEL: 0086-0769-88010888 FAX: 0086-0769-81800098

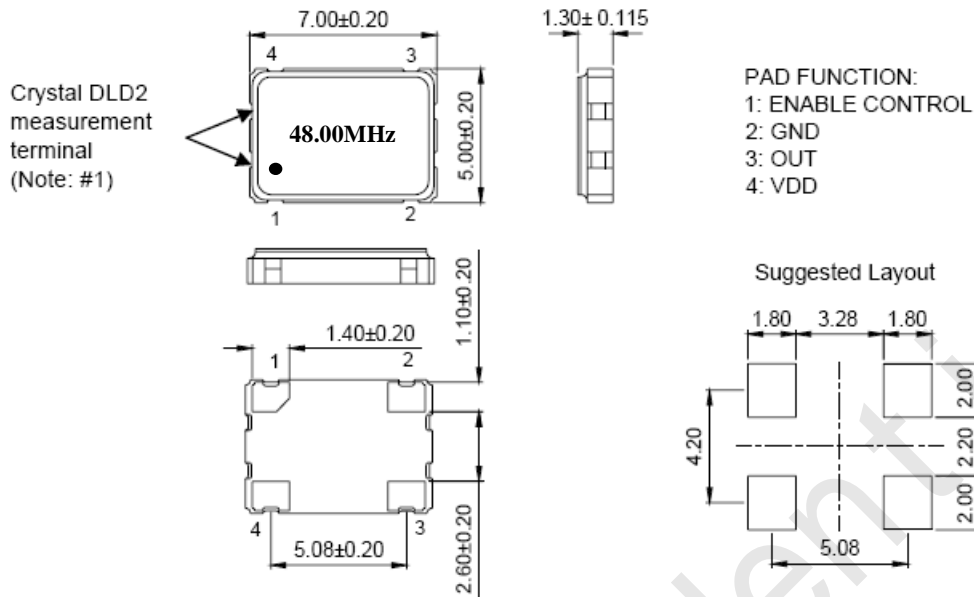


## 1、 Electrical Parameters

MODEL: DPZ7548M000033B0							
No.	Parameters	SYM.	Electrical Spec.				Notes
			Min.	Typ.	Max.	Units	
1	Nominal Frequency	FL	48.00			MHz	
2	Frequency Stability(Overall)	-	-50		+ 50	$\times 10^{-6}$	Includes frequency tolerance@25°C and frequency stability VS.operating temperature range and voltage variance and load change and first year aging.
3	Operating Temperature	Topr	-40	~	+ 85	°C	
4	Storage Temperature	Tstg	-55	~	+ 125	°C	
5	Supply Voltage	V <sub>DD</sub>	2.97	3.3	3.63	V	
6	Input Current	I <sub>cc</sub>			15	mA	
7	Output waveform	-	CMOS				
8	Output Load	CL	15			pF	
9	Output Voltage High	V <sub>OH</sub>	90%			V <sub>DD</sub>	
10	Output Voltage Low	V <sub>OL</sub>			10%	V <sub>DD</sub>	
11	Rise/Fall Time	Tr、 Tf			4	ns	20%-80% V <sub>DD</sub> Level
12	Aging	-	-3		+ 3	$\times 10^{-6}$	First Year at 25°C
13	Tri-State Output Enable	-	70%			V <sub>DD</sub>	Pin 1, OE
14	Tri-State Output Disable	-			30%	V <sub>DD</sub>	Pin 1, OE
15	Duty Cycle	-	45	~	55	%	
16	Start-Up Time	Tstart			10	ms	Measured from the time V <sub>DD</sub> reaches its rated minimum value



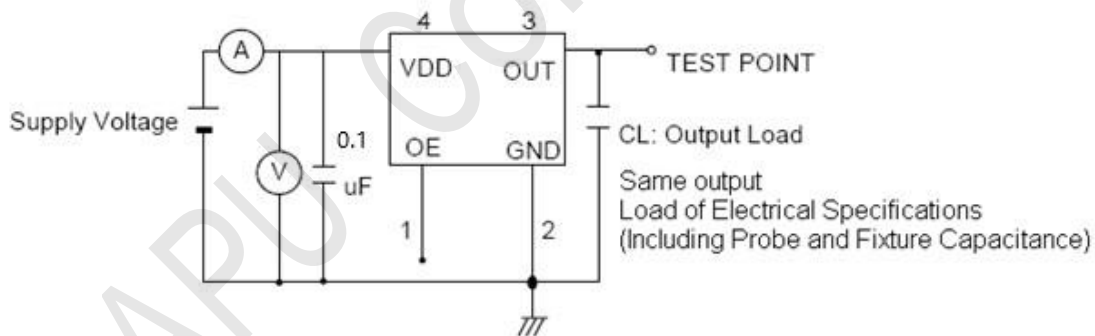
## 2、Mechanical Structure(mm)



Note: #1. DLD2 / Drive Level Dependency 2 Maximum resistance minus minimum resistance.

**Note1:**Tolerance  $\pm 0.2\text{mm}$  without mark

## 3、Test Circuit



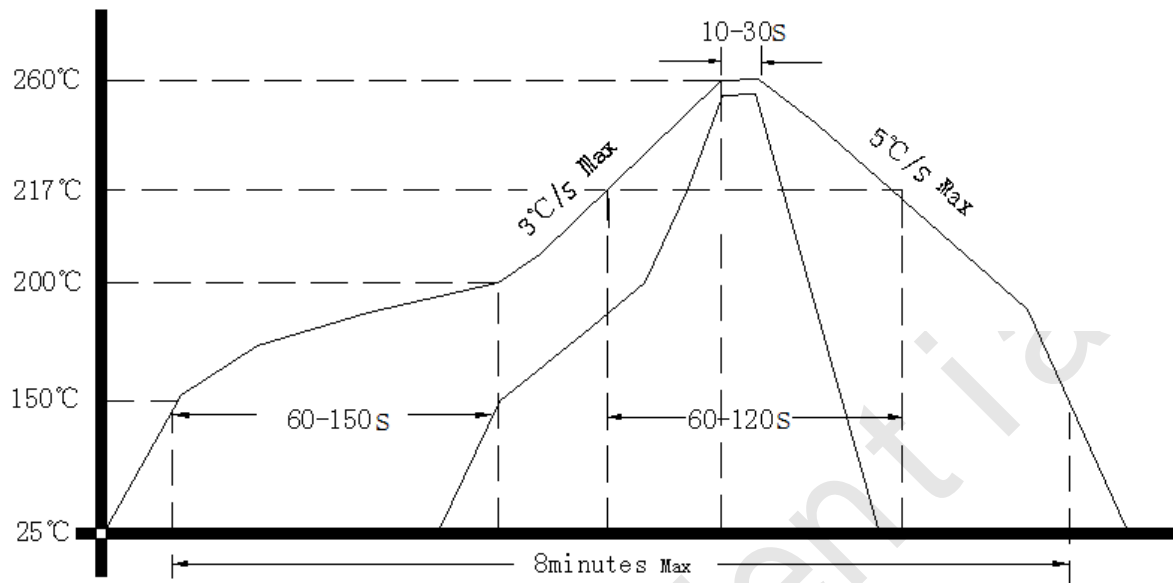
Control input (output enable/disable)

Logic 1 or open on pad 1: Oscillator output

Logic 0 on pad 1 : Disable output to high impedance



#### 4、 Reflow Soldering Curve (RoHS)



#### 5、 Package: Tape & Reel (mm)

