Guangdong Dapu Telecom Technology Co., Ltd

http://www.dptel.com

Bldg. 5, SSL Modern Enterprise Accelerator Zone, Dongguan City, Guangdong Province, PRC China
TEL:0086-0769-88010 888
FAX:0086-0769-81800098

INS5101A(A) —Low Power Consumption I²C RTC

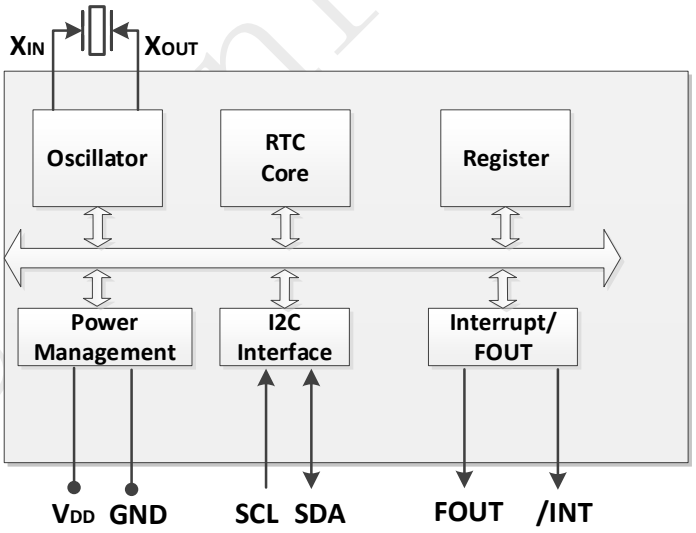
Key Features

- Low Current Consumption: 0.8uA (Typ.)
- Timer, Alarm and Interrupt
- Frequency Output
- Communication Interface: I²C bus
- Build-in 128bit RAM
- Integrated Oscillator Capacitors:6pF/12.5pF
- Power Supply Voltage: 1.2V~5.5V
- Operation Temperature Range: -40℃ ~ +85℃
- Leap Years Autocorrection
- Package: 4.9mm × 6.0mm × 1.6mm (SOP8)

Ordering Information

Part Number	Integrated Oscillator Capacitors	Package
INS5710A	12.5pF	SOP8
INS5710AA	6pF	SOP8

Block Diagram



Overview

INS5101A(A) is an I²C bus interface real-time clock with low power consumption. It supports calendar (year, month, day, hour, minute, second), timer and alarm function. The SOP8 package makes it suitable to be used in portable electronic devices.

Revision History

Version	Change Contents	Prepared by	Revised Date
V1.0	Released Version		2021.11.30
V1.1	Parameter update		2022.07.07
V1.2	Add INS5101AA (6pf)		2022.08.01

Index

1 Overview

INS5101A(A) is an I²C bus interface real-time clock with low power consumption. It supports calendar (year, month, day, hour, minute, second), timer and alarm function. The SOP8 package makes it suitable to be used in portable electronic devices.

2 Block Diagram

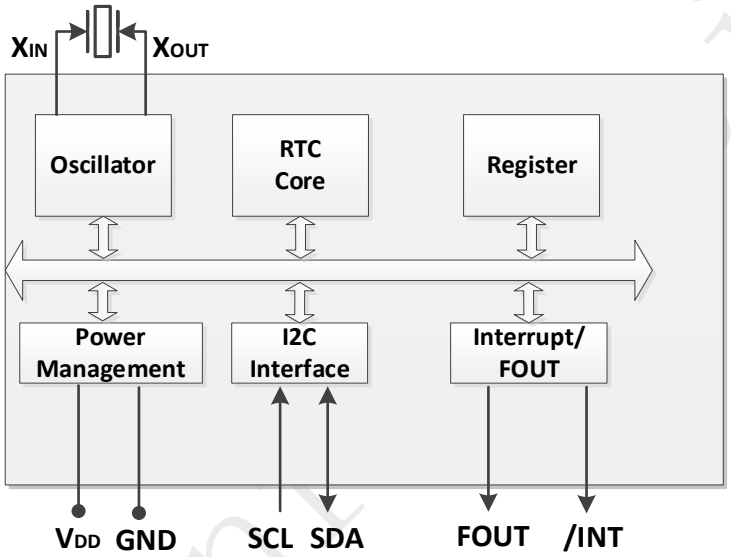


Figure 1. Block Diagram

3 Features

- Low Current Consumption: 0.8 uA (Typ.)
- Communication Interface: I²C bus
- Alarm, Timer and Interruption
- Frequency Out
- Build-in 128bit RAM
- Integrated Oscillator
  Capacitors:6pF/12.5pF
- Power Supply Voltage: 1.2V ~ 5.5V
- Leap Years Autocorrection
- Operation Temperature Range: -40℃ ~ +85℃
- Package: 4.9 * 6.0 * 1.6mm (SOP8)

4 Pin Definition

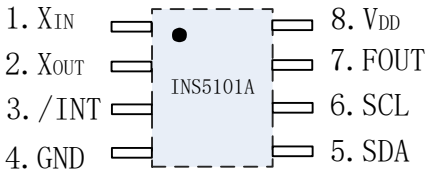


Table1. Pin Definition

Pin Number	Pin Name	I/O	Description
1	X_{IN}		Oscillator Input
2	X_{OUT}		Oscillator Output
3	/INT	Out	This pin can be configured as output of Alarm、Timer. Time-update Interrupt or Frequency, effective when Low Voltage (Open-Drain)
4	GND	-	Ground
5	SDA	In/Out	I2C data signal
6	SCL	In	I2C clock signal
7	FOUT	Out	This pin can be configured as the output of timer or frequency, effective when Low Voltage (CMOS)
8	V_{DD}	-	Power in

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table2. Absolute Maximum Ratings

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage	V_{DD}	-0.3		6.5	V	
I/O Input Voltage	V_{IN}	GND-0.3		6.5	V	SCL, SDA Input
Clock Output Voltage1	V_{OUT1}	GND-0.3		V_{DD}+0.3	V	FOUT
Clock Output Voltage2	V_{OUT2}	GND-0.3		6.5	V	SDA，/INT Output
Storage Temperature	T_{STG}	-55		125	℃	

5.2 Recommended Operating Conditions

Table3. Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage (normal mode)	V_{DD}	1.6	3.0	5.5	V	*
Power Supply Voltage (Time keeping)	V_{DD}	1.2	3.0	5.5	V	*
Operation Temperature	T_{OPR}	-40	25	85	℃	

Note 1: V_{DD} need to be supplied with more than 1.6V at least for the oscillator to work until stabilization.

Note 2: Ensure that the power on time from 0 to VDD is less than 100ms

5.3 Oscillator Characteristics

Table4. Oscillator Characteristics

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Oscillator						
Integrated Capacitance	C		12.5		pF	INS5101A
			6		pF	INS5101AA
External Crystal(32.768KHz)						
Series Resistance	R_S			100	kΩ	
Load Capacitance	C_L		12.5		pF	INS5101A
			6		pF	INS5101AA
FOUT Duty cycle	t_w/t	40	50	60	%	FOUT

5.4 DC Characteristics

Table5. DC Characteristics

Parameter	Symbol	Value			Unit	Notes	
		Min.	Typ.	Max.			
Average Current1	I_{DD1}		1.0	3.0	uA	V_{DD}=5.0V	Input pins are "L" f_{SCL} = 0 Hz, /INT = OFF, FOUT = OFF
Average Current2	I_{DD2}		0.8	2.8		V_{DD}=3.0V	
Average Current3	I_{DD3}		4.0	6.5		V_{DD}=5.0V	FOUT = 32.768KHz (CL=15PF), /INT=OFF
Average Current4	I_{DD4}		3.5	6.0		V_{DD}=3.0V	
Input High Voltage	V_{IH}	0.8*V_{DD}		5.5	V	SCL， SDA	
Input Low Voltage	V_{IL}	GND-0.3		0.2*V_{DD}	V		
Output High Voltage	V_{OH1}	4.5		5.0	V	VDD=5V, IOH=-1mA	FOUT
	V_{OH2}	2.7		3.0		VDD=3V, IOH=-0.5mA	
Output Low Voltage	V_{OL1}	GND		GND+0.25	V	VDD =5V, IOL=1mA	/INT
	V_{OL2}	GND		GND+0.4		VDD =3V, IOL=1mA	
	V_{OL3}	GND		GND+0.5		VDD =5V, IOL=1mA	FOUT
	V_{OL4}	GND		GND+0.3		VDD =3V, IOL=0.5mA	
Input Leak Current	I_{LK}	-0.1		0.1	uA	SDA, SCL， V_{IN} = V_{DD} or GND	
Output Leak Current	I_{OZ}	-0.1		0.1	uA	SDA, V_{IN} = V_{DD} or GND	

5.5 AC Characteristics

Table6. AC Characteristics

V_{DD}=1.6V ~ 5.5V; Ta=-40℃ ~ +85℃

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}			400	kHz
SCL Low Voltage Time	t_{LOW}	1.3			us
SCL How Voltage Time	t_{HIGH}	0.6			us
Start condition hold time	$t_{HD;\ STA}$	0.6			us
Start condition setup time	$t_{SU;\ STA}$	0.6			us
Stop condition setup time	$t_{SU;\ STO}$	0.6			us
Bus idle time between start condition and stop condition	t_{RCV}	1.3			us
Data setup time	$t_{SU;\ DAT}$	100			ns
Data hold time	$t_{HD;\ DAT}$	0			ns
SCL, SDA rising time	t_r			0.4	us
SCL, SDA falling time	t_f			0.4	us

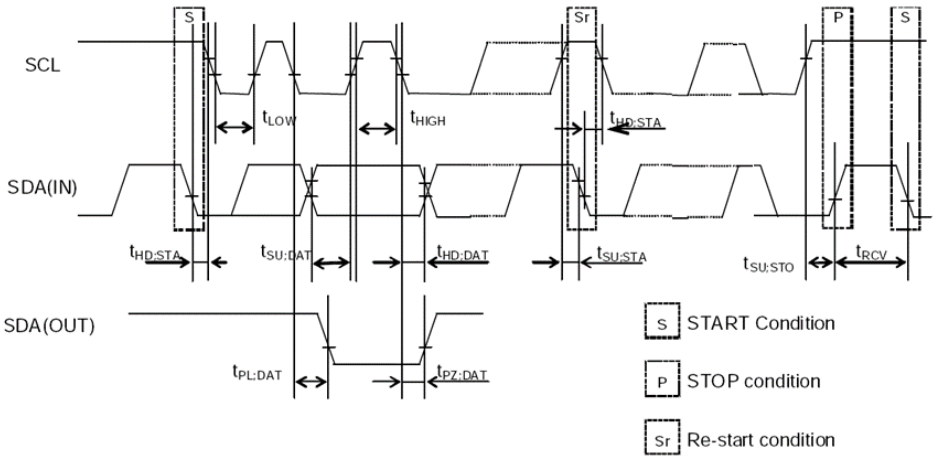


Figure 2. I^2C bus Timing Chart

Note：When the master device gets access to this slave device through I2C, the whole operation duration should be less than 1s, otherwise it will be reset by the I2C bus through the internal bus overtime function.

6 Registers

6.1 Register Lists

Address 0x10~0x1F: Basic Time and Calendar Registers

Address 0x20~0x2F: RAM Register Group

Address 0x30~32: Extended Register Group

Table1. Basic Time and Calendar Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x10	SEC	○	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				R/W
0x11	MIN	○	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R/W
0x12	HOUR	○	○	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0x13	WEEK	○	6	5	4	3	2	1	0	R/W
0x14	DAY	○	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x15	MONTH	○	○	○	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				R/W
0x16	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				R/W
0x17	RSV	Reserved								R/W
0x18	MIN Alarm	AE	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R/W
0x19	HOUR Alarm	AE	●	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0x1A	WEEK Alarm	AE	6	5	4	3	2	1	0	R/W
	DAY Alarm		●	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x1B	Timer Counter 0	128	64	32	16	8	4	2	1	R/W
0x1C	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256	R/W
0x1D	Extension Register	FSEL [1]	FSEL [0]	USEL	TE	WADA	TSEL [2]	TSEL [1]	TSEL [0]	R/W
0x1E	Flag Register	○	○	UF	TF	AF	Reserved	VLF	○	R/W
0x1F	Control Register	TEST	STOP	UIE	TIE	AIE	TSTP	Reserved	Reserved	R/W
0x20~| 0x2F	RAM	●	●	●	●	●	●	●	●	R/W
0x30	RSV	Reserved								R/W
0x31	RSV	Reserved								R/W

Note:

1, After power-up reset or in case VLF bit returns “1”, make sure to initialize all registers before using the RTC.

2. The default value of register after power on:

Initial 0: TEST、WADA、USEL、TE、FSEL[1:0]、TSEL[1:0]、UF、TF、AF、UIE、TIE、TSTP

Initial 1: VLF、TSEL[2].

3.The bits marked with "○" can be read out "0" after initializing.

4.The bits marked with "●" are RAM bits which can be used to write or read any data.

5.Only 0 can be written to UF、TF、AF and VLF bits.

6.Make sure "0" to be written for TEST bits which are used for manufacturing testing only.

6.2 Details of Registers

6.2.1 Clock counter registers

Table2. Second、Minute and Hour Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x10	SEC	○	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				0x00
0x11	MIN	○	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x00
0x12	HOUR	○	○	BCD code, Hour tens place, 0-2		0x00				0x00

SEC: BCD format, Value: 0~59

MIN: BCD format, Value: 0~59

HOUR: BCD format, Value: 0~23

Table3. Week Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x13	WEEK	○	6	5	4	3	2	1	0	0x40

WEEK: Value 01h, 02h, 04h, 08h, 10h, 20h, 40h. Only one bit can be set to 1 each time, all others must be set to 0.

Table4. WEEK Register Value table

WEEK	Data	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sunday	01h	0	0	0	0	0	0	0	1
Monday	02h	0	0	0	0	0	0	1	0
Tuesday	04h	0	0	0	0	0	1	0	0
Wednesday	08h	0	0	0	0	1	0	0	0
Thursday	10h	0	0	0	1	0	0	0	0
Friday	20h	0	0	1	0	0	0	0	0
Saturday	40h	0	1	0	0	0	0	0	0

Table5. Day Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x14	DAY	○	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				0x01

DAY: BCD format, the value range will be adjusted automatically according to the month setting and if a leap year or not.

Table6. DAY Register Value Range

Month	Day Value Range
1, 3, 5, 7, 8, 10, 12	1~31
4, 6, 9, 11	1~30
February in normal year	1~28
February in leap year	1~29

Table7. Month and Year Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x15	MONTH	○	○	○	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				0x01
0x16	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				0x00

MONTH: BCD format, Value1~12
YEAR: BCD format, Value0~99(2000~2099)
Example: 2020/01/01 Wednesday 21:18:36

Table8. Example of time setting

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x10	SEC	○	0	1	1	0	1	1	0
0x11	MIN	○	0	0	1	1	0	0	0
0x12	HOUR	○	○	1	0	0	0	0	1
0x13	WEEK	○	0	0	0	1	0	0	0
0x14	DAY	○	○	0	0	0	0	0	1
0x15	MONTH	○	○	○	0	0	0	0	1
0x16	YEAR	0	0	1	0	0	0	0	0

6.2.2 Alarm registers

Table9. Alarm Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x18	MIN Alarm	AE	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x00
0x19	HOUR Alarm	AE	•	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				0x00
0x1A	WEEK Alarm	AE	6	5	4	3	2	1	0	0x00
	DAY Alarm		•	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				

Alarm interruption can be generated with the setting of these registers and the cooperation of AIE、AF and WADA.

WEEK Alarm/Day Alarm: WADA control bit 0x0A can choose week alarm or day alarm, details refer to 0x1D register bit3

AE（Alarm Enable）：Alarm Enable bit，0-Enable；1-Disable.

AF function refer to 0x1E register bit3.

AIE function refer to 0x1F register bit3.

6.2.3 Timer registers

Table10. Timer Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x1B	Timer Counter 0	128	64	32	16	8	4	2	1	0x00
0x1C	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256	0x00

Alarm interruption can be generated with the setting of these registers and the cooperation of TE、TF 、TIE and TSEL[1:0].

TE function refer to 0x1D register bit4.

TF function refer to 0x1E register bit4.

TIE function refer to 0x1F register bit4.

TSEL[1:0] function refer to 0x1D register bit2, bit1 and bit0.

6.2.4 Extension registers

Table11. Extension Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x1D	Extension Register	FSEL [1]	FSEL [0]	USEL	TE	WADA	TSEL [2]	TSEL [1]	TSEL [0]	0x04

Used for the specified functions, including Alarm、 Time Update Interruption、Setting and etc.

WADA（Week Alarm/Day Alarm）： 0-WEEK Alarm, 1-DAY Alarm。

USEL（Update Interrupt Select）：0-Interrupt per Second（Default），1-Interrupt per Minute。

TE（Timer Enable）：0- Disable Timer Interrupt function, 1-Enable Timer Interrupt function。

FSEL[1]，FSEL[0] to confirm the output frequency. Shown as below table：

Table12. FSEL Table

FSEL [1]	FSEL [0]	FOUT Frequency
0	0	Disable
0	1	1Hz output
1	0	1024Hz output
1	1	32768Hz Output

TSEL[2]，TSEL[1]，TSEL[0]：Timer/Counter Clock configuration bits, just as below table：

Table13. TSEL Table

TSEL [2]	TSEL [1]	TSEL [0]	Timer/Counter Clock	Interruption duration
0	0	0	4096Hz（244.14us）	122uS
0	0	1	64Hz（15.625ms）	7.813mS
0	1	0	1Hz（S）	7.813mS
0	1	1	1/60Hz（Min）	7.813mS
1	0	0	1/3600Hz（Hour）	7.813mS

6.2.5 Flag Register

Table14. Flag Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x1E	Flag Register	○	○	UF	TF	AF	Reserved	VLF	○	0x26

UF（Update Flag）：Time Update Flag, when time update interruption generates, this bit will change from “0”to “1”,and keep this value until written to “0” by software;

TF（Timer Flag）：Timer Flag, when timer interruption generates, this bit will change from “0”to “1”,and keep this value until written to “0” by software;

AF（Alarm Flag）：Alarm Flag, when Alarm Interruption generation, this bit will change from “0”to “1”,and keep this value until written to “0” by software;

VLF（Voltage Low Flag）：Voltage Low Flag, when voltage is lower than 1.3V ,this bit will be set to”1”, and keep this value until written to “0” by software。

6.2.6 Control Register

Table15. Control Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x1F	Control Register	TEST	STOP	UIE	TIE	AIE	TSTP	Reserved	Reserved	0x00

TEST：Test bit for manufacture，must always be“0” when used and cannot be changed by user;

UIE（Update Interrupt Enable)：When UF changes from“0”to“1”，this bit can control if the interruption generates or not。0-Did not generate（/INT maintain high resistance），1-generate the interruption（/INT changes from high resistance to low voltage）。

TIE（Timer Interrupt Enable）：When TF changes from“0”to“1”，this bit can control if the interruption generates or not。0-Did not generate（/INT maintain high resistance），1-generate the interruption（/INT changes from high resistance to low voltage）。

AIE（Alarm Interrupt Enable）：When AF changes from“0”to“1”，this bit can control if the interruption generates or not。0-Did not generate（/INT maintain high resistance），1-generate the interruption（/INT changes from high resistance to low voltage）。

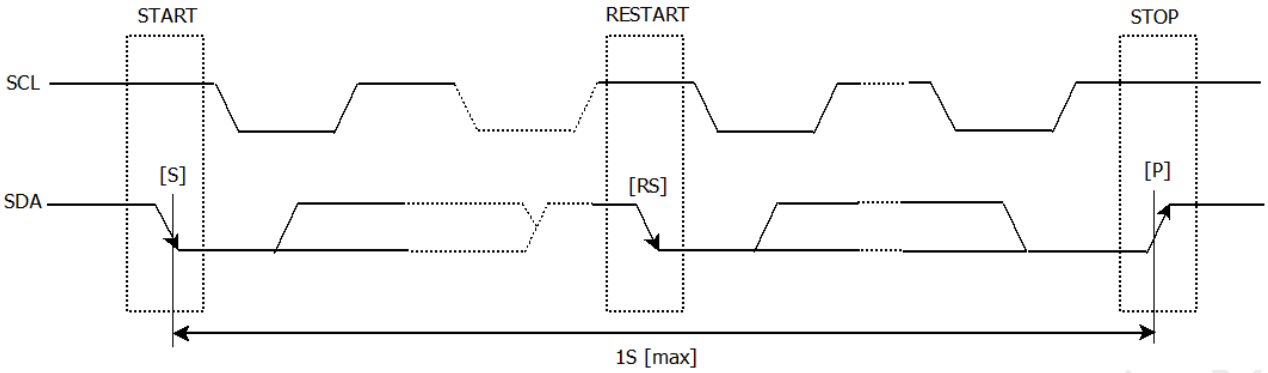
TSTP (Timer Stop): This bit is used to stop the count-down timer, always be used with STOP at the same time.

STOP: Used to stop the timer operation. When “STOP=1”, all timer update and calendar stop working. Fixed period timer stops the interruption partly; the output frequency can be 32768Hz, but 1Hz and 1024hz are disable.

Table16. STOP & TSTP Setting Table

STOP	TSTP	Description
0	0	When TSTP is written to“0”，Start timer
	1	When TSTP is written to“1”，Stop timer
1	X	At this moment, when frequency output is set to 64Hz，1Hz，1/60Hz or 1/3600Hz，the timer stop working。

7 I²C Bus Interface



I²C bus supports bi-directional communications through a serial clock line SCL and a serial data line SDA. I²C bus device can be defined as "Master" and "Slave". INS5101A (A) can only be used as Slave.

7.1 Cautions

I²C bus includes START, RESTART, STOP conditions, the duration between START and STOP must be less than 1 second just in case the bus to be set to standby mode automatically. If the time is more than 1S, INS5101A(A) will reset I²C Interface.

INS5101A(A) I²C bus interface supports single byte read/write operations as well as multiple bytes incremental access. After 0xFF address, the next one will be 0x00.

7.2 Slave Address

Table17. I²C Bus Slave Address

Transfer data	Slave address							R/W
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
65h (Read)	0	1	1	0	0	1	0	1 (Read)
64h (Write)								0 (Write)

INS5101A(A) I²C bus Slave Address is [0110 010*].

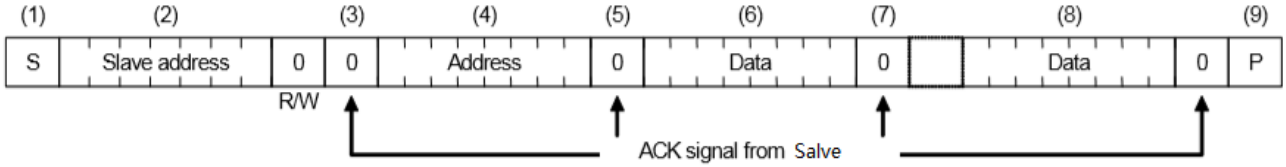
7.3 I²C bus protocol

It is assumed CPU is master and INS5101A(A) is slave in this section.

7.3.1 Write process

I²C bus includes an address auto-increment function, once the initial address has been specified, the INS5101A(A) increments (+1) the address automatically after each data is sent, then to write next data.

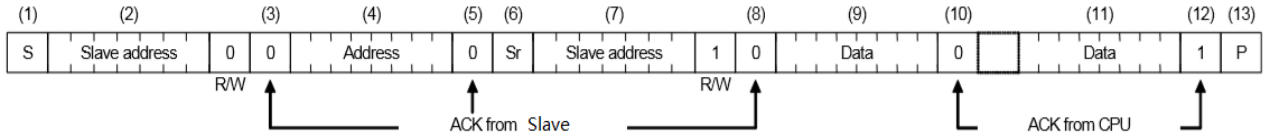
(1) CPU sends start condition[S]
(2) CPU sends INS5101A's slave address with R/W bit to set to write mode
(3) CPU verifies ACK signal from INS5101A
(4) CPU sends write address to INS5101A
(5) CPU verifies ACK signal from INS5101A
(6) CPU sends write data to the address specified at step (4)
(7) CPU verifies ACK signal from INS5101A
(8) Repeat (6) (7) if multiple bytes need to be written, address will be incremented automatically
(9) CPU ends stop condition[P]



7.3.2 Read process

Writing the address to be read with write mode firstly, then reading the data with read mode.

(1) CPU sends start condition[S]
(2) CPU sends INS5101A's slave address with R/W bit to set to write mode
(3) CPU verifies ACK signal from INS5101A
(4) CPU sends address for reading from INS5101A
(5) CPU verifies ACK signal from INS5101A
(6) CPU sends RESTART condition [Sr]
(7) CPU sends INS5101A's slave address with R/W bit to set to read mode
(8) CPU verifies ACK signal from INS5101A
(9) CPU reads data from the specified address in step (4)
(10) CPU sends ACK signal for "0"
(11) Repeat (9) (10) if multiple bytes need to be read, address will be incremented automatically
(12) CPU sends ACK signal for "1"
(13) CPU sends stop condition[P]



8 Reflow Soldering Curve

Standard: IPC/JEDEC J-STD-020

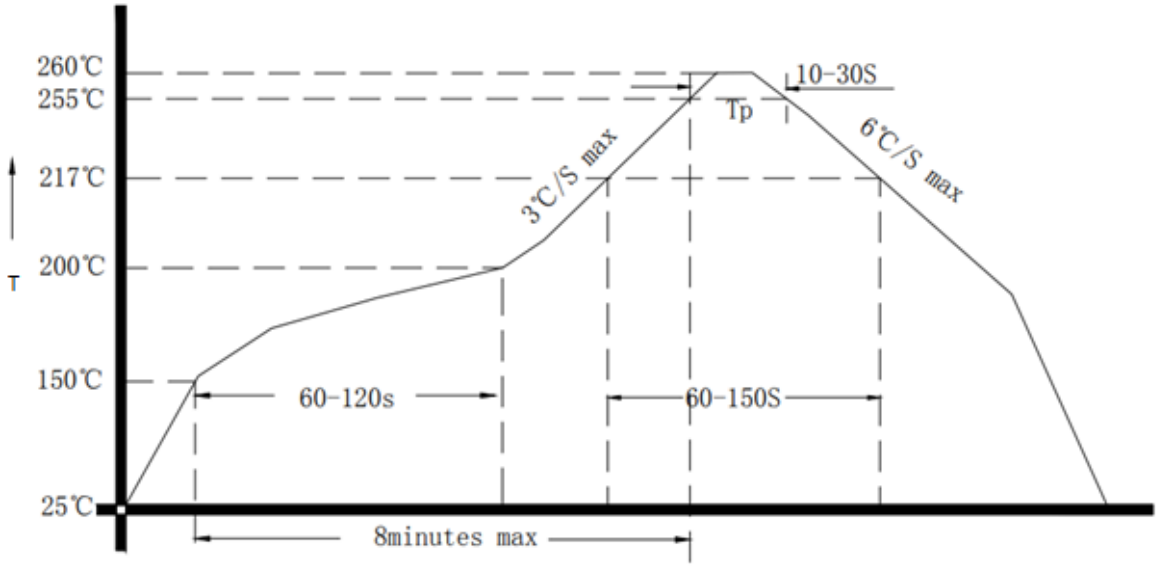


Figure 3. Reflow Soldering Curve

Note: It is suggested to solder IC under the condition shown in the curve above. Must pay attention to the temperature and time when manual soldering,

9 Dimensions

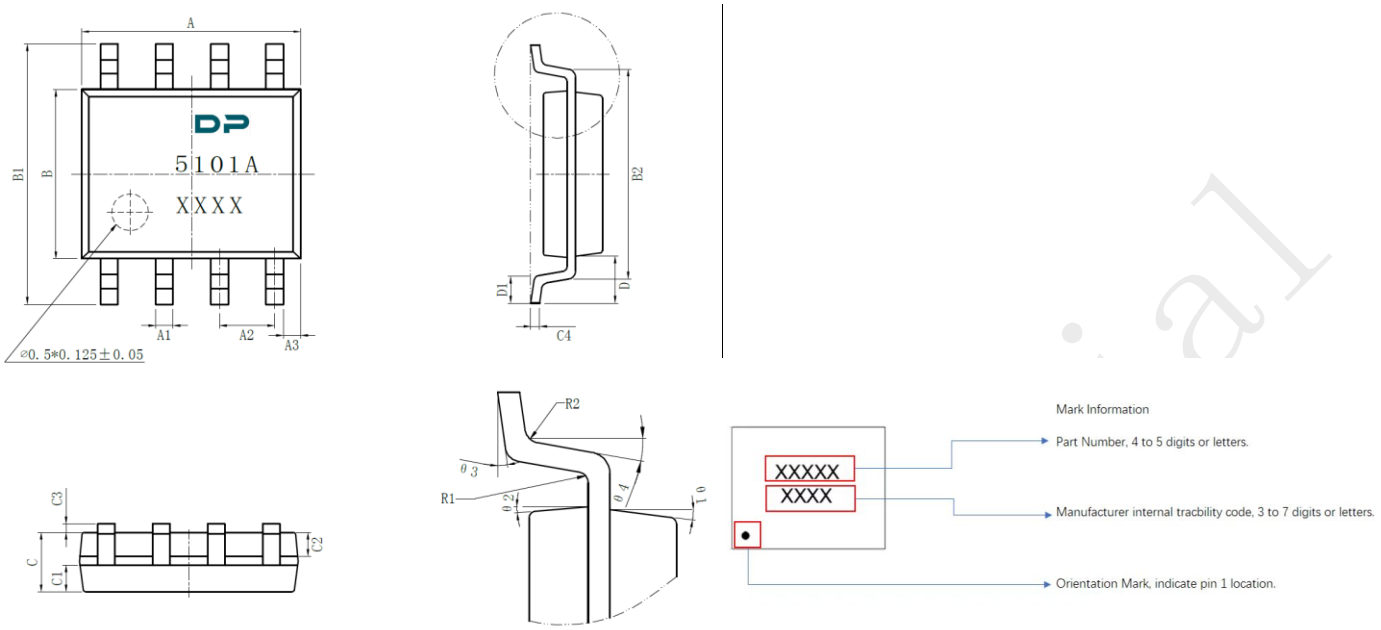


Figure 4. Dimension and Mark information

Dimension	Min.	Typ.	Max.
A	4.8	4.9	5.0
A1	0.356	--	0.456
A2	--	1.27	--
A3	--	0.345	--
B	3.8	3.9	4.0
B1	5.8	6.0	6.2
B2	--	5.00	--
C	1.3	--	1.6
C1	0.55	--	0.65
C2	0.55	--	0.65

(Unit: mm)

Dimension	Min.	Typ.	Max.
C3	0.05	--	0.20
C4	0.203	--	0.233
D	--	1.05	--
D1	0.4	--	0.8
R1	--	0.2	--
R2	--	0.2	--
θ1	17°		
θ2	13°		
θ3	0°~8°		
θ4	4°~12°		

(Unit: mm)

10 Package Information

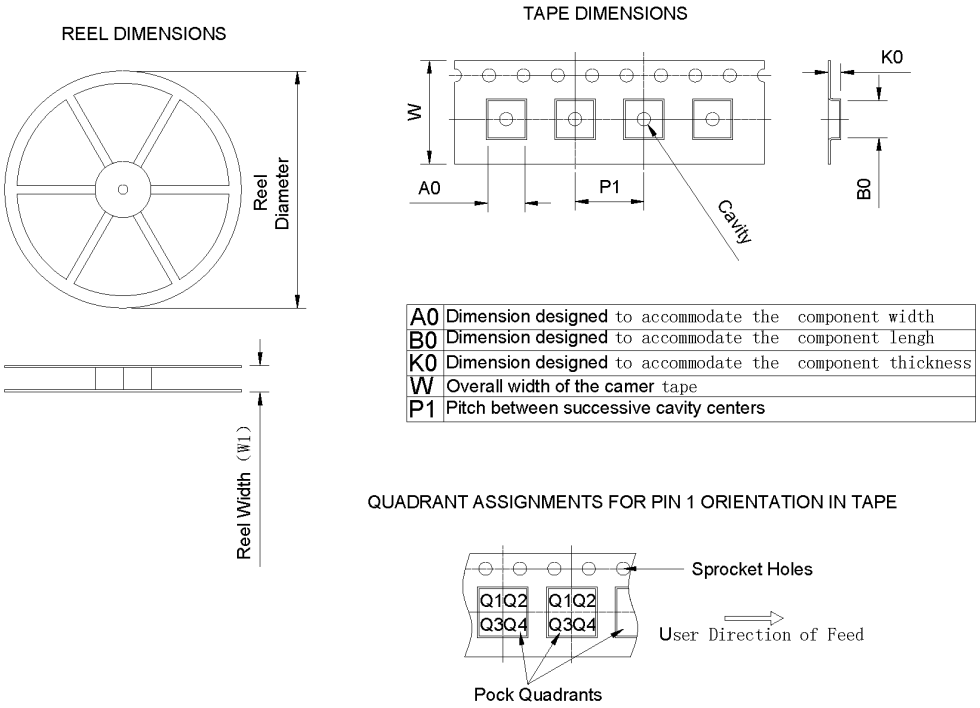


Figure 5. Package information

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	PIN1 Quadrant
INS5101A/ INS5101AA	SOP	8	3000	330±1	12.4±0.2	6.40	5.30	2.10	8.00± 0.1	12.00 ±0.1	Q1