Customer Code :_____

DATASHEET

DAPU P/N: **DPBF21250001**

Plot			The Label
Drew	Audited	Approved	
Amway.wei	Carry.Wang	James.Liu	
Date: 2018.04.04			Stamp, please! Thanks!

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1、Electrical Parameters

MODEL：DPBF21250001							
No.	Parameters	SYM.	Electrical Spec.				Notes
			Min.	Typ.	Max.	Units	
1	Nominal Frequency	FL		212.50		MHz	
2	Output Waveform			LVDS			
3	Supply Voltage		2.97	3.3	3.63	V	
4	Frequency Stability	F-stab	-25		+25	$\times 10^{-6}$	Inclusive of initial tolerance, operating temperature, rated power supply voltage, and load variations
5	Operating Temperature	T-opr	-40	~	85	℃	Industrial
			-20		70	℃	Extended Commercial
6	Storage Temperature	T-stg	-65	~	+150	℃	
7	Current Consumption	Idd	-	47	55	mA	
8	OE Disable Current	I_OE			35	mA	
9	Output Disable Leakage Current	I_leak			1	μA	
10	Standby Current	I_std			100	μA	
11	Rise/Full Time	Tr、Tf		495	600	ps	20%~80%
12	Duty Cycle	DC	45		55	%	
13	First Year Aging	F_aging1	-2	-	+2	$\times 10^{-6}$	25℃
14	10-year Aging	F_aging10	-5	-	+5	$\times 10^{-6}$	25℃
15	Input Voltage High	VIH	70%	-	-	Vdd	Pin 1 , ST
16	Input Voltage Low	VIL	-	-	30%	Vdd	Pin 1 , ST
17	Input Pull-up Impedence	Z_in		100	250	KΩ	Pin 1, OE logic high or logic low, or ST logic high
18	Start up Time	T_start	-	6	10	ms	Measured from the time Vdd reaches its rated minimum value
19	OE Enable/Disable Time	T_oe	-	-	115	ns	
20	Differential Output Voltage	VOD	250	350	450	mA	
21	VOD Magnitude Change				50	mV	
22	Offset Voltage	VOS	1.125	1.2	1.375	V	
23	VOS Magnitude Change				50	mV	
24	Resume Time	T_ resume		6	10	ms	In Standby mode, measured from the time ST pin crosses50% threshold.
25	RMS Period Jitter	T_jitt	-	1.2	1.7	ps	
26	RMS Phase Jitter (random)	T_phj		0.6	0.85	ps	Integration bandwidth =12kHz to 20MHz

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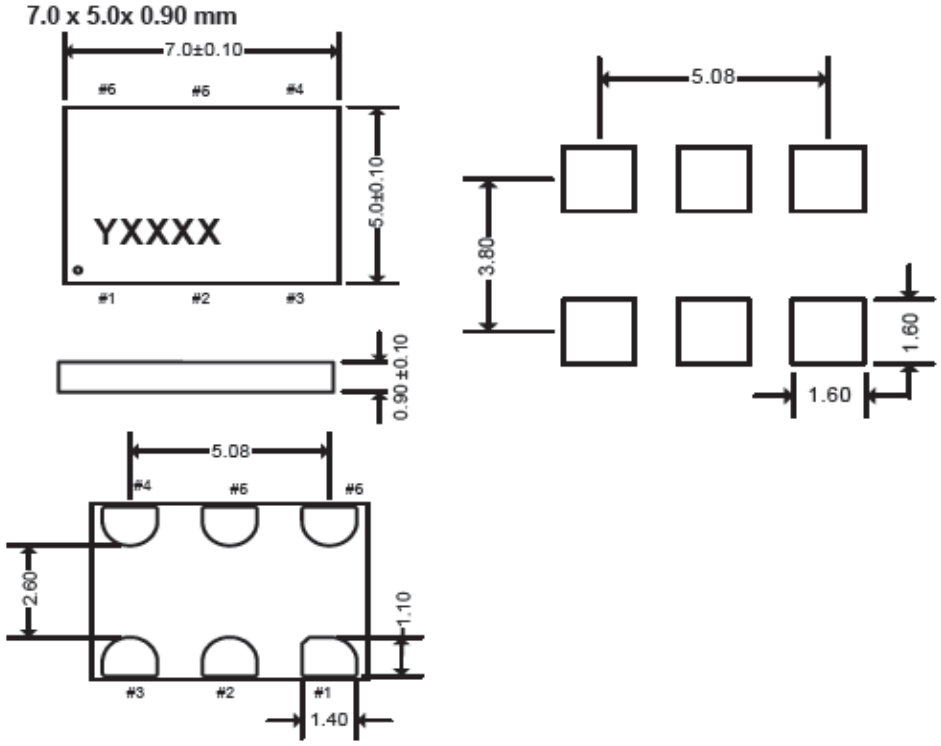
2、Mechanical Structure(mm)



unit:mm

Pin Description

Pin	Map	Functionality	
1	OE	Input	H or Open: specified frequency output L: output is high impedance
	$\overline{ST}$	Input	H or Open: specified frequency output L: Device goes to sleep mode. Supply current reduces to I_std.
2	NC	NA	No Connect; Leave it floating or connect to GND for better heat dissipation
3	GND	Power	VDD Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage

Note1: Tolerance±0.2mm without mark

Note2: Referential weight 0.2g

Note3: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device

Note4: A capacitor of value 0.1μ F or higher between Vdd and GND is required.

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3、Waveform Diagrams

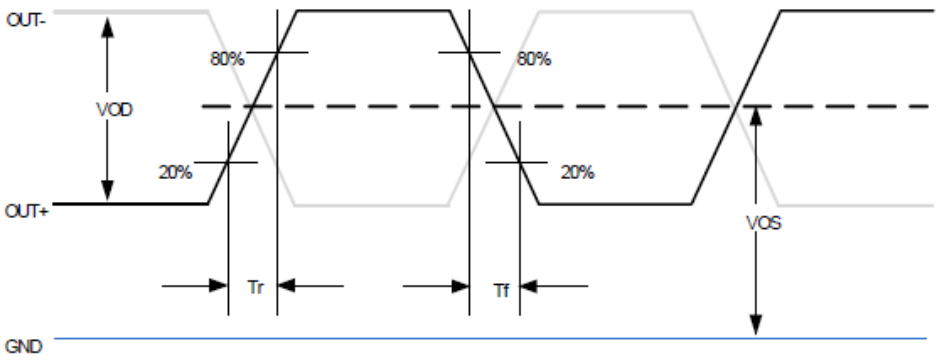

Figure 2. LVDS Voltage Levels per Differential Pin (OUT+/OUT-)

4、Termination Diagrams

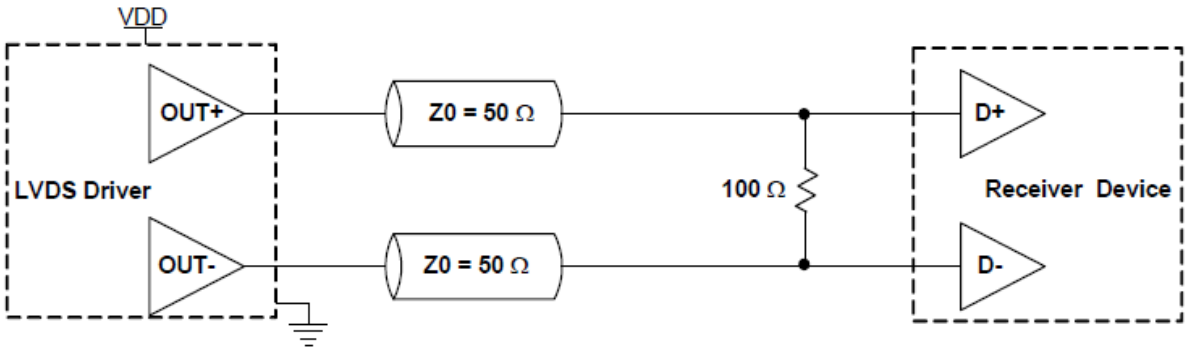

Figure 6. LVDS Single Termination (Load Terminated)

5、Package: Tape & Reel (mm)