Customer Code :_____

# DATASHEET

DAPU P/N: **DP7X66000002**

| Plot | | | The Label |
|---|---|---|---|
| Drew | Audited | Approved | |
| Amway.wei | Carry.Wang | James.Liu | |
| Date: 2017.02.28 | | | Stamp, please! Thanks! |


## Guangdong Dapu Telecom Technology Co.,Ltd

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# 1、Electrical Parameters

| **MODEL：DP7X66000002** | | | | | | | |
|---|---|---|---|---|---|---|---|
| No. | Parameters | SYM. | Electrical Spec. | | | | Notes |
| | | | Min. | Typ. | Max. | Units | |
| 1 | Nominal Frequency | FL | | 66.00 | | MHz | |
| 2 | Output Waveform | | | LVCMOS | | | |
| 3 | Vdd | | -0.5 | | 4 | V | |
| 4 | Supply Voltage | | 2.25 | 2.5 | 2.75 | V | |
| 5 | Frequency Stability | F-stab | -20 | | +20 | $\times 10^{-6}$ | Inclusive of Initial tolerance at 25℃, 1st year aging at 25℃, and variations over operating temperature, rated power supply voltage and load. |
| 6 | Operating Temperature | T-opr | -40 | ~ | +85 | ℃ | |
| 7 | Storage Temperature | T-stg | -65 | ~ | +150 | ℃ | |
| 8 | Current Consumption | Icc | - | 3.7 | 4.2 | mA | |
| 9 | OE Disable Current | I_OD | | | 4.2 | mA | |
| 10 | Standby Current | I_std | | 1.1 | 2.5 | μA | |
| 11 | Rise/Full Time | Tr、Tf | | 1 | 2 | ns | 20%~80% |
| 12 | Duty Cycle | DC | 45 | | 55 | % | |
| 13 | Output Voltage High | VOH | 90% | - | - | Vdd | IOH = -4 mA |
| 14 | Output Voltage Low | VOL | - | - | 10% | Vdd | IOL = 4 mA |
| 15 | Input Voltage High | VIH | 70% | - | - | Vdd | Pin 1 , ST |
| 16 | Input Voltage Low | VIL | - | - | 30% | Vdd | Pin 1 , ST |
| 17 | Input Pull-up Impedence | Z_in | 50 | 87 | 150 | KΩ | Pin 1, OE logic high or logic low, or ST logic high |
| 18 | Start up Time | T_start | - | - | 5 | ms | Measured from the time Vdd reaches its rated minimum value |
| 19 | Enable/Disable Time | T_oe | - | - | 130 | ns | |
| 20 | Resume Time | T_ resume | | | 5 | ms | |
| 21 | RMS Period Jitter | T_jitt | - | 1.8 | 3 | ps | |
| 22 | Peak to Peak Period Jitter | T_pk | | 12 | 25 | ps | |
| 23 | Phase Jitter | T_phj | - | 0.5 | 0.9 | ps | 900 kHz～7.5 MHz |
| 24 | Mechanical Shock | | MIL-STD-883F,Method 2002 | | | | |
| | Mechanical Vibration | | MIL-STD-883F,Method 2007 | | | | |
| | Temperature Cycle | | JESD22, Method A104 | | | | |
| | Solderability | | MIL-STD-883F,Method 2003 | | | | |
| | Moisture Sensitivity Level | | MSL1@260℃ | | | | |

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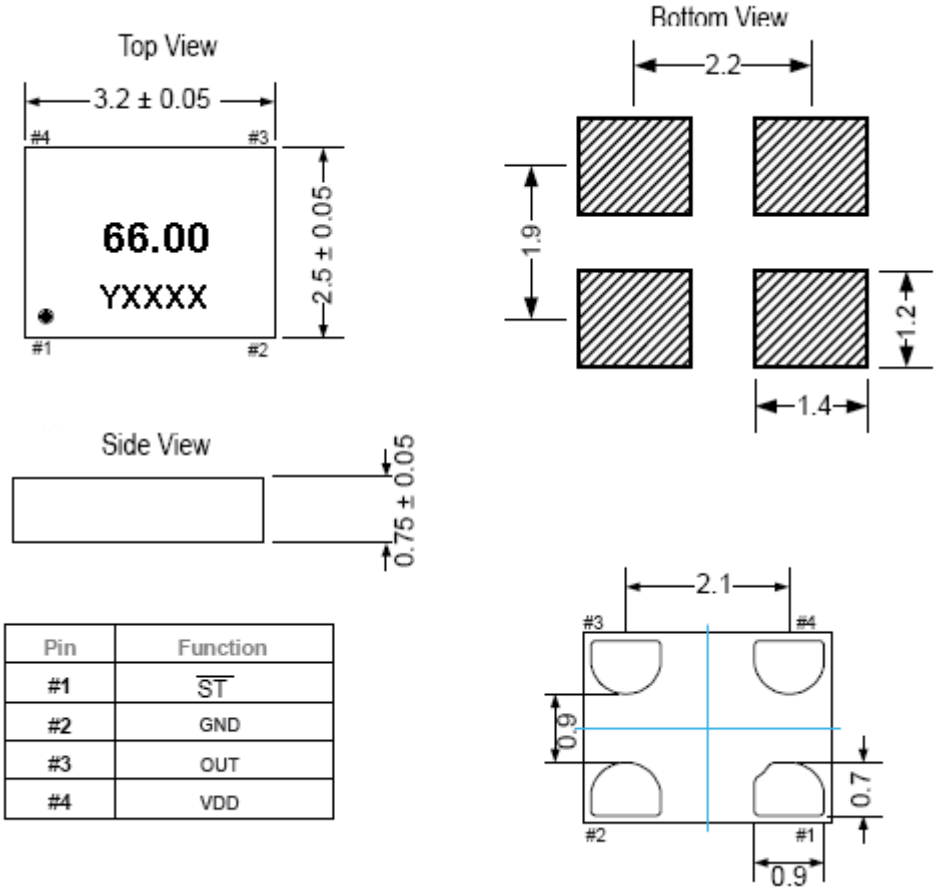
## 2、Mechanical Structure(mm)




| Pin | Function |
|---|---|
| #1 | $\overline{ST}$ |
| #2 | GND |
| #3 | OUT |
| #4 | VDD |

**unit:mm**

**Note1:**Tolerance±0.2mm without mark

**Note2:** Referential weight 0.2g

**Note3:**Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device

**Note4:** A capacitor of value 0.1 μ F or higher between Vdd and GND is required

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## 3、Test Circuit And Waveform

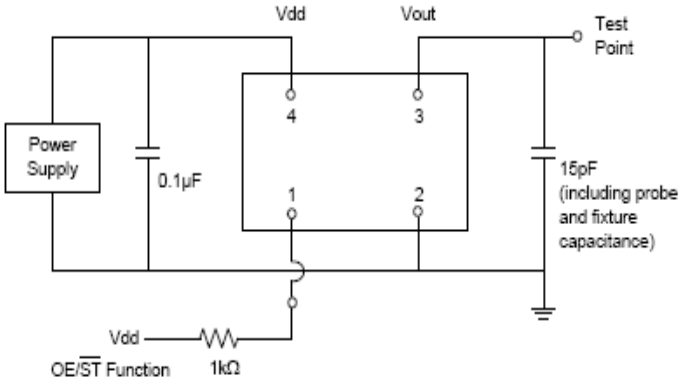



Figure 2. Test Circuit

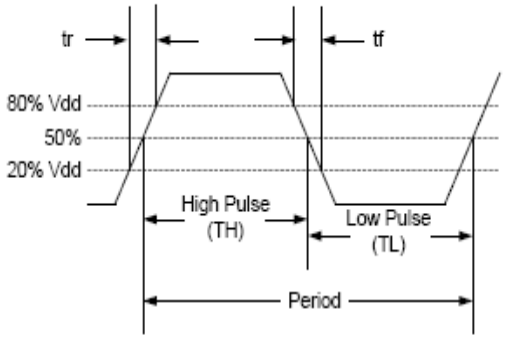
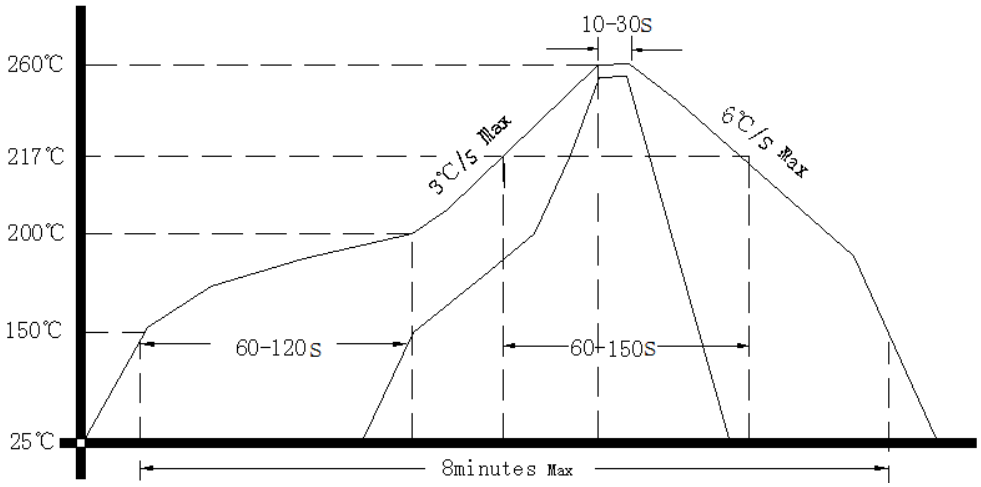



Figure 3. Waveform

## 4、Reflow Soldering Curve (RoHS)




## 5、Package: Tape & Reel (mm)