

Travelling Merchant: _____

DATASHEET

Standard: DP7W20000001Y75YM20001

Plot			The Label
Drew	Audited	Approved	Stamp, please! Thanks!
Date: 2014.09.04			

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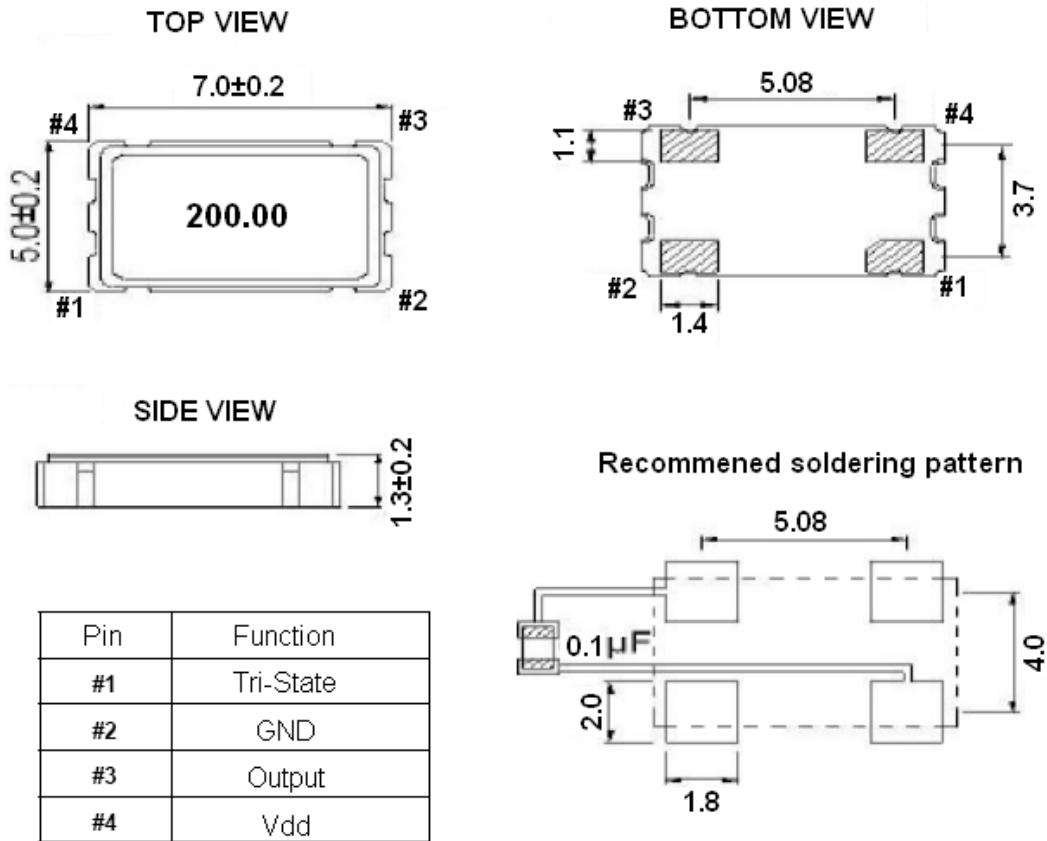
1、Electrical Parameters

MODEL: DP7W2000001							
No.	Parameters	SYM.	Electrical Spec.				Notes
			Min.	Typ.	Max.	Units	
1	Nominal Frequency	FL	200.00			MHz	
2	Supply Voltage	VDD	2.97	3.3	3.63	V	
3	Current consumption	-	-	-	50	mA	
4	Output Waveform	-	CMOS			-	
5	Standard Output Load	-	15pF				
6	Frequency Stability	-	-50	~	+50	$\times 10^{-6}$	Frequency stability includes frequency tolerance@25°C and frequency stability vs. operating temperature range and voltage variance and first year aging.
7	Frequency Stability	vs. Tolerance	-20	-	+20	$\times 10^{-6}$	Frequency at 25°C
8		vs. Temperature	-20	-	+20	$\times 10^{-6}$	Referenced to the frequency at 25°C
9		vs. Supply Voltage	-5	-	+5	$\times 10^{-6}$	Supply voltage varied $\pm 10\%$ at 25°C
10	Operating Temperature	Topr	-40	-	+85	°C	The operating temperature Range over which the Frequency stability is measured
11	Storage Temperature	Tstg	-55	-	+125	°C	
12	Duty Cycle	-	40	50	60	%	
13	Start-up Time	Tosc	-	-	8	mS	
14	Rise/Fall Time	Tr/ Tf	-	-	3	nS	
15	Output High Logic1	-	2.97			V	
16	Output Low Logic0	-			0.33	V	
17	Aging	-	-3	-	+3	$\times 10^{-6}$	Frequency drift in first year
18	Output Active		2.31or			V	Pin 1 Tri-state
19	Output in High-Impedance state	-	-	-	0.99	V	
20	Period Jitter (Pk-Pk)				200	pS	
21	Period Jitter (RMS)				1.0	pS	12KHz-20.00MHz



22	ESD Level	Human Body Model,class2: 2000V to 4000V; ANSI/ESDA/JEDEC JS-001-2010.
		Machine Model, class B: 200V to 400V; ANSI/ESDA/JEDEC JS-001-2010.
23	Moisture Sensitivity Level	Level 2.
24	Vibration	Test Condition: 0.75mm ;acceleration:10g;10Hz~2000Hz, one cycle per 30 min, test 2 hour. (3 times for each 3 directions X ,Y , Z) .IEC 68-2-06 Test Fc.
25	Shock	100g; 6ms; half sine wave (3 times for each 3 directions X ,Y , Z),IEC 68-2-27 Test Ea/Severity 50A.

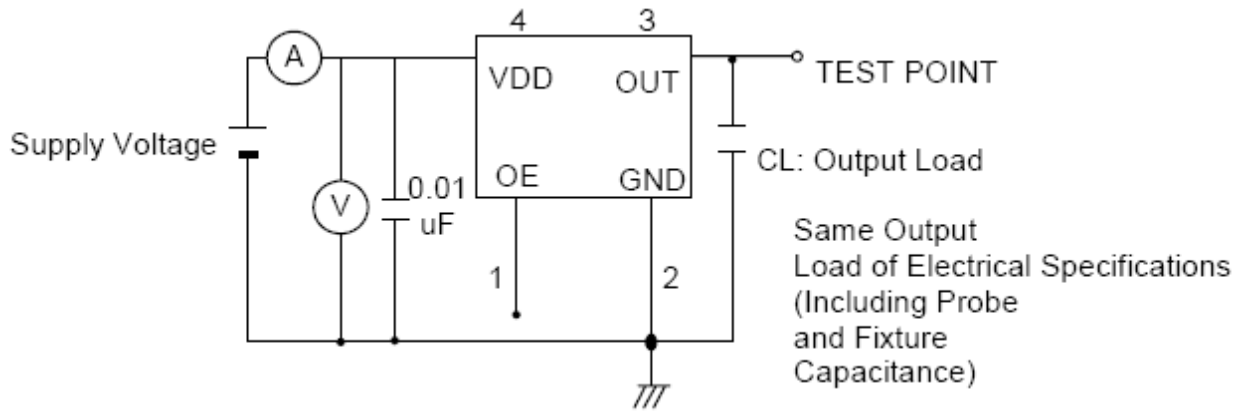
2、Mechanical Structure(mm)



Note1: Tolerance ±0.2mm

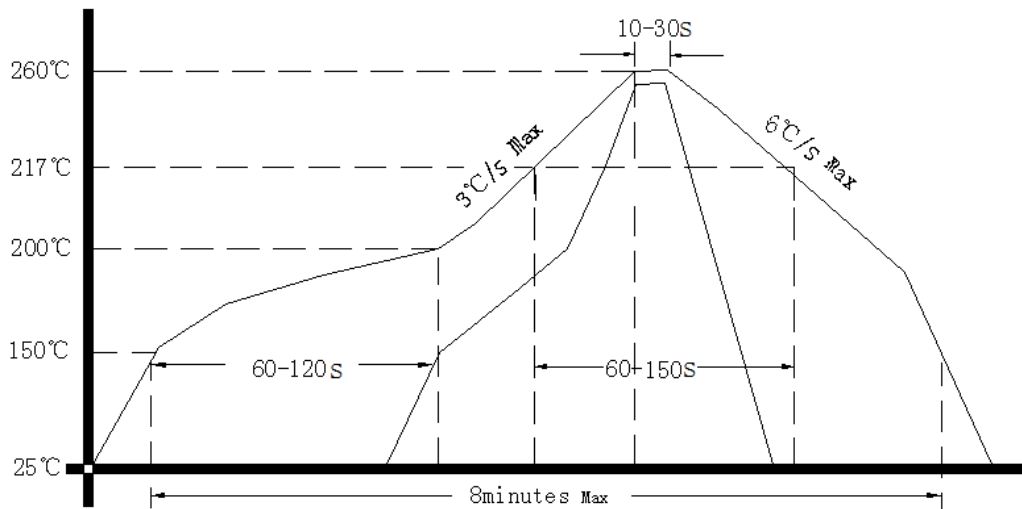


3、 Test Diagram



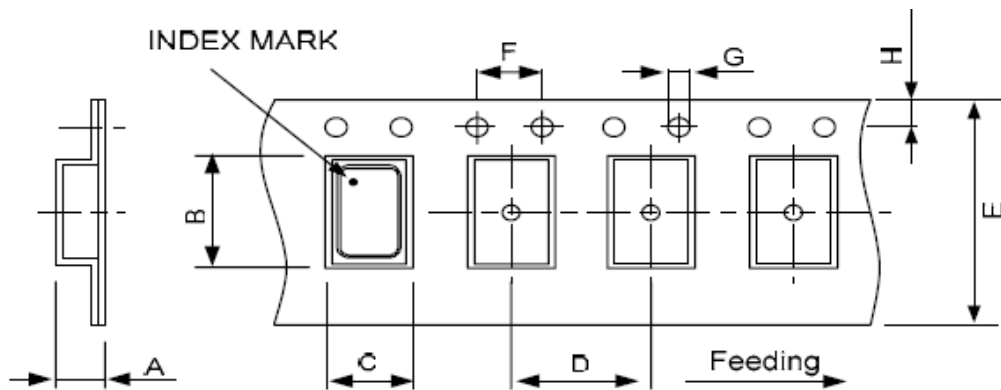
Control input (output enable/disable)
Logic 1 or open on pad 1: Oscillator output
Logic 0 on pad 1 : Disable output to high impedance

4、 Reflow Soldering Curve (RoHS)





5、 Package: Tape & Reel (mm)



DIMENSIONS	A	B	C	D	E	F	G	H	(UNIT : mm)
	2.30	7.90	5.45	8.00	16.00	4.00	1.50	1.75	

REMARK :

