Customer Code:

DATASHEET

DAPU P/N: **CM35B-C118-10.00MHz-A**

CustomerP/N: _____

DAPU			Customer Approval
Drew	Audited	Approved	
Amway.wei	Carry.Wang	James.Liu	
Date: 2019.10.10			Stamp, please! Thanks!

Guangdong Dapu Telecom Technology Co.,Ltd

Bldg 16, N.Ind. Zone, SSL Industry Park, Dongguan City, Guangdong Province, China

TEL：0086-0769-88010888 FAX：0086-0769-81800098

Table of Amendment

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Dongguan City, Guangdong Province,
PRC China
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Version	Revision contents	Prepared by	Revised date
1.0	The first issued	Amway	2019.10.10

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1. General Description

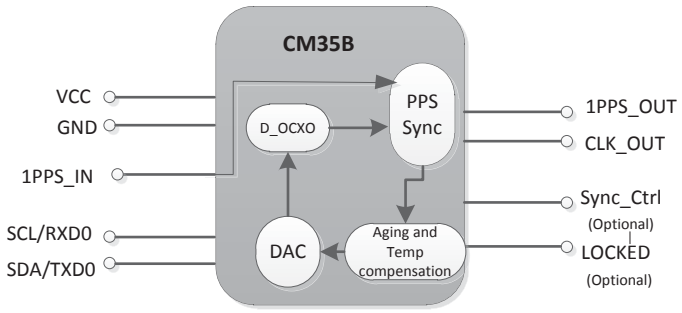

Figure 1 CM35B

Figure 1 is the basic diagram of CM35B. CM35B is a high-performance clock module designed to provide precise frequency and phase synchronizing with external time reference for telecom and other applications.

Key features:

- **Reference:** 1PPS and TOD from GNSS receiver, IEEE1588 etc.;
- **Temperature Stability:**±0.075ppb;
- **Holdover:** ±1.5μs/24h @Δ T=±20℃ after power-onfor5days and locked for 2dayscontinually;
- **Clocks Input and Output:**1PPS input, 1PPS output and 10MHz output;
- **Management Interface:**I2C(default), UART(optional);
- **Mechanical Size:**35mm*35mm*13mm.

2. Product Number

Table 1 Product Number

Product Number	Management Interface
CM35B-C118-10.00MHz-A	I2C Interface
CM35B-C118-10.00MHz-B	UART Interface*

Note: * UART could support firmware updating online and TOD message.

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3. Pin Definition

Table 2 Pin Definition

Pin group	Pin#	Pin Name	Type	Description
Supply Voltage	4	GND	GND	Ground
	7	VCC	PWR	Power Supply
Control and Status Pins	Y[1]	SYNC_CTRL	I	Synchronizing Procedure Control(Optional)
	X[1]	LOCKED	O	Locked Status(Optional)
I2C/UART	6[2]	SCL	I	For I2C mode, clock signal input.
		RXD0	I	For UART mode, Asynchronous Serial Data Input
	5[2]	SDA	IO	For I2C mode, data input and output
		TXD0	O	For UART mode, Asynchronous Serial Data Output
Input Clock	2	1PPS_IN	I	1PPS Reference Input.
Output Clocks	3	1PPS_OUT	O	1PPSOutput
	1	CLK_OUT	O	10.00MHz Output

Note: 1. Pin X and Pin Y are optional pins. These pins could be removed if customers don't need them.
2.Pin 5 and Pin6 are the I2C interface for CM35B-C118-10.00MHz-A, the UARTinterface for CM35B-C118-10.00MHz-B.

4. DCElectrical Parameters

Table 3DC Electrical Parameters

Parameter	Symbol	Minimum	Typical	Maximum	Units
HCMOSInput					
High Level Input Voltage	V_{IH}	2.4			V
Low Level Input Voltage	V_{IL}			0.4	V
HCMOSOutput					
High Level Output Voltage	V_{OH}	2.4			V
Low Level Output Voltage	V_{OL}			0.4	V

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5. Power Supply

Table 4 Power Supply

Item	Parameter	Minimum	Typical	Maximum	Units	Test Condition
Supply Voltage	Supply Voltage	4.75	5.0	5.25	V	
	Warm Up Current			2000	mA	
	Steady Current		500		mA	@25℃
	POWER-ON RECALL Voltage	2.2			V	Minimum VCC at which memory recall occurs
	VCC Ramp Rate	0.2			V/ms	

6. RF Output

Table 5 RF Output

Item	Parameter	Minimum	Typical	Maximum	Units
Clock Output	Waveform	Sine Wave			
	Load	45	50	55	Ω
	Output Power	5	7	9	dBm
	Harmonics			-40	dBc
	Spurious			-80	dBc
	Start-up time			1	Second

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7. Performance

7.1 Free Run Mode

Table 6Free Run Mode

Item	Parameter	Minimum	Typical	Maximum	Units	Test Condition
Clock Output	Nominal Frequency		10.00		MHz	Synchronizing with 1PPS reference.
	Frequency calibration (at 25°C ± 2°C)	-50		+50	$\times10^{-9}$	Referenceto nominal frequency. Note1.
	Frequency vs. Temperature (Peak-Peak)			0.075	$\times10^{-9}$	Vcc=5.0 V; O_{load}=50 Ω; $T_A$varies from-40℃ to 85℃, temperature slope less than 2℃per minute.
	Frequency vs. Power Supply	-0.01		+0.01	$\times10^{-9}$	Nominal VCC ± 5% variation
	Frequency vs. Load	-0.01		+0.01	$\times10^{-9}$	50 Ω ± 10% variation
	Frequency vs. Acceleration	-5		5	ppb/g	vs static orientation
	Daily Aging	-0.2		+0.2	$\times10^{-9}$	Vcc=5.0V; T_A=25℃.
	10 Yearly Aging	-0.25		+0.25	$\times10^{-6}$	
	Warm-up time			3	min	@ 25°C,Within 10ppb of frequency after1 hour of continuous operation
				5	min	@ -40°C,Within 10ppb of frequency after1 hour of continuous operation
	Retrace vs. operating temperature range		±1	±5	$\times10^{-9}$	24h on, 24h off and 1h on
	Phase Noise			-90	dBc/Hz	1Hz
				-120		10Hz
				-140		100Hz
				-145		1KHz
				-150		10KHz

Note1. 1 This characteristicmay be temporarily affected by assembly and soldering process. The frequency specificationsapply 48 hours after assembly. Nominal conditions apply unless otherwise stated

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7.2 Acquiring Mode

Table 7 Acquiring Mode

Item	Parameter	Minimum	Typical	Maximum	Units	Test Condition
1PPS Input	Nominal Frequency		1		Hz	Synchronizing with 1PPS reference.
	Waveformcompatibility		HCMOS			
	Pulse width	10			us	
	Time deviation (TDEV)		0.5	2	ns	Tau = 1s
			3	10	ns	Tau = 10s
			20	90	ns	Tau = 100s to 10 000s
1 PPS Output	Nominal Frequency		1		Hz	
	1PPS Output availability			50	s	after locking on 1PPS Input
	Waveformcompatibility		HCMOS			Table 2, Load 15pF // 10kΩ min
	Pulse Width		100		us	
	Rise and fall times			5	ns	10% to 90% level, 15pF load

7.3 Locked Mode

Table 8Locked Mode

Item	Parameter	Minimum	Typical	Maximum	Units	Test Condition
Clock Output	Nominal Frequency		10.00		MHz	Synchronizing with 1PPS reference.
	Time deviation (ADEV)		1.5	5	$\times10^{-12}$	Tau = 1s
			4	7	$\times10^{-12}$	Tau = 10s
			5	7	$\times10^{-12}$	Tau = 100s to 10 000s
	Phase Noise			-90	dBc/Hz	1Hz
				-120		10Hz
				-140		100Hz
				-145		1KHz
				-150		10KHz
1PPS Input	Nominal Frequency		1		Hz	Synchronizing with 1PPS reference.
	Waveformcompatibility		HCMOS			

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	Pulse width	10			us	
	Time deviation (TDEV)		0.5	2	ns	Tau = 1s
			3	10	ns	Tau = 10s
			20	90	ns	Tau = 100s to 10 000s
1 PPS Output	Nominal Frequency		1		Hz	
	Waveformcompatibility	HCMOS				Table 2, Load 15pF // 10kΩ min
	Pulse Width		100		us	
	Rise and fall times			5	ns	10% to 90% level, 15pF load
	Accuracy	-30		+30	ns	Synchronizing with 1PPS reference. Mean is 0, and standard deviation is 30ns. After 2 hours locked.

7.4 Holdover Mode

Table 9Holdover Mode

Item	Parameter	Minimum	Typical	Maximum	Units	Test Condition
Clock Output	Nominal Frequency		10.00		MHz	
	Frequency vs. Power Supply	-0.01		+0.01	$\times10^{-9}$	Nominal VCC ± 5% variation
	Frequency vs. Load	-0.01		+0.01	$\times10^{-9}$	50 Ω ± 10% variation
	Frequency vs. Acceleration	-5		+5	ppb/g	vs static orientation
	Time deviation (ADEV)		1.5	5	$\times10^{-12}$	Tau = 1s to 1000s
			2	6	$\times10^{-12}$	Tau = 10 000s
	Phase Noise			-90	dBc/Hz	1Hz
				-120		10Hz
				-140		100Hz
				-145		1KHz
				-150		10KHz
1 PPS Output	Nominal Frequency		1		Hz	

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	Waveformcompatibility	HCMOS				Table 2, Load 15pF // 10kΩ min
	Pulse Width		100		us	
	Rise and fall times			5	ns	10% to 90% level, 15pF load
	Acceptance window (depending on variant)	0.5			us	Programmable by customer
	Recovering speed after a holdover period withinthe acceptance window			3	ns/s	-Recovering speedprogrammable from 1 to3ns/s - No timeout occurred - No PPS muting
	Recovering after a holdover period out ofacceptance window			24	Hour	- Timeout occurred - PPS mutingC - Reset internal counter
	24 hours holdover	-1.5		+1.5	μs	ΔT=±20℃,24 hours holdover after poweredup 5daysand locked 2days,. Temperature slope less than 1℃ per minute.

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8. Management Interface

8.1I2C Interface (Only for CM35B-C118-10.00MHz-A)

I2C interface is used for management as a slave. It is compliant with Philips Semiconductors Inter-IC bus (I2C-bus) specification version 2and supports standard mode(0~100Kbit/s) and fast mode (400Kbit/s).

The number of ICsthat can be connected to the same bus is limited only by a maximum bus capacitance of 400pF.

The receiver's I2C address is set to 0b' 110 0000 by default and can be changed on request.

The I2C interface allows 128 slave registers to be addressed. As shown in I2C Register table only a few of these arecurrently implemented. Others are reserved for future uses or internal computation and must not be addressed.

Table 10 I2C Register Table

Register address	R/W	Register Name	Description	Message Info	
				Bytes	Data-Type
0x3E	R	Temperature Register.	The module temperature The value is available from 0x00 to 0xFF, which represents the temperature is from -128 to 127℃.	1	Byte
0x41	R	Frequency Control	The value is available from 0x00000000 to 0x0000 FFFF. 8E-12 typical frequency variation per step	4	U-Long
0x42	R	Status	The module's status information, refer to Status Details table for more information.	2	Char
0x50	R	Product Identification	Product identification information for trackingASCII format	64	Char
0x51	R	firmware revision	Module name, version revision, release date and special parameters. ASCII format	64	Char
0x52	R	Relative Time Interval Error	Time Interval Error in ns with an offset of +2000ns. Only available when system is locked and phase measurement is available. When there is no 1PPS measurement, system phase equivalent ageing is displayed. Ox0000 to Ox0FFF	2	U-Short
0xA0	W	DAC Register	Writing DAC value. Hex value from 0x00000000 to 0x000FFFF（16bits）.	4	U-Long
0xC2	W	Frequency control	Saves the value of the frequency control set with 0xA0 command. This value will be reloaded at start-up.	None	None
0x10	W	Disable PPS out	Permanently disable the 1PPS output	None	None

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0x11	W	Enable PPS out	Permanently enable the 1PPS output	None	None
0x12	W	Resync counter	Resets the internal counter of 1PPS. This produces a phase jump on the 1 PPS Output	None	None
0x13	W	Switch to internally locked mode	Slavery is performed by the system itself. System needs to be reset through 0xFA command after thiscommand has been sent.	None	None
0x14	W	Switch to DFC	Digital Frequency Control Mode is set. System needs to be reset through 0xFA command after thiscommand has been sent.	None	None
0xFA	W	Reset	System restarts in the last configured mode.	None	None
0x15	R	Timeout	The minimum guaranteed available holdover time. The unit is second.	4	U-Long
0x16	W	Set Timeout	Sets the minimum and maximum holdover acceptance window. The unit is ns.	2	Short
0x17	R	recovering speed	The recovering speed. The unit is ps.	2	U-Short
0x18	W	Set recovering speed	Set the recovering speed. The unit is ps.	2	U-Short

Table 11 Status Register Detail

Byte MSB							Byte LSB						
14	13	12	11	10	9	8	7	6	5	4	3	2 1	0
0	0	0	0	0	0	0	0	/P.Out	Syst.F	1	HV	Lock Status	1PPS

Bit	**R/W**	**Bit Name**	**Description**
0	R	1PPS	0: No PPS input 1: there is a valid PPS input
2:1	R	Lock Status	00: power on mode or free run mode 01: 30s to 30mn since system started – Stabilization (Acquiring mode) 10: System ready for use (Locked mode)
3	R	HV	1: Holdover Mode, no PPS detected. 0: not in Holdover mode, PPS detected
4	R	1	Must be 1 for normal operation.
5	R	Syst.F	System Fail check. If 1PPS has been provided.
6	R	/P.Out	0: PPS ready and available on 1PPS out pin. 1: PPS not ready and not available on 1PPS out Pin.
7	R	0	Must be 0 for normal operation.

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8.2 UART Interface (Only for CM35B-C118-10.00MHz-B)

UART interfacesare used for management and TOD, which has a fixed baud rate (115200) using 1 stop bit and no parity. It is a LVTTL-compatible port and needs an external translator to work with other signal types (such as RS-232C or RS-485). All parameters defined in I2C register table could also be implementedviaUART interface.

Management mode

In management mode, system could get the status of CM35B and control CM35B.

Example:

$PDP,00,0,F,Q,-3095,32768.0000,32768.0000,000,000,00000.0000,00000.0000,00000.0000,00000.0000,3-23,+000.0000,-0000,www.dptel.com,1.1,2011-05-16*55

Notes:

In the Format column, c stand for char,d stand for digit, s stand for sign.

Table 12 UART Management Message

Field No.	Name	Format	Description	Length (byte)
0	$PDP	$ccc	Message ID, DAPU Telecom Technology protocol header	4
1	No	dd	Message No.	2
2	TxRxFlag	d	The transmit and receive flag.(0: upper computer transmit; 1: upper computer receive)	1
3	CStatus	c	Current status.(F: 3 mins warm-up; L: Lock; H: Hold over)	1
4	TrackStatus	d	Track status (Q: fast track;1: slow track;S: slow track over 1 hour;S: track over 48 hours)	1
5	cPHDiff	sdddd	Current phase difference	5
6	cPWM1	ddddd.dddd	Current PWM1 (Voltage-controlled value1)	10
7	cPWM2	ddddd.dddd	Current PWM2 (Voltage-controlled value2)	10
8	SYNCNT	ddd	The synchronous times	3
9	HCNT	ddd	Hours after enter slow track	3
10	HPAVG	ddddd.dddd	The average of the PWM in the last 1 hour	10
11	VCH1	ddddd.dddd	Voltage-controlled compensation value every 1 hour	10
12	HPMOD	ddddd.dddd	The Module DAC Value	
13	VCM10	ddddd.dddd	Voltage-controlled compensation value every 10 minutes	10
14	POS	d-dd	The position of the product.(Layer-No), just for the inner test.	4
15	inT	sddd.dddd	NA	9
16	TcPHDiff	sdddd	The product current phase difference	5
17	Website		www.dptel.com	13
18	Version	d.d	version	3

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19	Date	dddd-dd-dd	Date	10
20		dd	35	2
21	END		<CR><LF>	2

Time of Day

A TOD message format can be a GPRMC message or one of a group of other GPS messages or proprietary messages to suit specific causes. Such as a GPRMC message has the format $GPRMC,122356,A,0000.0000,N,00000.0000,W,0.0.0.0,120508,,,A*F6 in which the commas are separators.The message is 62 characters in length (i.e. 62 bytes). No parity bit is used, but each byte has a stop bit. The architecture of the message is shown in Table 4.

Table 13 Architecture of GPRMC message

Elements	Description
$GPRMC	Message header.
122356	UTC value.
A	Status (A = active, V = void).
0000.0000,N	Latitude, north (fixed to zero).
00000.0000,W	Longitude, west (fixed to zero).
0.0	Speed over ground (fixed to zero).
0.0	Track angle (fixed to zero).
120508	Date (ddmmyy).
A	A = autonomous, D = differential, E = estimated, S = simulation, N = not valid.
*F6	Checksum.

9. Control and Status Pins (Optional)

CM35B is a clock module which synchronizes the local clock to reference such as 1 PPS retrieving from GNSS. CM35B will work normally performing synchronizing algorithm when the SYNC_CTRL pin is driven high. It also could be forced to work in free-run or holdover status when the SYNC_CTRL pin is driven low.

The LOCKED pin indicates the lock status of CM35B. High level indicates the module is locked to external 1PPS reference. When the module never is locked to reference after power up, the status of module is free-run, the LOCKED pin outputs low. When the reference is lost, the status of module is holdover, the LOCKED pin also output low.

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10. Environmental Conditions

Table 14Environmental Conditions

Parameter	Conditions	
Operating Temperature	-40℃ to 85℃	
Operable Temperature	-45℃ to 90℃	
Storage Temperature	-55℃ to 105℃	
Storage Humidity	30%~80%	
ESD Level	Human Body Model, class2: 2000V to 4000V; ANSI/ESDA/JEDEC JS-001-2010.	
	Machine Model, class B: 200V to 400V; ANSI/ESDA/JEDEC JS-001-2010.	
Moisture Sensitivity Level	Not humidity sensitive.	
Vibration	Test Condition: 0.75mm ;acceleration:10g;10Hz～500Hz, one cycle per 30 min, test 2 hour. (3 times for each 3 directions X ,Y , Z), IEC 68-2-06 Test Fc.	
Shock	50g; 11ms; half sine wave (3 times for each 3 directions X,Y, Z),IEC 68-2-27 Test Ea/Severity 50A.	
Relative Humidity	20%～70%	Full Package Storage
Temperature	-10℃~35℃	

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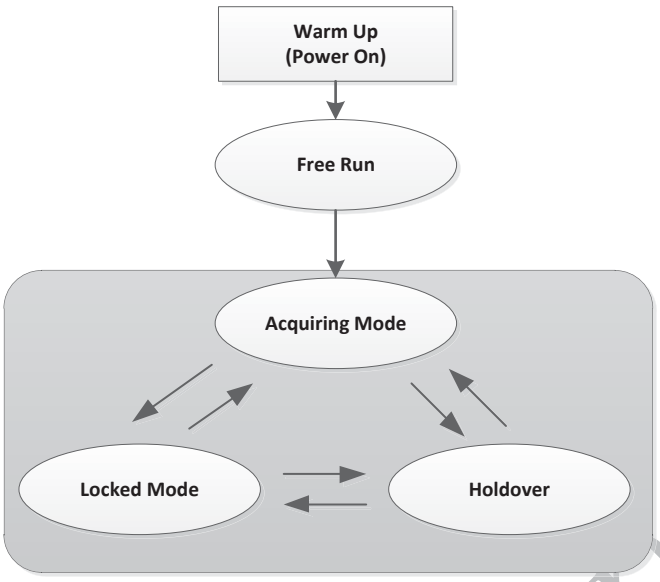
11. Workflow Diagram



Warm Up

The stage is decided by the characteristics of OCXO. It could occur after long powered-off time (shipment, storage,installation process, etc.). Due to frequency recovery phenomenon, the device must be re-stabilized over continuous time ofoperation before reaching its overall intrinsic performances.

Power consumption will stabilize after a few of minutes after powering-on at +25°C; that stabilization isdependent onambient temperature at start (up to 5 minutes maximum at -40°C).Ageing slope will reach its final performance after recover time.

Free Run

Clock module powers on without 1PPS reference anyway, and featured stand-alone OCXO delivering its intrinsic performances, except ageing slope (as it depends on the recoveryphenomenon).

System is preparing for the data acquisition stage. No 1PPS output.

Acquiring Mode

When 1PPS input is available, start to adjust the OCXO 10MHz output frequency, and quickly to track the 1PPS of 10MHz with 1PPS reference.

When acquisition process is successful (30min. total time minimum):

- frequency accuracy is guaranteed within less than 1ppb;
- phase is aligned to the 1pps input signal.

Locked mode

Take advantage of algorithm to optimize the loop performance and get the best of GNSS stability and the performance of OCXO. At the same time, learn the ageing information. During this mode, the phase and frequency are locked and guaranteed.

After 2 hours of continuous operation, phase accuracy is less than ±30ns.

Hold Over

During locked mode, an algorithm has been developed which enables adaptive modeling of the frequency stability of an OCXO with reference from GNSS. When GNSS signal missed, the algorithm would guarantee the frequency and phase stability over operating temperature.

After initial warm-up, system requires 5 days of power-on for meeting specified holdover stability.48 hours locked after 5 days of power on should be guaranteed so that hold over capability can reach 1.5us over 24 hours.

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12. Typical Application

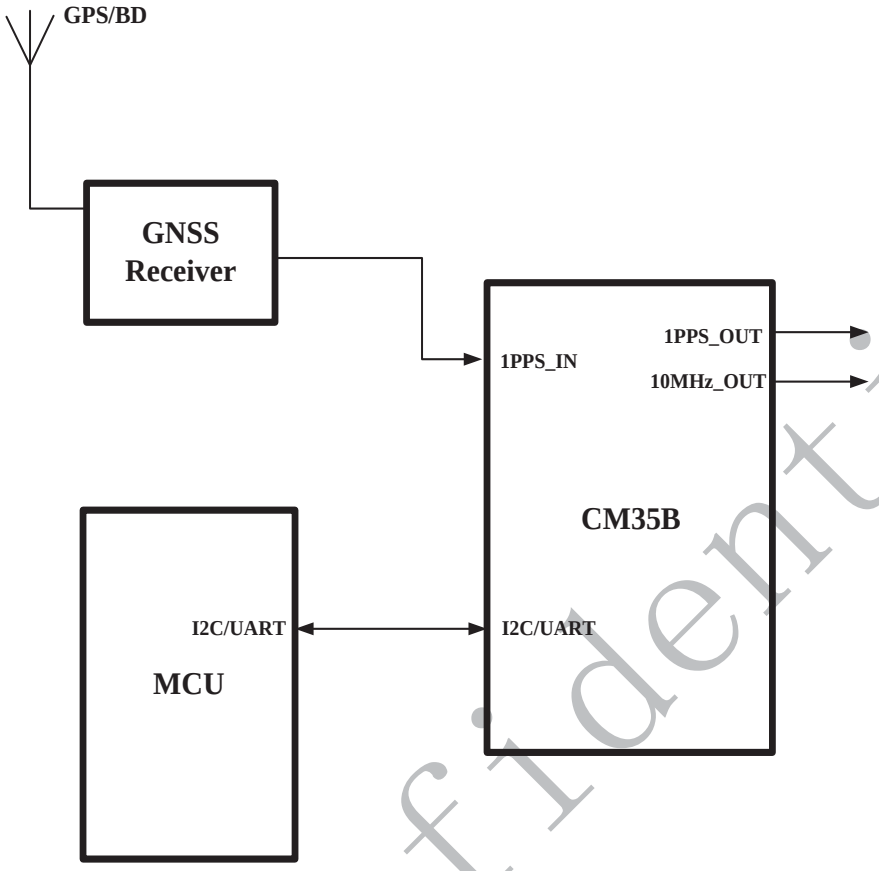

Figure 2Typical application

GNSS Receiveroffers 1PPS signal to CM35B.

The MCU manages and monitors the work state of CM35B.

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13. Mechanical Structure (mm)

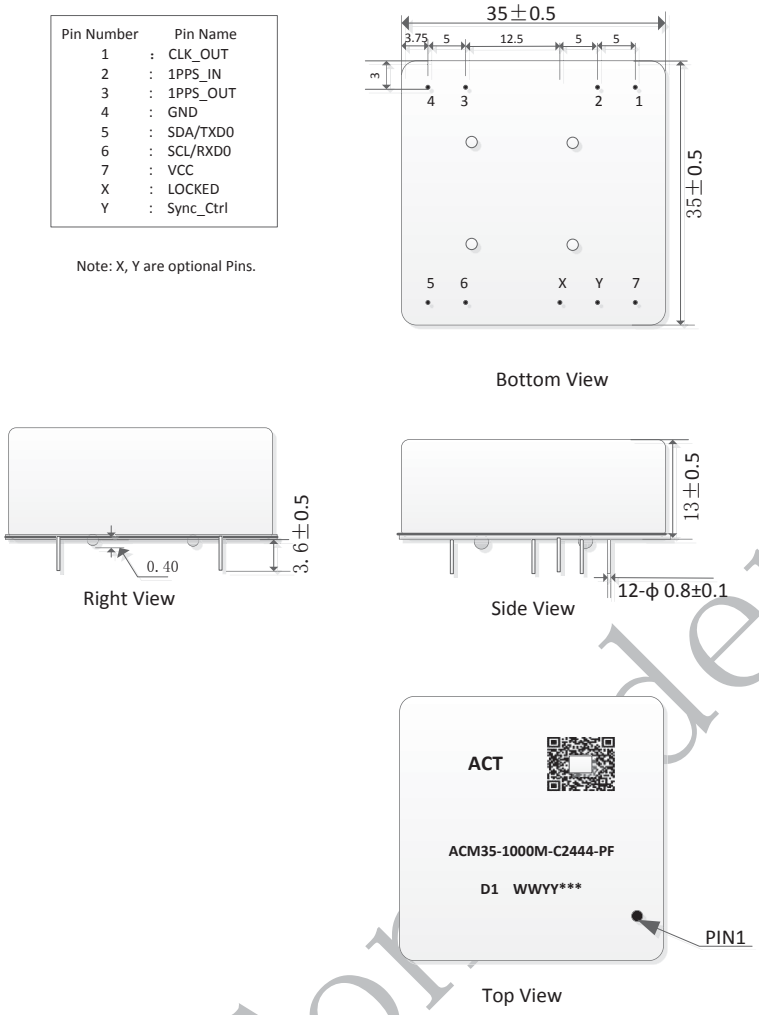

Figure 3 Mechanical structure

Note1: Tolerance ± 0.3mm without mark.

Note2: WWrepresentative:week.

YY representative: year.

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14. Wave Soldering Curve(RoHS)

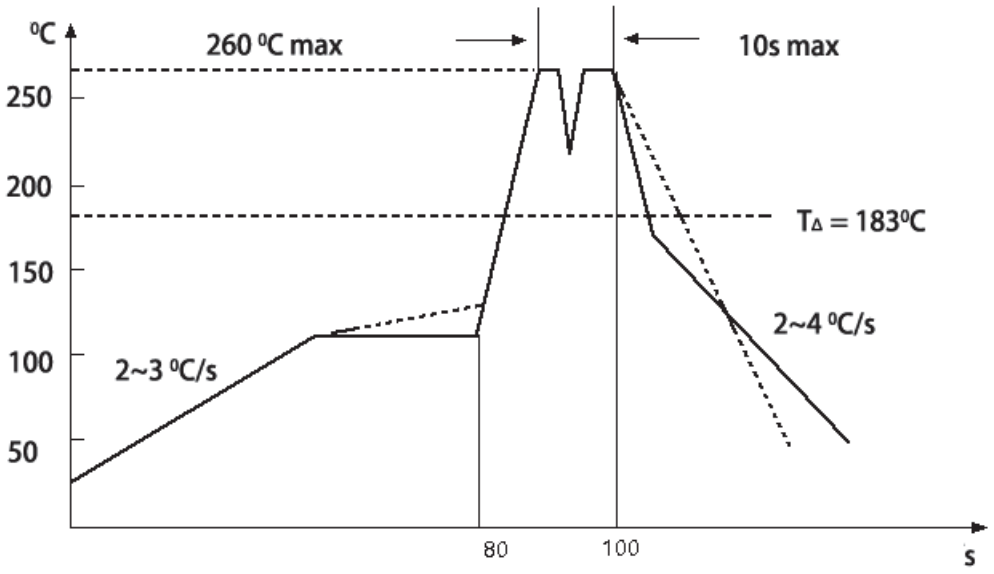
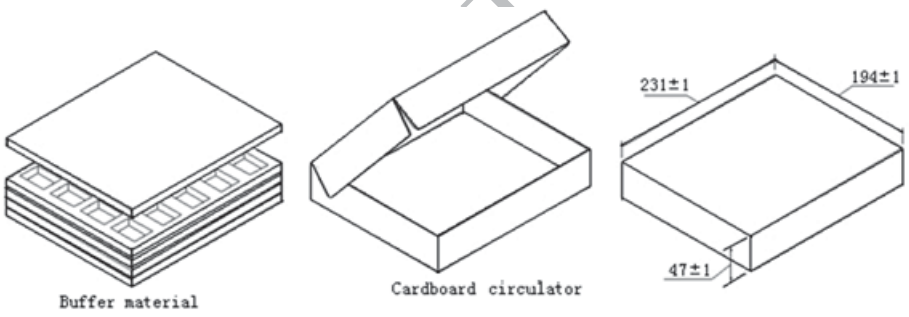


Figure 4 Wave soldering curve

15. Package（mm）



Note: Max 12pcs in each box.

Figure 5 Package