To Customer：_____

DPXA05 Datasheet

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Ordering Information

Manufacture Part Number	Product Name	Description
DPXA05D	DPXA05	

Guangdong Dapu Telecom Technology Co., Ltd

Bldg 5, SSL Modern Enterprise Accelerator Zone, Dongguan City, Guangdong Province, PRC China

TEL:0086-0769-88010888 FAX:0086-0769-81800098

Index

1 OVERVIEW 3

2 KEY FEATURES 3

3 PAD INFORMATION 4

4 PAD DEFINITION 5

5 ELECTRICAL CHARACTERISTICS 7

5.1 ABSOLUTE MAXIMUM RATINGS 7

5.2 RECOMMENDED OPERATING CONDITIONS 7

5.3 DC CHARACTERISTICS 8

5.4 AC CHARACTERISTICS 10

6 REGISTERS 11

6.1 REGISTER LISTS 11

6.1.1 Details of Normal Registers (0x10~0x3C) 12

6.1.2 Details of Debug Registers (0x40~0x57) 17

7 EFUSE OPERATION 19

7.1 EFUSE WRITE: VDD SHOULD SET TO 5.5V. 19

7.2 EFUSE READ: 19

7.3 EFUSE WRITE ADDRESS CALCULATION: 19

7.4 EFUSE READ ADDRESS CALCULATION: 20

8 I²C BUS INTERFACE 21

8.1 CAUTIONS 21

8.2 SLAVE ADDRESS 21

8.3 I²C BUS PROTOCOL 21

8.3.1 Write process 21

8.3.2 Read process 22

9 REVISION HISTORY 23

1 Overview

DPXA05 is an I²C/SPI bus interface real-time clock with low power consumption. It support backup battery and embeds a 32.768KHz TCXO. It supports calendar (year, month, day, hour, minute, second), clock, timer and digital offset functions etc.

2 Key Features

Operation voltage: 1.6V~5.5V

Timekeeper Voltage: 1.6V~5.5V

Operation temperature range: -45℃~90℃

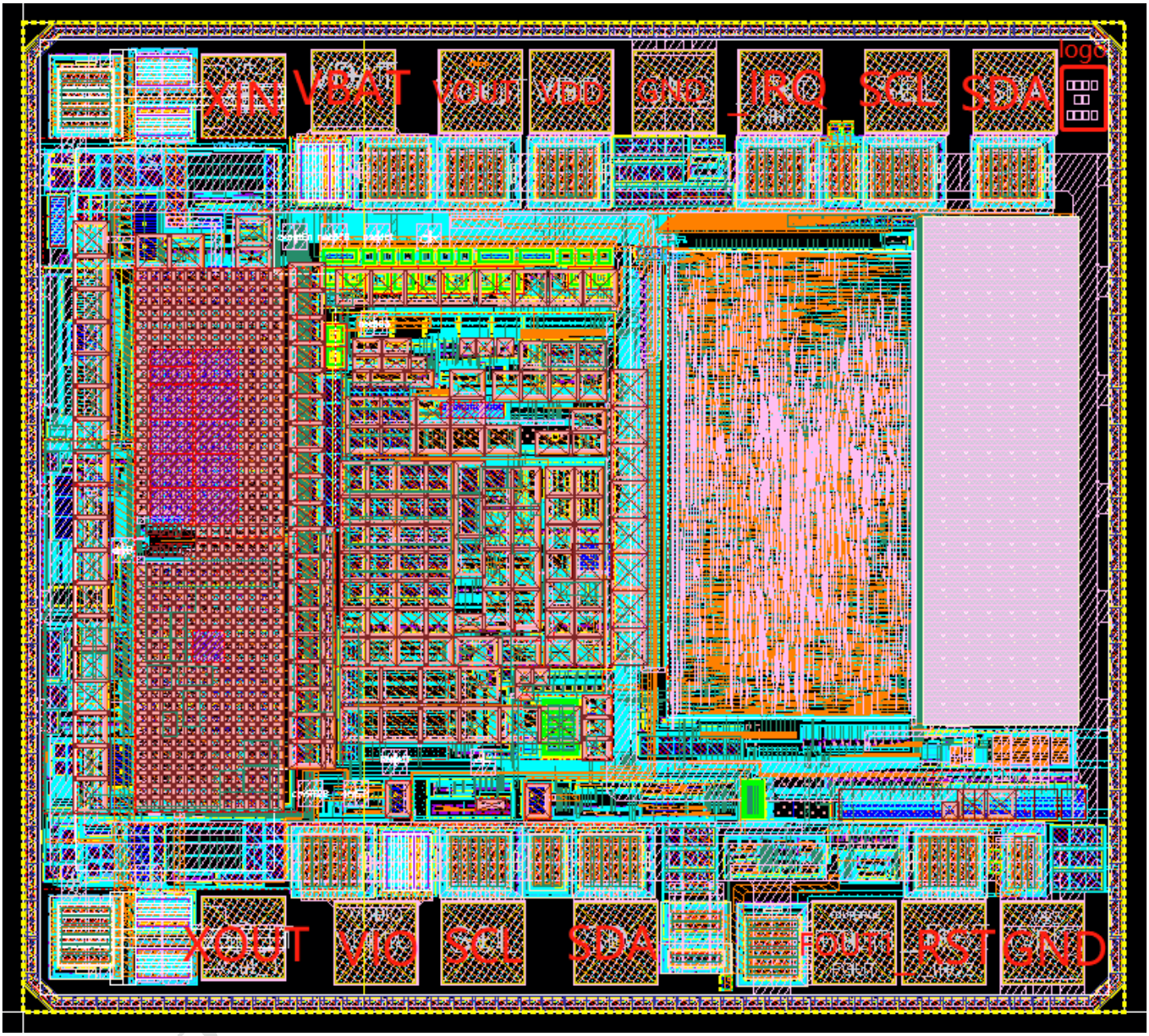
Crystal frequency: 32768Hz

Crystal load capacity: 12.5pF

Crystal max ESR: <90KΩ

400Khz I2C interface

3 PAD information



PAD	x:890	y:800
scribe line	60um	
pad open size	65um*65um	
Top line / unit: um		
XIN	177.930	739.610
VBAT	266.730	744.000
VOUT	369.963	744.000
VDD	442.970	744.000
GND	526.370	744.000
_IRQ	611.902	744.000
SCL	714.225	744.000

SDA	801.355	744.000
Bottom line / unit: um		
XOUT	177.930	60.390
VIO	284.985	56.000
SCL	371.967	56.185
SDA	478.968	56.185
FOUT1	671.375	56.000
_RST	744.056	56.000
GND	824.000	56.000

4 PAD definition

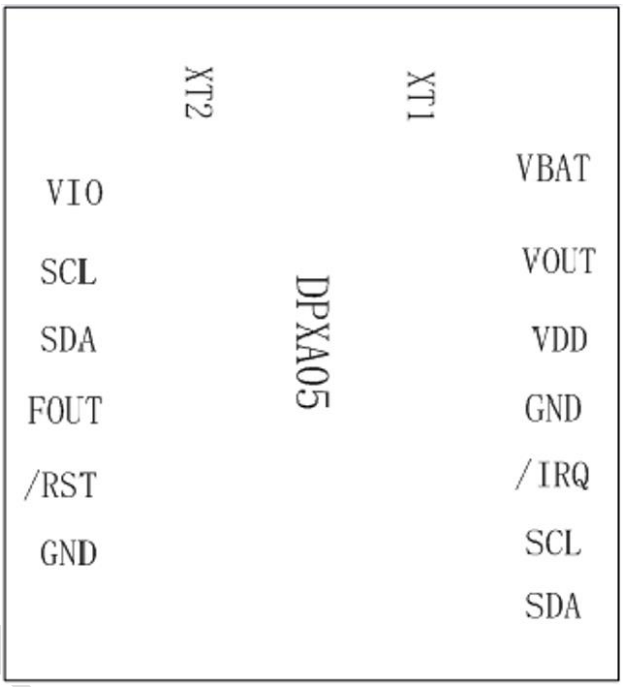


Table1. Pin Definition

Pin Number	Pin Name	I/O	Description
1	XT2	Out	Crystal output pin
2	XT1	In	Crystal input pin
3	VIO	-	Interface power supply
4	SCL	In	I^2C clock signal
5	SDA	In/Out	I^2C data signal
6	FOUT	Out	Frequency output.
7	/RST	Out	Generate a /RST signal for VDD drop or release /RST signal for VDD rise. (Open Drain)
8	GND	-	Ground
9	/IRQ	Out	Interrupt output by alarm or Timer events. (Open Drain)
10	VDD	-	Power supply VDD

Pin Number	Pin Name	I/O	Description
11	VOUT	-	Internal power supply pin, connect smoothing capacity of 1.0uF
12	VBAT	-	Power supply VBAT. Backup battery pin.

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table2. Absolute Maximum Ratings

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage	V_{DD}	-0.3		6.5	V	
	V_{BAT}	-0.3		6.5	V	
	V_{OUT}	-0.3		6.5	V	
	V_{IO}	-0.3		6.5	V	
Input Voltage	V_{IN}	GND-0.3		6.5	V	SCL, SDA
Clock Output Voltage	V_{OUT1}	GND-0.3		V_{DD}+0.3	V	FOUT
Output Voltage	V_{OUT2}	GND-0.3		6.5	V	SDA, /IRQ
Storage temperature	T_{STG}	-55		125	℃	

5.2 Recommended Operating Conditions

Table3. Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage	V_{DD}	1.2	3.0	5.5	V	
	V_{BAT}	1.2	3.0	5.5	V	
	V_{IO}	1.6	3.0	5.5	V	
EFUSE Write Voltage	V_{WR}		5.5		V	For VDD pin
Operation temperature	T_{OPR}	-40	25	85	℃	

5.3 DC Characteristics

Table4. DC Characteristics

Item	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Average Current consumption1	IDD1		0.9	5.6	uA	SCL=SDA = 'H', FOUT=OFF, /INT=OFF, VDD=VIO=3.0V,CHGEN=0b or VBAT≧VDET3, -40℃~85℃
Average Current consumption 2	IDD2		3.4	7.8	uA	SCL=SDA = 'H', FOUT=32.768kHz (FOUT pin CL=15pF), /INT=OFF,VDD=VIO=3.0V, CHGEN=0b or VBAT≧VDET3,-40℃~85℃
Average Current consumption 3	IDD3		1.0	5.0	uA	SCL, SDA = 'L', VBAT=3.0V, VDD=VIO=0V, -40℃~+85℃
Detector Threshold voltage1 （VDD rising edge）	+VDET11	2.25	2.6	2.95	V	/RST releases setting:2.6 V
Detector Threshold voltage1 （VDD falling edge）	-VDET11	2.20	2.55	2.90	V	/RST output setting:2.6 V
Detector Threshold voltage2 （VDD rising edge）	+VDET12	2.20	2.55	2.90	V	/RST releases setting:2.55V
Detector Threshold voltage2 （VDD falling edge）	-VDET12	2.15	2.5	2.85	V	/RST output setting:2.55 V
Detector Threshold voltage3 （VDD rising edge）	+VDET2	1.22	1.46	1.7	V	Exchange voltage：VBAT to VDD
Detector Threshold voltage3 （VDD falling edge）	-VDET2	1.2	1.44	1.68	V	Exchange voltage：VDD to VBAT
Detector Threshold voltage4 （VBAT rising edge）	+VDET31	2.77	2.97	3.17	V	Stop charging voltage (full charge) BFVSEL=00b
Detector Threshold voltage4 （VBAT falling	-VDET31	2.68	2.90	3.12	V	Recharge voltage. BFVSEL=00b

Item	Symbol	Value			Unit	Notes	
		Min.	Typ.	Max.			
edge）							
Detector Threshold voltage5 （VBAT rising edge）	+VDET30	2.7	2.88	3.1	V	Stop charging voltage (full charge) BFVSEL=10b	
Detector Threshold voltage5 （VBAT falling edge）	-VDET30	2.65	2.8	3.00	V	Recharge voltage. BFVSEL=10b	
Detector Threshold voltage6 （VBAT rising edge）	+VDET32	2.82	3.05	3.28	V	Stop charging voltage (full charge) BFVSEL=01b	
Detector Threshold voltage6 （VBAT falling edge）	-VDET32	2.72	2.95	3.2	V	Recharge voltage. BFVSEL=01b	
VBAT off voltage	-VDET4	2.1	2.3	2.6	V	Low VBAT detection VBLF = 1b	
VDD-VOUT Off-leak current	ISW1			15	nA	VDD=0V，VOUT=3.0V	
VDD-VOUT Off-leak current	ISW2			15	nA	VOUT=0V，VBAT=3.0V	
VOUT output voltage1	VOUT1		VDD-0.06V		V	VDD=3V，IOUT=1mA	
VOUT output voltage2	VOUT2		VBAT-0.02V		V	VBAT=3.0V，IOUT=0.1mA	
Input voltage	VIH	0.8*VIO		5.5	V	SCL， SDA	
Input voltage	VIL	GND-0.3		0.2*VIO	V		
Output voltage	VOH	VIO-0.5		VIO	V	IOH = -1mA	FOUT 脚
Output voltage Low-level	VOL1	GND		GND+0.5	V	IOL = 1mA	FOUT 脚
	VOL2	GND		GND+0.25	V	VIO=5.0V, IOL=1mA	/RST, /INT
	VOL3	GND		GND+0.4	V	VIO=3.0V, IOL=1mA	
	VOL4	GND		GND+0.4	V	VIO≥2.0V, IOL=3mA	SDA

5.4 AC Characteristics

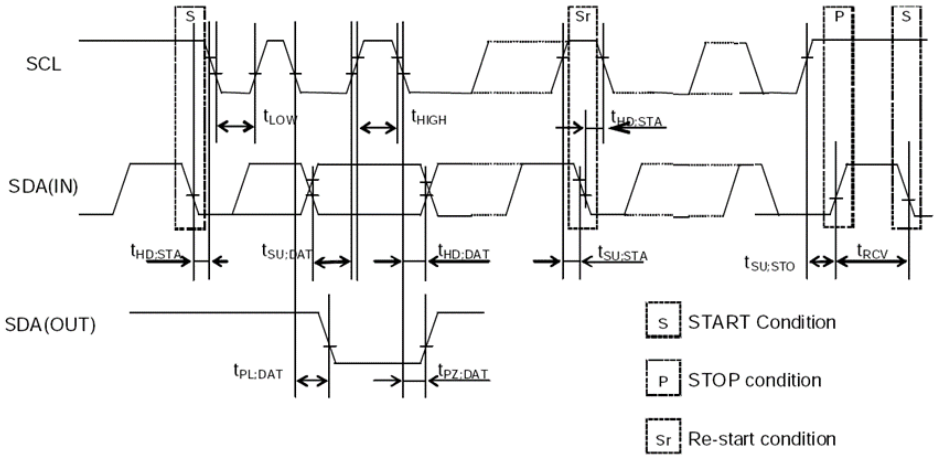


Figure1. I2C bus Timing Chart

Table5. AC Characteristics

V_{DD}=1.6V ~ 5.5V; Ta=-40℃ ~ +125℃

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}			400	kHz
SCL low level time	t_{LOW}	1.3			us
SCL high level time	t_{HIGH}	0.6			us
Start condition setup time	$t_{HD;STA}$	0.6			us
Start condition hold time	$t_{SU;STA}$	0.6			us
Stop condition setup time	$t_{SU;STO}$	0.6			us
Bus idle time between start condition and stop condition	t_{RCV}	1.3			us
Data setup time	$t_{SU;DAT}$	100			ns
Data hold time	$t_{HD;DAT}$	0			ns
SCL, SDA rising time	t_r			0.3	us
SCL, SDA falling time	t_f			0.3	us

Note: when the master accesses the equipment through I2C bus, all communication from sending start condition to sending stop shall be completed within 1 second. If it exceeds 1 second, the I2C bus interface will be reset through the internal bus timeout function.

6 Registers

6.1 Register Lists

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x10	SEC	○	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				R/W
0x11	MIN	○	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R/W
0x12	HOUR	○	○	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0x13	WEEK	○	6	5	4	3	2	1	0	R/W
0x14	DAY	○	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x15	MONTH	○	○	○	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				R/W
0x16	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				R/W
0x17	MIN Alarm	AE	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R
0x18	HOUR Alarm	AE	•	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0x19	WEEK Alarm	AE	6	5	4	3	2	1	0	R/W
	DAY Alarm		•	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x1A	Timer Counter 0	128	64	32	16	8	4	2	1	R/W
0x1B	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256	R/W
0x1C	Extension Register	FSEL[1]	FSEL[0]	USEL	TE	WADA	TSEL[2]	TSEL[1]	TSEL[0]	R/W
0x1D	Flag Register	VBLF	○	UF	TF	AF	RSF	VLF	VBFF	R/W
0x1E	Control Register	○	STOP	UIE	TIE	AIE	TSTP	TBKON	TBKE	R/W
0x1F	Control Register	SMP TSEL[1]	SMP TSEL[0]	CHGEN	INIEN	○	RSVSEL	BF VSEL[1]	BF VSEL[0]	R/W
0x20 | 0x23	RAM	•	•	•	•	•	•	•	•	R/W
0x30	Digital offset	DTE	L7	L6	L5	L4	L3	L2	L1	R/W

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x31	VBLFE	○	○	○	○	○	○	○	VBLFE	R/W

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x3C	ID	RTC_ID=8'hD4								R

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x40	Debug	debug mode								W/R
0x41	Efuse_Ctrl1	efuse_vpp_pwr_on	○	○	○	reg_rden	reg_pgmen	reg_efuse_iso_en	reg_efuse_pwr_on	W/R
0x42	Efuse_Addr	○	○	reg_addr_6bit[5:0]						W/R
0x44	Efuse_Data	efuse_dout[7:0]								W/R
0x45	Efuse_Rst	efuse_written_flag	○	○	○	○	efuse_reset	○	analog_test	W/R
0x46	Efuse_Wren	○	○	○	○	○	○	○	efuse_wren1	W/R
0x47	Efuse_Wren	○	○	○	○	○	○	○	efuse_wren2	W/R
0x50	ana_control0	○	○	○	○	○	○	○	Efuse_Load	W/R
0x51	ana_control1	CapAdj<7:0>								W/R
0x52	ana_control2	CapAdj<10:8>			○		○			W/R

6.1.1 Details of Normal Registers (0x10~0x3C)

0x00~0x06

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x10	SEC	○	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				0x00
0x11	MIN	○	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x00
0x12	HOUR	○	○	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				0x00
0x13	WEEK	○	6	5	4	3	2	1	0	0x40
0x14	DAY	○	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				0x01
0x15	MONTH	○	○	○	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				0x01
0x16	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				0x00

SEC: BCD format, Value: 0~59

MIN: BCD format, Value: 0~59

HOUR: BCD format, Value: 0~23

WEEK: Value 01h, 02h, 04h, 08h, 10h, 20h, 40h. Only one bit can be set to 1 each time, all others must be set to 0.

Table6. WEEK Register

WEEK	Data	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sunday	01h	0	0	0	0	0	0	0	1
Monday	02h	0	0	0	0	0	0	1	0
Tuesday	04h	0	0	0	0	0	1	0	0
Wednesday	08h	0	0	0	0	1	0	0	0
Thursday	10h	0	0	0	1	0	0	0	0
Friday	20h	0	0	1	0	0	0	0	0
Saturday	40h	0	1	0	0	0	0	0	0

DAY: BCD format, the value range will be adjusted automatically according to the month setting and if a leap year or not.

Table7. DAY Register Value

Month	Day Value Range
1, 3, 5, 7, 8, 10, 12	1~31
4, 6, 9, 11	1~30
February in normal year	1~28
February in leap year	1~29

MONTH: BCD format, Value1~12

YEAR: BCD format, Value0~99(2000~2099)

Example: 2020/01/01 Wednesday 21:18:36

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x00	SEC	○	0	1	1	0	1	1	0
0x01	MIN	○	0	0	1	1	0	0	0
0x02	HOUR	○	○	1	0	0	0	0	1
0x03	WEEK	○	0	0	0	1	0	0	0
0x04	DAY	○	○	0	0	0	0	0	1
0x05	MONTH	○	○	○	0	0	0	0	1
0x06	YEAR	0	0	1	0	0	0	0	0

0x17~0x19

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x17	MIN Alarm	**AE**	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x00
0x18	HOUR Alarm	**AE**	●	BCD code, Hour tens place, 0-2		BCD code, Minute ones place, 0-9				0x00
0x19	WEEK Alarm	**AE**	6	5	4	3	2	1	0	0x00
	DAY Alarm		●	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				

AE: Alarm Enable bit, 0-enable; 1-disenable.

WEEK Alarm/DAY Alarm: Controlled by WADA bit in 0x0D register.

According to AIE, AF, WADA bits setting, the alarm interrupt will be generated once the current time match

the settings in the above registers, the /INT pin goes to low level and AF bit is set to '1' to record an alarm interrupt event has occurred.

0x1A-0x1B

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x1A	Timer Counter0	TimerCountr<7:0>								0x00
0x1B	Timer Counter1	TimerCountr<15:8>								0x00

Presetting timer counter value <15:0>.

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x1C	Extension Register	FSEL[1]	FSEL[0]	USEL	TE	WADA	TSEL[2]	TSEL[1]	TSEL[0]	0x00
0x1D	Flag Register	VBLF	○	UF	TF	AF	RSF	VLF	VBFF	0x03
0x1E	Control Register	TEST	STOP	UIE	TIE	AIE	TSTP	TBKON	TBKE	0x00
0x1F	Control Register	SMP TSEL[1]	SMP TSEL[0]	CHGEN	INIEN	○	RSVSEL	BF VSEL[1]	BF VSEL[0]	0x00

FSEL[1:0]: Fout out frequency config

FSEL[1:0]	Fout frequency select
00	32768Hz
01	1024Hz
10	1Hz
11	OFF

USEL: Update interrupt select, this function is enabled by default and can't close;

0: sec update interrupt

1: min update interrupt

TE: Timer enable control

0: timer function is disable

1: timer function is enable

WADA: select 0x19 register function

0: 0x19 register is use for week alarm

1: 0x19 register is use for day alarm

TSEL[2:0]: Timer counter source clock select

TSEL[1:0]	Fout frequency select	Interrupt Self-Cleaning Cycle (tRTN)
000	4096Hz	8192Hz
010	64Hz	128Hz
010	1Hz	128Hz
011	1Min	128Hz
100	1Hour	128Hz

VBLF: VBAT Low Flag
0: VBAT Voltage not low.
1: Low VBAT Voltage is detected, keep 1 until software to write 0.
UF: time update interrupt flag
0: time update interrupt is not occurred
1: time update interrupt is occurred, keep 1 until software to write 0
TF: timer interrupt flag
0: timer interrupt is not occurred
1: timer interrupt is occurred, keep 1 until software to write 0
AF: alarm interrupt flag
0: alarm interrupt is not occurred
1: alarm interrupt is occurred, keep 1 until software to write 0
RSF: Flag for RST signal generation.
0: RST signal is not generation.
1: RST signal is generation, keep 1 until software to write 0.
VLF: voltage low detection flag
0: VDD voltage low is not detected
1: VDD voltage low is detected, keep 1 until software to write 0
VBFF: VBAT voltage full detection flag
0: VBAT voltage is not full.
1: VBAT voltage is full. Auto clear to 0 when VBAT is not full.
TEST:

STOP: Stop time
0: Not stop time.
1: Stop time from 1024Hz to year counter.
UIE: control time update interrupt output to /IRQ
0: time update interrupt not output to /IRQ
1: time update interrupt output to /IRQ
TIE: control timer interrupt output to / IRQ
0: timer interrupt not output to / IRQ
1: timer interrupt output to / IRQ
AIE: alarm interrupt control
0: alarm interrupt not output to / IRQ
1: alarm interrupt output to / IRQ
TSTP: Stop timer.
0: Resume timer count.
1: Stop timer count.
TBKON: Control timer work on normal mode or backup mode when TBKE=1
0: Timer only work on backup mode.
1: Timer only work on normal mode.
TBKE:
0: Timer can work on normal and backup mode.
1: Timer work mode controlled by TBKON.
SMPTSEL[1:0]: VDD detection period.

0: 2ms
1: 16ms
2: 128ms
3: 256ms

CHGEN: Enable charge mode.
0: Exit VBAT charge mode.
1: Enter VBAT charge mode.

INIEN: IO Control on RST mode.
0: IO is enable when RST signal generation.
1: IO is disable when RST signal generation.

RSVSEL: RST voltage selection.
0: 2.6V
1: 2.55V

BFVSEL[1:0]: Threshold voltage of VBAT full detection.
00: 3.02V
01: 3.08V
10: 2.92V
11: OFF(no limit)

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x30	Digital offset	DTE	L7	L6	L5	L4	L3	L2	L1	0x00

DTE (Digital offset function Enable): Enables the digital offset adjustment function. If DET is “1”, digital offset adjustment is enabled. DET is “0” to turn off digital offset adjustment; After the digital offset function is enabled, the digital offset register adjusts the sub-second clock according to the value set in the digital offset register. The calibration of the "seconds" register takes place every 10 seconds and the amount of offset set determines the intensity of the calibration. This feature does not affect the 32.768 kHz signal output on the FOUT pin because it does not change the oscillation frequency of the built-in crystal. In the case of 1Hz or 1024Hz signal output on FOUT, the offset correction will cause some jitter on the clock signal. The alarm function and wake timer function (if a source clock less than 4096 Hz is selected) are affected by this function The following table shows the corresponding offset value from L7 to L1. When L7 bit is “0”, the offset value is positive (the clock runs faster) and when L7 bit is “1” the offset value is negative (the clock runs slower)：

Table8. **Digital offset registers**

L7	L6	L5	L4	L3	L2	L1	Offset Value (ppm)
0	1	1	1	1	1	1	+192.26
0	1	1	1	1	1	0	+189.21
…	……						…
0	0	0	0	0	1	0	+6.1
0	0	0	0	0	0	1	+3.05
0	0	0	0	0	0	0	±0
1	1	1	1	1	1	1	-3.05
1	1	1	1	1	1	0	-6.1
…	……						…
1	0	0	0	0	0	1	-192.26

L7	L6	L5	L4	L3	L2	L1	Offset Value (ppm)
1	0	0	0	0	0	0	-195.31

Digital offset calculation method is as follows.

When the offset value is positive, L [7:1] = [Offset Value]/3.05, decimals are discarded.

When the offset value is negative, L [7:1] = 128- [Offset Value]/3.05, decimals are discarded.

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x31	Extension Register1	○	○	○	○	○	○	○	VBLFE	0x00

VBLFE (VBAT Low Flag Enable) : enables the battery Low voltage detection function；

Table9. **VBLFE Settings**

Operation	VBLFE	Describe
Write	0	CHGEN:0 VBLF detection not enable CHGEN:1 VBLF detection enable (during normal mode re-chargeable battery charging)
	1	VBLF detection enable during VDD supply

If you want to use VBLF detection, the INIEN should be set to 1 in addition to VBLFE bit setting. In VDD drive mode VBAT low voltage (non-rechargeable, rechargeable battery) can be detected. VBLF function is not available in case of backup mode.

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	default
0x3C	ID	RTC_ID=8'hD4								0x00

RTC_ID: RTC_ID = 0xD4

6.1.2 Details of Debug Registers (0x40~0x57)

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	default
0x40	Debug	debug mode								0x00
0x41	Efuse_Ctrl1	efuse_vpp_pwr_on	○	○	○	reg_rden	reg_pgmen	reg_efuse_iso_en	reg_efuse_pwr_on	0x02
0x42	Efuse_Addr	○	○	reg_addr_6bit[5:0]						0x00
0x44	Efuse_Data	efuse_dout[7:0]								0x00
0x45	Efuse_Rst	efuse_written_flag	○	○	○	○	efuse_reset	○	analog_test	0x00
0x46	Efuse_Wren	○	○	○	○	○	○	○	efuse_wren1	0x00

0x47	Efuse_Wren	○	○	○	○	○	○	○	efuse_wren2	0x00

DEBUG: enter debug mode to assess the register from 0x40 to 0x57.

Write 0x40=0xa1,0xb2,0xc3 to enter debug mode. Write 0x40 = 0x00 to exit debug mode.

EFUSE_VPP_PWR_ON: EFUSE AVDD switch.

0: switch is open

1: switch is close

REG_RDEN:

0: disable read efuse data

1: enable read efuse data

REG_PGMEN:

0: disable efuse program

1: enable efuse program

REG_EFUSE_ISO_EN:

0: disable isolation for efuse data

1: enable isolation for efuse data

REF_EFUSE_PWR_ON:

0: efuse DVDD switch is open

1: efuse DVDD switch is close

EFUSE_ADDR_6BIT: Efuse address config.

EFUSE_DOUT: Efuse data output register.

EFUSE_WRITTEN_FLAG: Efuse program flag.

EFUSE_RESET:

0: not reset efuse

1: reset effuse

ANALOG_TEST:

0: Normal mode

1: Enter analog test mode

EFUSE_WREN1 / 2: Write 0x46=0x01,0x47=0x00 to generate a signal to trig efuse read or write.

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x50	ana_control0	○			○			○	EFUSE_LOAD	0x84
0x51	ana_control1	CapAdj<7:0>								0x00
0x52	ana_control2	CapAdj<10:8>			○		○			0x0C

EFUSE_LOAD:

0: Efuse value will not load to register 0x50~0x57

1: Efuse value will load to register 0x50~0x57

CAPADJ[10:0]: Adjust Fout frequency.

7 EFUSE operation

7.1 Efuse write: VDD should set to 5.5V.

① Enter debug mode

② 0x41=0x09，power on DVDD，set RDEN to high

③ 0x41=0x01，dry RDEN to low

④ 0x41=0x81，power on AVDD

⑤ 0x41=0x85，set PGMEN to high，efuse enter program mode

⑥ 0x42 [5:0] write addr.

⑦ 0x46=0x01 ，0x47=0x00，to trig effuse enable written.

Repeat step⑥⑦, until program is done.

⑧ 0x41=0x81

⑨ 0x41=0x03

⑩ 0x41=0x02 to exit effuse.

7.2 Efuse read:

① Enter debug mode

② 0x41=0x01，power on DVDD.

③ 0x41=0x09，set RDEN high

④ 0x42 [2:0] write the address you should read out.

⑤ 0x46=0x01 ，0x47=0x00，to trig effuse read enable.

Repeat step④⑤，until read is done

⑥ 0x41=0x01，set RDEN low

⑦ 0x41=0x02

7.3 Efuse write address calculation:

For example, if you need to burn 0x51[3]=1

0) Find the EFUSE address corresponding to the 0x51 byte address is byte[2:0]=0x001
1) Find the bit you need to burn 1 is bit=3, bit[2:0]=0x011.
2) Effuse_addr = bit[2:0]_byte[2:0] = 011_001 = 0x19

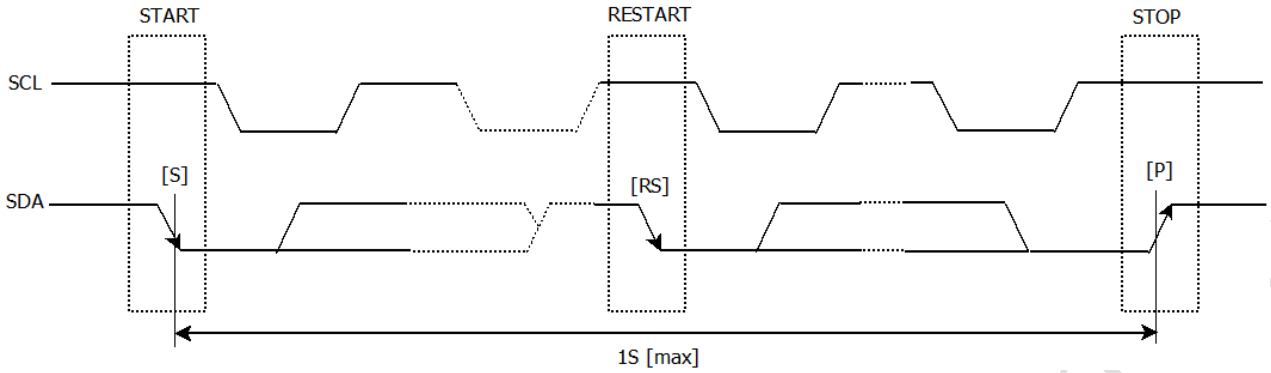
7.4 Efuse read address calculation:

If you need to read 0x51 efuse data :

Find 0x51 byte address, byte[2:0]=0x001

Effuse_addr = xxx_byte[2:0] = xxx_001 = 000_001 = 0x01

8 I²C Bus Interface



I²C bus supports bi-directional communications through a serial clock line SCL and a serial data line SDA. I²C bus device can be defined as "Master" and "Slave". DPXA05 can only be used as Slave.

8.1 Cautions

I²C bus includes START, RESTART, STOP conditions, the duration between START and STOP must be less than 1 second just in case the bus to be set to standby mode automatically. A new START condition must be transferred before restarting of any communications.

DPXA05 I²C bus interface supports single byte read/write operations as well as multiple bytes incremental access. After 0xFF address, the next one will be 0x00.

8.2 Slave Address

Table10. I²C Bus Slave Address

Transfer data	Slave address							R/W
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
65h (Read)	0	1	1	0	0	1	0	1 (Read)
64h (Write)								0 (Write)

DPXA05 I²C bus Slave Address is [0110 010*].

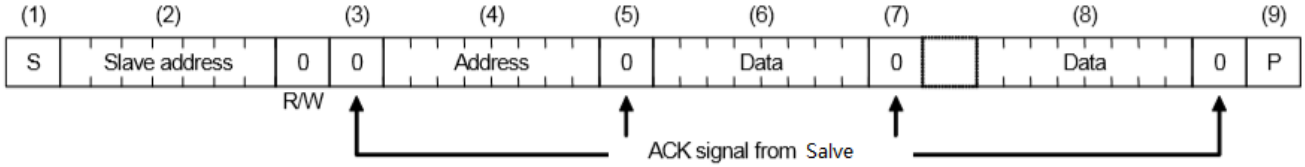
8.3 I²C bus protocol

It is assumed CPU is master and DPXA05 is slave in this section.

8.3.1 Write process

I²C bus includes an address auto-increment function, once the initial address has been specified, the DPXA05 increments (+1) the address automatically after each data is sent, then to write next data.

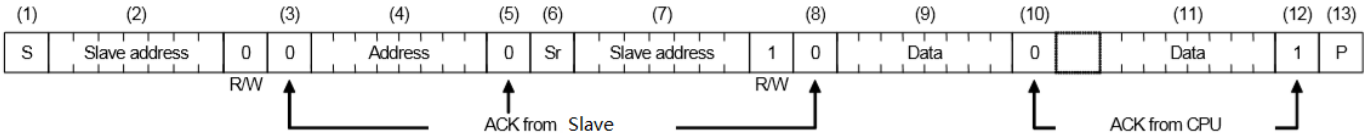
(1) CPU sends start condition[S]
(2) CPU sends DPXA05's slave address with R/W bit to set to write mode
(3) CPU verifies ACK signal from DPXA05
(4) CPU sends write address to DPXA05
(5) CPU verifies ACK signal from DPXA05
(6) CPU sends write data to the address specified at step (4)
(7) CPU verifies ACK signal from DPXA05
(8) Repeat (6) (7) if multiple bytes need to be written, address will be incremented automatically
(9) CPU ends stop condition[P]



8.3.2 Read process

Writing the address to be read with write mode firstly, then reading the data with read mode.

(1) CPU sends start condition[S]
(2) CPU sends DPXA05's slave address with R/W bit to set to write mode
(3) CPU verifies ACK signal from DPXA05
(4) CPU sends address for reading from DPXA05
(5) CPU verifies ACK signal from DPXA05
(6) CPU sends RESTART condition [Sr]
(7) CPU sends DPXA05's slave address with R/W bit to set to read mode
(8) CPU verifies ACK signal from DPXA05
(9) CPU reads data from the specified address in step (4)
(10) CPU sends ACK signal for "0"
(11) Repeat (9) (10) if multiple bytes need to be read, address will be incremented automatically
(12) CPU sends ACK signal for "1"
(13) CPU sends stop condition[P]



9 Revision History

Version	Change Contents	Prepared by	Revised Date
V1.0	First Issued		2025.01.15