裕太微电子
Motor Comm

Motorcomm YT8522

Datasheet

10/100 FAST ETHERNET TRANSCEIVER

VERSION DRAFT 0.2
DATE 2023-03-14

Copyright Statement

Disclaimer

This document only provides periodic information, and its contents will/may be updated from time to time according to actual situation of Motorcomm’s products without further notice. Motorcomm will not take any responsibility for any direct or indirect losses caused due to improper use of this document.

Revision History

Revision	Release Date	Summary
Draft 0.1	2022/12/04	draft version
Draft 0.2	2023/3/11	Modify strappin setting and some description errors

Content

List of Table

List of Figures

1. General Description

The YT8522 is a low power single-port 10/100 Mbps Ethernet PHY. It provides all physical layer functions needed to transmit and receive data over both standard twisted pair cables transceiver or Fiber PECL interface to an external 100Base-FX optical transceiver module. Additionally, the YT8522 provides flexibility to connect to a MAC through a standard MII and RMII interface.

The YT8522 uses mixed-signal processing to perform equalization, data recovery, and error correction to achieve robust operation over CAT5 twisted-pair cable or 100Base-FX optical transceiver module.

The YT8522 offers integrated built-in self-test and loopback capabilities for ease of use.

The YT8522 offers innovative and robust approach for reducing power consumption through EEE, WoL and other programmable energy savings modes.

1.1. Features

- Supports IEEE 802.3az (Energy Efficient Ethernet)
- 100Base-TX IEEE 802.3u Compliant
- 10Base-Te IEEE 802.3 Compliant
- Supports MII mode
- Supports RMII mode
- Supports I/O 1.5V/1.8V/2.5V/3.3V (except for Crystal and LED pins)
- Full/Half duplex operation
- Twisted pair or fiber mode output
- Supports Auto-negotiation
- Supports Power down mode
- Supports Base Line Wander (BLW) compensation
- Supports Auto MDIX
- Supports Interrupt function
- Supports WOL, Wake on Lan
- Automatic Polarity correction
- 2 sets LED indicator
- 25 MHz crystal or OSC
- Provide 50Mhz clock source for MAC
- Single Power supply, internal LDO
- Package QFN 32, 5x5mm

1.2. Target Applications

- Ethernet Switch
- DTV (Digital TV)
- Communication and Network Riser
- Routers, PON Equipment

- Printer and Office Machine
- MAU(Media Access Unit)

2. Pin Assignment

2.1. Pin Map

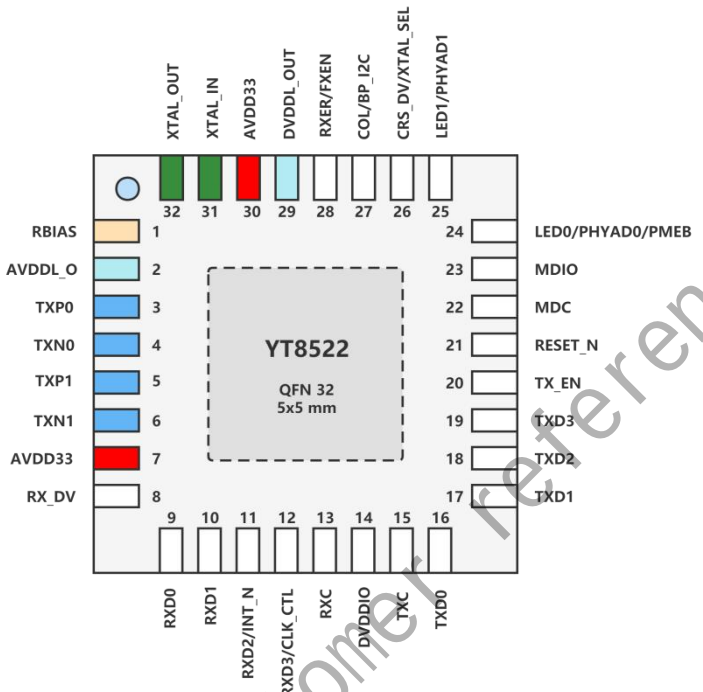


Figure 1.PIN MAP-YT8522

2.2. Pin Descriptions

- I = Input
- O = Output
- I/O = Bidirectional
- OD = Open–drain output
- PU = Internal pull–up
- PD = Internal pull–down
- HZ = High Impendence during power on reset
- PWR = Power related
- XT = Crystal related

Table 1.Pin Assignment

No.	Name	Type	Description
1	RBIAS	I	Bias Resistor. An external 2.49 kΩ ± 1% resistor must be connected between the RBIAS pin and GND
2	AVDDL_REG	PWR/O	Power Output. Be sure to connect a 1uF +0.1uF ceramic capacitor for decoupling purposes.
3	TRXP0	IO	Transmit/Receive Pairs for channel 0. Differential data from copper media is transmitted and received on the single TRD ± signal pair. There are 50Ω internal terminations on each pin. Since this device incorporates voltage driven DAC, it does not require a center–tap power supply.
4	TRXN0	IO	
5	TRXP1	IO	Transmit/Receive Pairs for channel 1. Differential data from copper media is transmitted and received on the single TRD ± signal pair. There are 50Ω internal terminations on each pin. Since this device incorporates voltage driven DAC, it does not require a center–tap power supply.
6	TRXN1	IO	
7	AVDD33	PWR	3.3V Analog Power Input. 3.3V power supply for analog circuit; should be well decoupled.
8	RX_DV	O/PD	Receive Data Valid. This pin’s signal is asserted high when received data is present on the RXD[3:0] lines. The signal is de–asserted at the end of the packet. The signal is valid on the rising edge of the RXC. This pin should be pulled low when operating in MII mode. Power On Strapping for MII/RMII selection. 0: MII mode 1: RMII mode An internal weakly pulled low resistor sets this to the default of MII mode. It is possible to use an external 4.7KΩ pulled high resistor to enable RMII mode.After power on, the pin operates as the Receive Data Valid pin.
9	RXD[0]	O/PD	Receive Data [0]
10	RXD[1]	O/PD	Receive Data [1] An internal weakly pulled low resistor sets RXD[1] to the LED function (default). Use an external 4.7KΩ pulled high resistor to enable the WOL function.
11	RXD[2]/INT_N	O/OD/PD	Receive Data [2] When in RMII mode, this pin is used for the interrupt function.
12	RXD[3]/CLK_CTL	O/PD	Receive Data [3] RXD[3]/CLK_CTL pin is the Power On Strapping in RMII Mode. 1: REF_CLK input mode, RMII1 mode 0: REF_CLK output mode, RMII2 mode Note: An internal weakly pulled low resistor sets RXD[3]/CLK_CTL to REF_CLK output mode (default).

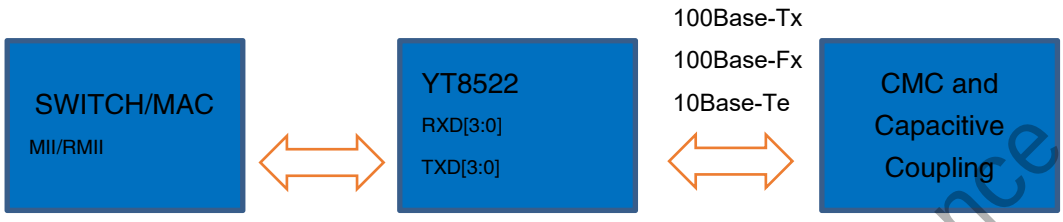
13	RXC	O/PD	Receive Clock. This pin provides a continuous clock reference for RX_DV and RXD [0:3] signals. RXC is 25MHz in 100Mbps mode and 2.5MHz in 10Mbps mode.
14	DVDDIO	PWR	Supports 3.3V/2.5V/1.8V/1.5V Digital Power Input. 3.3V/2.5V/1.8V/1.5V power supply for digital circuit.
15	TXC	IO/PD	MII Mode Transmit Clock. This pin provides a continuous clock as a timing reference for TXD [3:0] and TXEN signals. TXC is 25MHz in 100Mbps mode and 2.5MHz in 10Mbps mode RMII Mode Synchronous 50MHz Clock Reference for Receive, Transmit, and Control Interface. The default direction is reference clock output mode if RXD[3]/CLK_CTL pin floating.
16	TXD[0]	I/PD	Transmit Data [0]
17	TXD[1]	I/PD	Transmit Data [1]
18	TXD[2]	I/PD	Transmit Data [2]
19	TXD[3]	I/PD	Transmit Data [3]
20	TX_EN	I/PD	MII/RMII Mode Transmit Enable. The input signal indicates the presence of valid nibble data on TXD [3:0]. An internal weakly pulled low resistor prevents the bus floating.
21	RESET_N	I,HZ	RESET. Active–low, reset pin for chip.
22	MDC	I/PU	Management Data Clock. This pin provides a clock synchronous to MDIO, which may be asynchronous to the transmit TXC and receive RXC clocks. The clock rate can be up to 12.5MHz. Use an internal weakly pulled high resistor to prevent the bus floating.
23	MDIO	IO/PU	Management Data Input/Output. This pin provides the bi–directional signal used to transfer management information
24	LED0/PHYAD[0]/ PMEB	O/OD/PD	LED 0, Link On/Off. PHY address 0 selection
25	LED1/PHYAD[1]	O/PD	LED 1, Link On/Off,Active blink. PHY address 1 selection
26	CRS/CRS_DV/ XTAL_SEL	O/PD	MII mode: Carrier Sense. This pin’s signal is asserted high if the media is not in Idle state. RMII mode: Carrier Sense/Receive Data Valid. CRS_DV shall be asserted by the PHY when the receive medium is non–idle. This pin status is latched at power on reset to determine Reference Clock Input Selection .

			1:Reference Clock from TXC 0:Reference Clock from XTAL An internal weakly pulled low resistor sets this to select Reference Clock from XTAL.It is possible to use an external 4.7KΩ pulled high resistor to select Reference Clock from TXC.After power on,the pin operates as the CRS/CRS_DV pin.
27	COL/BP_I2C	O/PD	Collision Detect. COL is asserted high when a collision is detected on the media. It is possible to use an external 4.7KΩ pulled high resistor to bypass I2C load.After power on,the pin operates as the collision detect pin.
28	RXER/FXEN	O/PD	Receive Error. 100FX/UTP Enable. This pin status is latched at power on reset to determine the media mode to operate in. 1:Fiber mode 0:UTP mode An internal weakly pulled low resistor sets this to the default of UTP mode.It is possible to use an external 4.7KΩ pulled high resistor to enable fiber mode.After power on,the pin operates as the receive error pin.
29	DVDDL_REG	PWR/O	DVDDL Power Output. Be sure to connect a 1uF +0.1uF ceramic capacitor for decoupling purposes.
30	AVDD33	PWR	3.3V Analog Power Input. 3.3V power supply for analog circuit; should be well decoupled.
31	XTAL_IN	XT	25 MHz Crystal Input Pin. If use external oscillator or clock from another device. 1. When an external 25Hhz oscillator or clock from another device drivers XTAL_OUT. XTAL_IN must be shorted to GND 2. When an external 25Hhz oscillator or clock from another device drivers XTAL_IN; keep the XTAL_OUT floating.
32	XTAL_OUT	XT	25 MHz Crystal Output Pin. If use external oscillator or clock from another device. 1. When an external 25Hhz oscillator or clock from another device drivers XTAL_OUT. XTAL_IN must be shorted to GND 2. When an external 25Hhz oscillator or clock from another device drivers XTAL_IN; keep the XTAL_OUT floating.
33	EPAD	GND	Exposed ground pad on back of the chip, tie to ground

3. Function Description

3.1. Application Diagram

3.1.1. 100Base-Tx/100Base-Fx/10Base-Te application



3.2. MII interface

The Media Independent Interface (MII) is the digital data interface between the MAC and the physical layer that can be enabled when the device is functioning in 10BASE-Te, 100BASE-TX/FX,. The original MII transmit signals include TX_EN, TXC, TXD[3:0], and TX_ER. The receive signals include RX_DV, RXC, RXD[3:0], and RX_ER. The media status signals include CRS and COL. Due to pin-count limitations, the YT8522 supports a subset of MII signals. This subset includes all MII signals except TX_ER.

3.3. RMII interface

Reduced media-independent interface (RMII) is a standard which was developed to reduce the number of signals required to connect a PHY to a MAC. If this interface is active, the number of data signal pins required to and from the MAC is reduced to half by doubling clock frequency.

3.4. Management interface

The Status and Control registers of the device are accessible through the MDIO and MDC serial interface. The functional and electrical properties of this management interface comply with IEEE 802.3, Section 22 and also support MDC clock rates up to 12.5 MHz

3.5. DAC

The digital-to-analog converter (DAC) transmits MLT3, and Manchester coded symbols. The transmit DAC performs signal wave shaping that reduces electromagnetic interference (EMI). The transmit DAC uses voltage driven output with internal terminations and hence does not require external components or magnetic supply for operation.

3.6. ADC

Receive channel has its own analog–to–digital converter (ADC) that samples the incoming data on the receive channel and feeds the output to the digital data path.

3.7. Adaptive equalizer

The digital adaptive equalizer removes inter–symbol interference (ISI) created by the channel. The equalizer accepts sampled data from the analog–to–digital converter (ADC) on channel and produces equalized data. The coefficients of the equalizer are adaptive to accommodate varying conditions of cable quality and cable length.

3.8. Auto– negotiation

The YT8522 negotiates its operation mode using the auto negotiation mechanism according to IEEE 802.3 clause 28 over the copper media. Auto negotiation supports choosing the mode of operation automatically by comparing its own abilities and received abilities from link partner. The advertised abilities include:

a) Speed: 10/100Mbps

b) Duplex mode: full duplex and/or half duplex

c) Pause

Auto negotiation is initialized when the following scenarios happen:

a) Power–up/Hardware/Software reset

b) Auto negotiation restart

c) Transition from power–down to power up

d) Link down

Auto negotiation is enabled for YT8522 by default, and can be disable by software control.

3.9. Polarity detection and auto correction

YT8522 can detect and correct two types of cable errors: swapping of pairs within the UTP cable and swapping of wires within a pair.

For 10BASE–Te/100BASE–TX, YT8522 can handle both cable errors at the same time.

3.10. EEE

EEE is IEEE 802.3az, an extension of the IEEE 802.3 standard. EEE defines support for the PHY to operate in Low Power Idle (LPI) mode which, when enabled, supports QUIET times during low link utilization allowing both link partners to disable portions of each PHY's circuitry and save power.

4. Power Requirements

4.1. Power consumption

4.1.1. MII mode

Table 2. Power consumption-MII mode

Condition		3.3V(Pull up)	AVDD33	DVDDIO	3.3V total(mA)
Reset					
Power down					
Hibernation					
Active					
Link	10M				
	100M				
Traffic	10M				
	100M				

4.1.2. RMII mode

Table 3. Power consumption-RMII mode

Condition		3.3V(Pull up)	AVDD33	DVDDIO	3.3V total(mA)
Reset					
Power down					
Hibernation					
Active					
Link	10M				
	100M				
Traffic	10M				
	100M				

Unit is mA

Note: The power consumption is measured under room temperature with typical process DUT.

4.2. Maximum Power Consumption MII MODE

Table 4. Maximum Power Consumption MII MODE

Condition		3.3V(Pull up)	AVDD33	DVDDIO	3.3V total(mA)
Traffic	100M				

Note: The Maximum power consumption is measured under high temperature(T_A=85° C) with FF corner process (fast nmos and fast pmos)DUT.

5. Operational Description

5.1. Reset

YT8522 have a hardware reset pin(RESET_N) which is low active. RESET_N should be active for at least 10ms to make sure all internal logic is reset to a known state. Hardware reset should be applied after power up.

RESET_N is also used as enable for power on strapping. After RESET_N is released , YT8522 latches input value on POS related pins are used as configuration information which provides flexibility in application without mdio access.

YT8522 also provides a software reset control registers which are used to reset all internal logic except some mdio configuration registers. For detailed information about what register will be reset by software reset, please refer to register table.

5.2. Strapping pins setting

5.2.1. POS

Table 5.Power on strapping

No.	Name	POS	Internal Pull/Down	Description
24	LED0/PHYAD[0]	phy_address[0]	Pull Down	The PHY address is 00~11 config by phy_address[1:0].Wol_led_sel=1, this PAD works as PMEB, it shall be external pull–up, then phy_address[0] always =1.
25	LED1/PHYAD[1]	phy_address[1]	Pull Down	The PHY address is 00~11 config by phy_address[1:0]
10	RXD[1]	Wake on LAN selection	Pull Down	The power on strapping value of PAD RXD1, Wol_led_sel, determines the PAD LED0 working as LED0 or PMEB. 1, LED0 works as PMEB (WOL interrupt) 0, LED0 works as LED0.
12	RXD[3]/ CLK_CTL	Clock control	Pull Down	The power–on strapping value of {RX_DV, RXD3} determines the xMII mode:

8	RX_DV	MII/RMII mode selection	Pull Down	{RX_DV, RXD3}=2’b00 means MII mode; {RX_DV, RXD3}=2’b01 means ReMII mode; {RX_DV, RXD3}=2’b10 means RMII2 mode, TXC 50Mhz reference clock is output. {RX_DV, RXD3}=2’b11 means RMII1 mode, TXC 50Mhz reference clock is input.
26	CRS/CRS_DV/ XTAL_SEL	Reference Clock selection	Pull Down	This pin status is latched at power on reset to determine Reference Clock Input Selection . 1:Reference Clock from TXC 0:Reference Clock from XTAL An internal weakly pulled low resistor sets this to select Reference Clock from XTAL.It is possible to use an external 4.7KΩ pulled high resistor to select Reference Clock from TXC.After power on,the pin operates as the CRS/CRS_DV pin.
27	COL/BP_I2C	Bypass I2C load	Pull Down	It is possible to use an external 4.7K Ω pulled high resistor to bypass I2C load.After power on,the pin operates as the collision detect pin.
28	RX_ER/FXEN	FX_EN	Pull Down	This pin status is latched at power on reset to determine the media mode to operate in. 1:Fiber mode 0:UTP mode An internal weakly pulled low resistor sets this to the default of UTP mode.It is possible to use an external 4.7K Ω pulled high resistor to enable fiber mode.After power on,the pin operates as the receive error pin.

5.2.2. Phy address

Table 6.Power on strapping-Phy address

Pin 24 LED0/ PHYAD[0] (PD)	Pin 25 LED1/ PHYAD[1] (PD)	PHY address
0	0	00
0	1	10
1	0	01
1	1	11

5.2.3. Mode config

Table 7.Power on strapping-Mode config

Pin 8 RX_DV (PD)	Pin 12 RXD3 (PD)	Mode
0	0	MII
0	1	ReMII, Reverse MII Mode
1	0	RMII2, TXC 50Mhz reference clock is output by default
1	1	RMII1, TXC 50Mhz reference clock is input

5.2.4. Wake on lan selection

Table 8.Power on strapping-Wake on lan

Pin 10 RXD1 (PD)	Function	Mote
0	LED Mode	Pin 24 is LED0
1	WOL Mode	Pin 24 is PMEB, Must external pull up

5.3. XMII interface

YT8522 support 4 kinds of MII related interfaces: MII, RMII1, RMII2 and REMII.

5.3.1. MII

The Media Independent Interface (MII) is the digital data interface between the MAC and the physical layer that can be enabled when the device is functioning in 10BASE–Te, 100BASE–TX, The original MII transmit signals include TX_EN, TXC, TXD[3:0], and TX_ER. The receive signals include RX_DV, RXC, RXD[3:0], and RX_ER. The media status signals include CRS and COL. Due to pin–count limitations, the YT8522 supports a subset of MII signals. This subset includes all MII signals except TX_ER. For 100M application, TXC and RXC are 25MHz; for 10M application, TXC and RXC are 2.5MHz. TXC and RXC are output in this case.

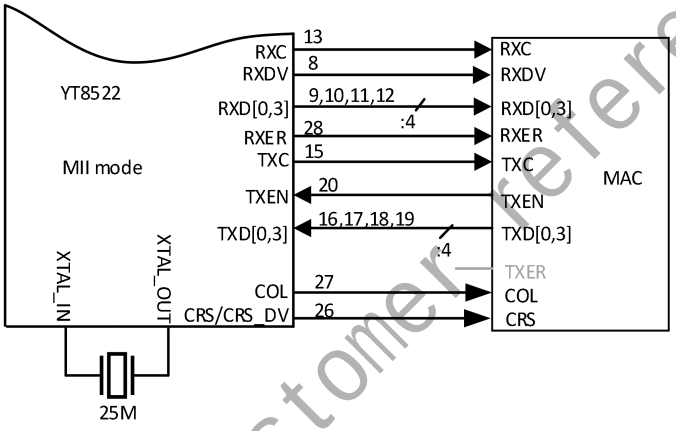


Figure 2. connection diagram of MII

5.3.2. RMII

Reduced media–independent interface (RMII) is a standard which was developed to reduce the number of signals required to connect a PHY to a MAC. If this interface is active, the number of data signal pins required to and from the MAC is reduced to half by doubling clock speed compared to MII. It has 7 signals: REF_CLK, TX_EN, TXD[1:0], RX_DV and RXD[1:0]. In YT8522, we use TXC as REF_CLK. For 100M application, REF_CLK is 50MHz; for 10M application, REF_CLK is still 50MHz, data will be duplicated for 10 times in 20ns cycles. YT8522 supports two types of connection method;

1. RMII1 mode: This is fully conforming to RMII standard.
2. RMII2 mode: TXC will be 50MHz output to MAC.

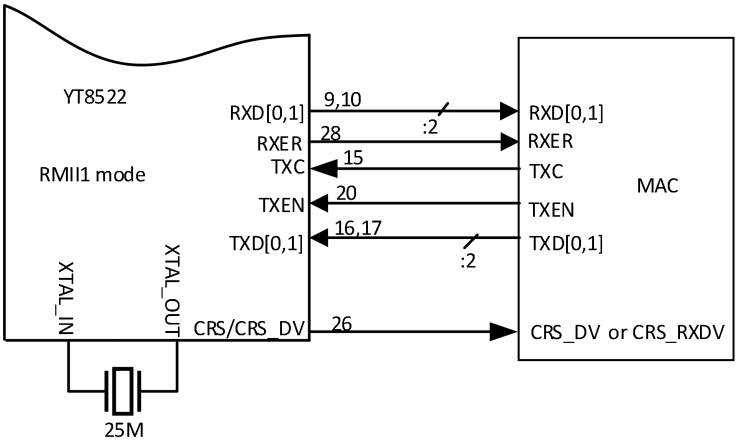


Figure 3. connection diagram of RMII1(with 25MHz and 50MHz clock)

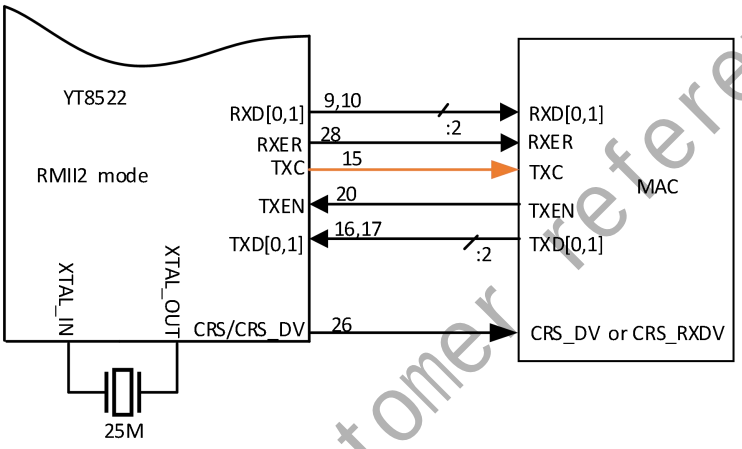


Figure 4. connection diagram of RMII2

5.3.3. REMII interface

Reverse media independent interface is the opposite of MII interface. The only difference is the direction of tx clock and rx clock. For MII, tx clock and rx clock are output; for REMII, tx clock and rx clock are input. REMII interface are used for back to back connection of two phys.

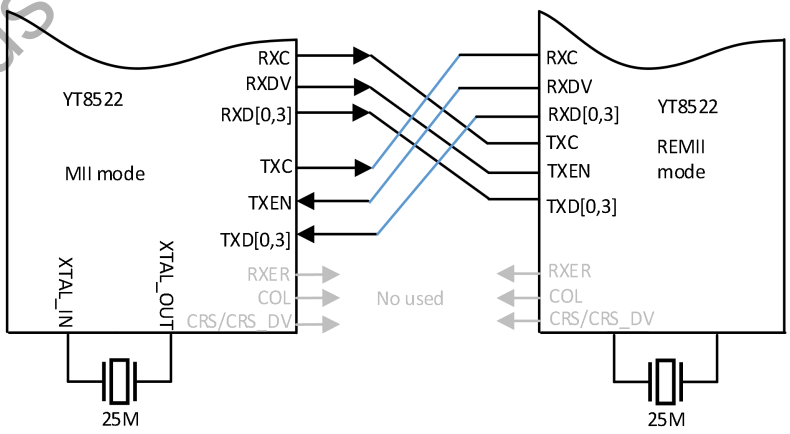


Figure 5. connection diagram of REMII

5.4. Loopback mode

There are three loopback modes in YT8522.

5.4.1. Internal loopback:

In Internal loopback mode, YT8522 feed transmit data to receive path in chip.

Configure bit 14 of mii register(address 0h0) to enable internal loopback mode. For 10Base–Te and 100Base–Tx, YT8522 feeds digital DAC data to ADC directly.

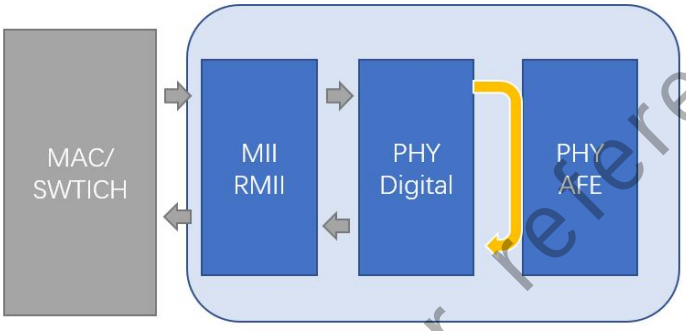


Figure 6. Internal loopback

5.4.2. External loopback

In external loopback mode, YT8522 feed transmit data to receive path out of chip. For 10Base–Te and 100Base–Tx, just connect TRX_P0/N0 to TRX_P1/N1.

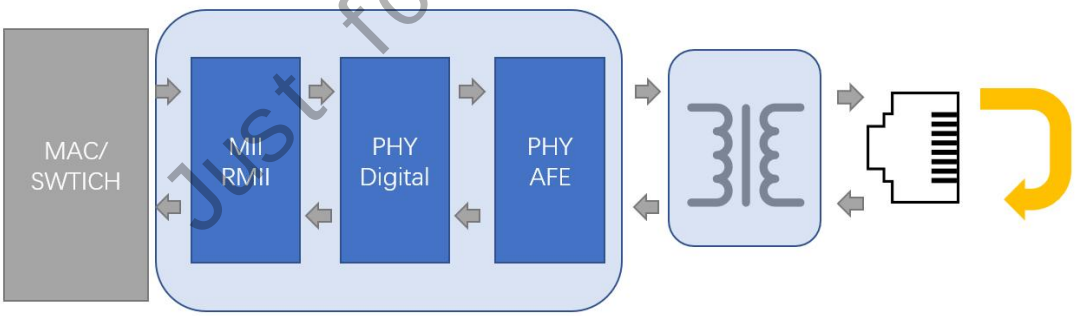


Figure 7. External loopback

5.4.3. Remote loopback

In remote loopback mode, YT8522 feed MII receive data to transmit path in chip. Configure bit 11 of extended register(address 0h4000) and for TRX interface, just connect to link partner normally.

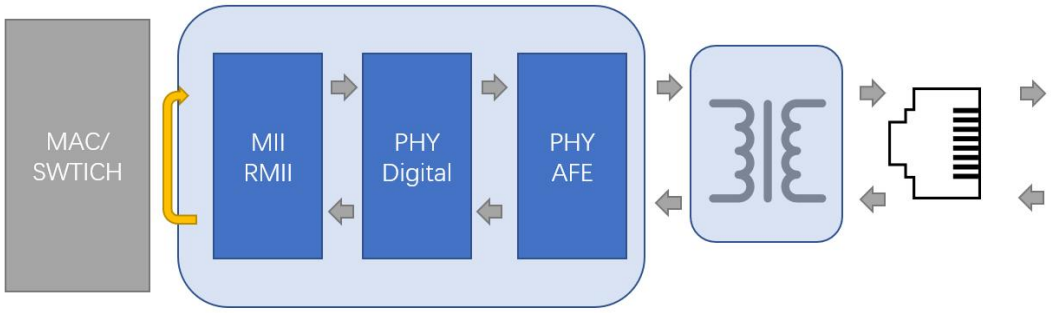


Figure 8. Remote loopback

5.5. WoL Wake on lan

5.5.1. WOL

Wake-on-LAN (WOL) is a mechanism to manage and regulate the total network power consumption.

5.5.2. WOL mechanism

YT8522 supports automatic detection of a specific frame and notification via dedicated hardware interrupt pin or general PHY interrupt pin. The specific frame contains a specific data sequence located anywhere inside the packet. The data sequence consists of 6 bytes of consecutive 1 (0xFFFFFFFFFFFF), followed by 16 repetitions of the MAC address of the computer to be waked up. The 48-bit MAC address is written in EXT 0x4004, 0x4005, 0x4006 registers.

For example, to write a specific MAC address (0xAAAABBBBCCCC) to PHY, write EXT 0x4004 = 0xAAAA, 0x4005 = 0xBBBB, and 0x4006 = 0xCCCC. The PHY internal MAC address can be set to any value.

NOTE: The MAC address is not a real MAC address and is only a symbol to indicate the content of the frame.

The WOL mechanism is enabled via EXT 0x4000 bit2. POS RXD[1] can't control enable or disable the WOL mechanism but only control pad LED0 working as WOL interrupt.

5.5.2.1. WOL Interrupt

YT8522 support dedicated WOL interrupt pin. When the pad RXD[1] is externally PULL UP, pad LED0 will work as WOL interrupt.

If EXT 0x4003 bit7 is 0, the dedicated WOL interrupt is programmed to a level, otherwise, it's programed to a pulse; either is active low. When it's programmed to a pulse, the pulse width can be programmed via EXT 0x4003 bit9:8.

WOL interrupt is also wire–and to general PHY interrupt RXD[2]_INTN when the bit6 INT_WOL in Interrupt enable register (MII Register 0x12) is set to 1. If the general PHY interrupt is triggered by WOL, it can be cleared by reading MII register 0x13 bit6.

NOTE:

When general PHY interrupt is used to monitor WOL interrupt, EXT 0x4003 bit7 should be 1, otherwise, the general PHY interrupt can't be read cleared.

Because PHY requires to receive packets from the line side, PHY cannot be powered down. If the link partner supports Energy Efficient Ethernet function, both ends can use EEE mode to save more power.

MII register 0x0 bit10 ISOLATE: When this bit is set to 1, the xMII output pins are HighZ. The xMII inputs are ignored.

6. Register Overview

7. Timing and electrical characteristics

7.1. Absolute Maximum Ratings

Table 11. Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
AVDD33	3.3 V power supply	–0.3	3.70	V
AVDDL	1.2 V power supply	–0.2	1.50	V
DVDDL	1.2 V power supply	–0.2	1.50	V
DVDDIO 3.3V	3.3V power supply	–0.3	3.70	V
DVDDIO 2.5V	2.5V power supply	–0.3	2.8	V
DVDDIO 1.8V	1.8V power supply	–0.3	2.3	V
DVDDIO 1.5V	1.5V power supply	TBD	TBD	V

7.2. Recommended Operating Condition

Table 12. Recommended Operating Condition

Description	Pins	Min	Typ	Max	Unit
Power Supply	AVDD33	2.97	3.30	3.63	V
	AVDDL	1.08	1.20	1.32	V
	DVDDL	1.08	1.20	1.32	V
	DVDDIO 3.3V	2.97	3.30	3.63	V
	DVDDIO 2.5V	2.25	2.50	2.75	V
	DVDDIO 1.8V	1.71	1.8	1.89	V
	DVDDIO 1.5V	TBD	1.5	TBD	V
YT8522C Ambient Operation Temperature Ta		0	–	70	° C
YT8522H Ambient Operation Temperature Ta		–40	–	85	
Maximum Junction Temperature				125	° C

7.3. Crystal Requirement

Table 13. Crystal Requirement

Symbol	Description	Min	Typ	Max	Unit
Fref	Crystal Reference Frequency	–	25	–	MHz
Fref Tolerance	Crystal Reference Frequency tolerance	–50	–	50	ppm
Duty Cycle	Reference clock input duty cycle	40	–	60	%
ESR	Equivalent Series Resistance	–		50	ohm
DL	Drive Level	–	–	0.5	mW
Vih	Crystal output high level	1.4	–	–	V
Vil	Crystal output low level	–	–	0.4	V

7.4. Oscillator/External Clock Requirement

Table 14. Oscillator/External Clock Requirement

Parameter	Condition	Min	Typ	Max	Unit
Frequency			25		MHz
Frequency tolerance	Ta= –40~85 C	–50		50	PPM
Duty Cycle		40	–	60	%
Peak to Peak Jitter				200	ps
Vih		1.4		AVDD33+0.3	V
Vil				0.4	V
Rise Time	10%~90%			10	ns
Fall Time	10%~90%			10	ns
Temperature Range	YT8522C	0		70	° C
Temperature Range	YT8522H	–40		85	° C

7.5. DC Characteristics

Table 15. DC Characteristics

Symbol	Description	Min	Typ	Max	Unit
AVDD33	3.3V power supply	2.97	3.3	3.63	V
DVDDL	1.2V power supply	1.08	1.2	1.32	V
AVDDL	1.2V power supply	1.08	1.2	1.32	V
DVDDIO 3.3V	3.3V power supply	2.97	3.30	3.63	V
DVDDIO 2.5V	2.5V power supply	2.25	2.50	2.75	V
DVDDIO 1.8V	1.8V power supply	1.71	1.8	1.89	V
DVDDIO 1.5V	1.5V power supply	TBD	1.5	TBD	V
Voh 3.3V	Minimum High Level Voltage Output Voltage	2.4	–	3.6	V
Vol 3.3V	Minimum Low Level Voltage Output Voltage	–0.3	–	0.4	V
Vih 3.3V	Maximum High Level Input Voltage	2	–	–	V
Vil 3.3V	Maximum Low Level Input Voltage	–	–	0.8	V
Voh 2.5V	Minimum High Level Voltage Output Voltage				
Vol 2.5V	Minimum Low Level Voltage Output Voltage				
Vih 2.5V	Maximum High Level Input Voltage				
Vil 2.5V	Maximum Low Level Input Voltage				
Voh 1.8V	Minimum High Level Voltage Output Voltage				
Vol 1.8V	Minimum Low Level Voltage Output				

	Voltage				
Vih 1.8V	Maximum High Level Input Voltage				
Vil 1.8V	Maximum Low Level Input Voltage				
Voh 1.5V	Minimum High Level Voltage Output Voltage				
Vol 1.5V	Minimum Low Level Voltage Output Voltage				
Vih 1.5V	Maximum High Level Input Voltage				
Vil 1.5V	Maximum Low Level Input Voltage				

7.6. MDC/MDIO Timing

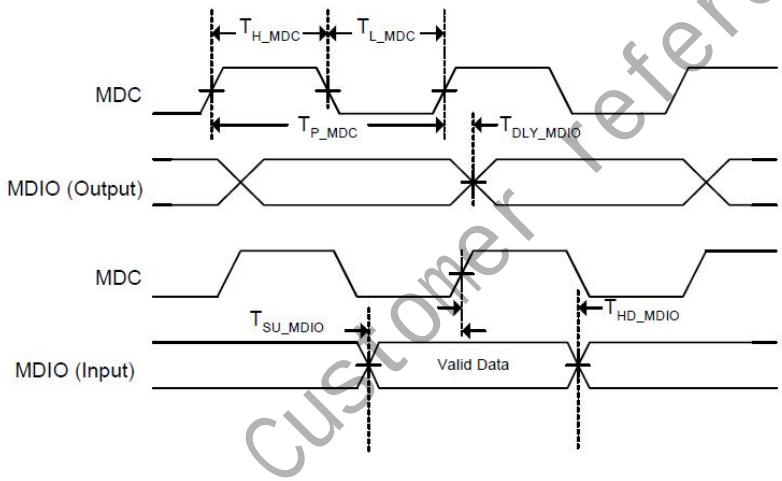


Figure 9. MDC/MDIO Timing

Table 16. MDC/MDIO Timing

Symbol	Description	Min	Typ	Max	Unit
T_{DLY_MDIO}	MDC to MDIO Output Delay Time			20	ns
T_{SU_MDIO}	MDIO Input to MDC Setup Time	10			ns
T_{HD_MDIO}	MDIO Input to MDC Hold Time	10			ns
T_{P_MDC}	MDC Period	80			ns
T_{H_MDC}	MDC High	30			ns
T_{L_MDC}	MDC Low	30			ns
Maximum Frequency = 12.5M Hz					

7.7. Power On Sequence/Clock/Reset

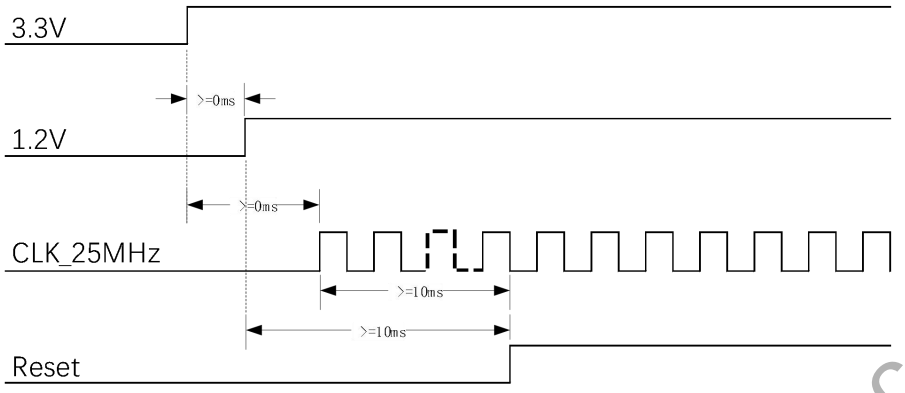


Figure 10. Power On Sequence

When using crystal, the clock generated internally, or 1.2V power from internal LDO, the sequence between clock and 3.3V, or 1.2V and 3.3V is determined by YT8522 inside and can be ignored.

When using external clock CLK_25MHz or 1.2V power from external power supply, the sequence between CLK_25MHz and 3.3V, or 1.2V and 3.3V should meet the requirements of the figure above.

No matter the clock and 1.2V from internal or external, for a reliable power on reset, suggest to keep asserting the reset low long enough (10ms) to ensure the clock is stable and clock–to–reset 10ms requirement is satisfied.

7.8. MII Transmission Cycle Timing

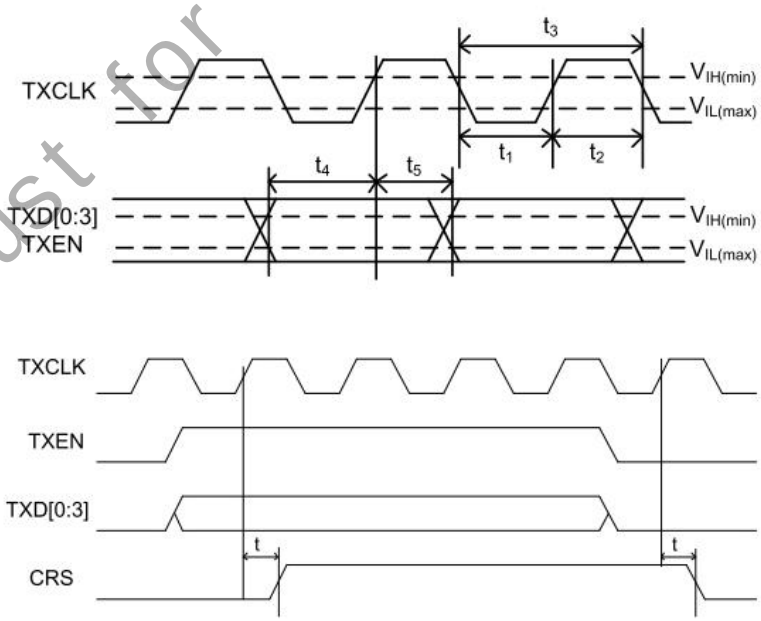


Figure 11. MII Transmission Cycle Timing

Table 17. MII Transmission Cycle Timing

Symbol	Description		Minimum	Typical	Maximum	Unit
t1	TXCLK High Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t2	TXCLK Low Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t3	TXCLK Period	100Mbps	–	40	–	ns
		10Mbps	–	400	–	ns
t4	TXEN, TXD[0:3] Setup to TXCLK Rising Edge	100Mbps	10	–	–	ns
		10Mbps	5	–	–	ns
t5	TXEN, TXD[0:3] Hold After TXCLK Rising Edge	100Mbps	0	–	–	ns
		10Mbps	0	–	–	ns
t6	TXEN Sampled to CRS High	100Mbps	–	–	40	ns
		10Mbps	–	–	400	ns
t7	TXEN Sampled to CRS Low	100Mbps	–	–	160	ns
		10Mbps	–	–	2000	ns

7.9. MII Reception Cycle Timing

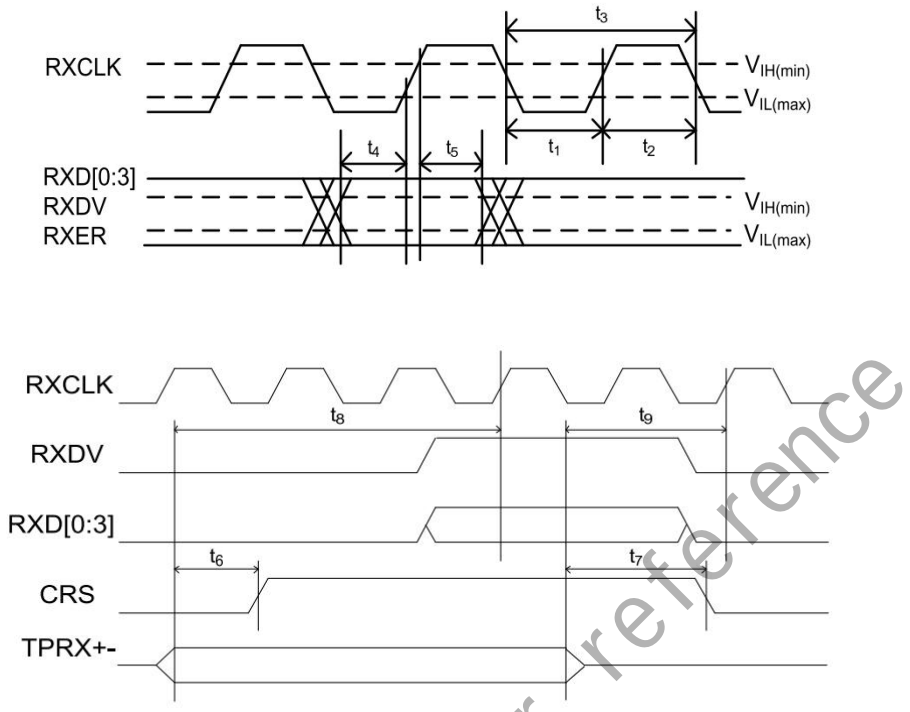


Figure 12. MII Reception Cycle Timing

Table 18. MII Reception Cycle Timing

Symbol	Description		Minimum	Typical	Maximum	Unit
t1	RXCLK High Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t2	RXCLK Low Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t3	RXCLK Period	100Mbps	–	40	–	ns
		10Mbps	–	400	–	ns
t4	RXER, RX_DV,RXD[0:3] Setup to RXCLK Rising Edge	100Mbps	10	–	–	ns
		10Mbps	10	–	–	ns
t5	RXER, RX_DV, RXD[0:3] Hold After RXCLK Rising Edge	100Mbps	10	–	–	ns
		10Mbps	10	–	–	ns
t6	Receive Frame to CRS High	100Mbps	–	–	130	ns
		10Mbps	–	–	2000	ns
t7	End of Receive Frame to CRS Low	100Mbps	–	–	240	ns
		10Mbps	–	–	1000	ns
t8	Receive Frame to Sampled Edge of RX_DV	100Mbps	–	–	150	ns
		10Mbps	–	–	3200	ns
t9	End of Receive Frame to Sampled Edge of RX_DV	100Mbps	–	–	120	ns
		10Mbps	–	–	1000	ns

7.10. RMII1 Transmission and Reception Cycle Timing

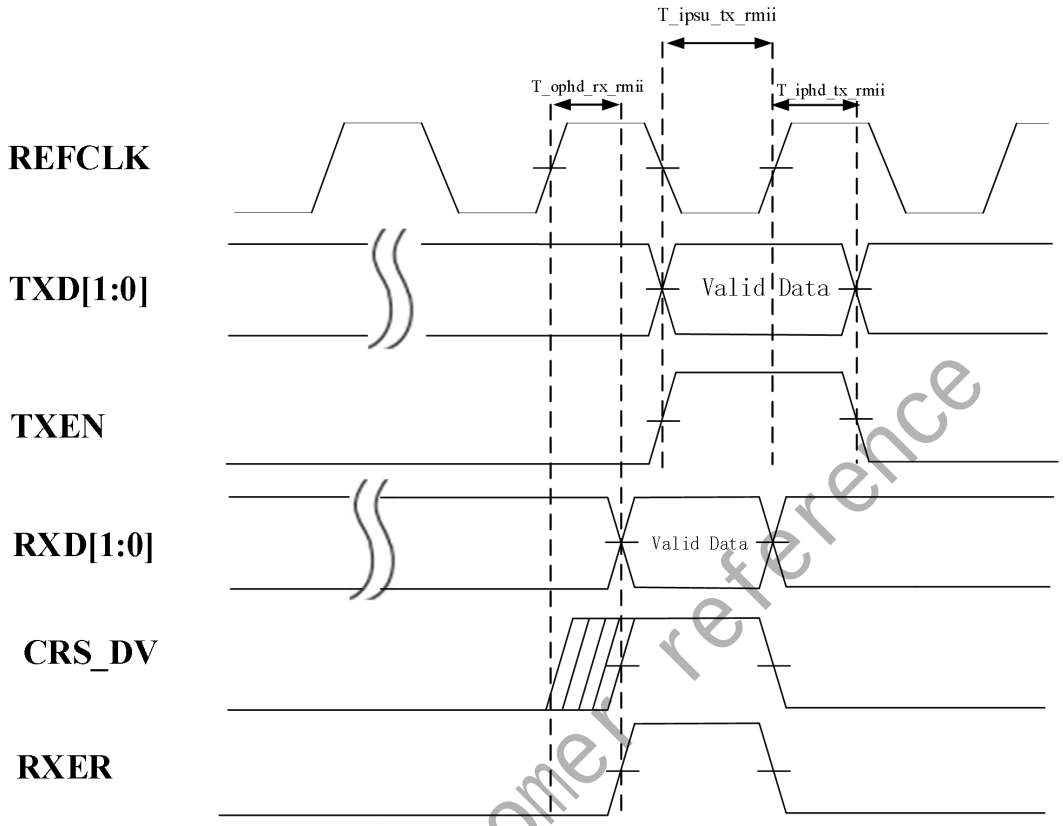


Figure 13. RMII1 Transmission and Reception Cycle Timing

Table 19. RMII1 Transmission and Reception Cycle Timing

Symbol	Description	Minimum	Typical	Maximum	Unit
REFCLK Frequency	Frequency of Reference Clock	–	50	–	MHz
REFCLK Duty Cycle	Duty Cycle of Reference Clock	35	–	65	%
T_ipsu_tx_rmii	TXD[1:0]/TXEN Setup Time to REFCLK	4	–	–	ns
T_iphd_tx_rmii	TXD[1:0]/TXEN Hold Time from REFCLK	2	–	–	ns
T_ophd_rx_rmii	RXD[1:0]/CRS_DV/RXER Output Delay Time from REFCLK	6	–	12	ns

7.11. RMII2 Transmission and Reception Cycle Timing

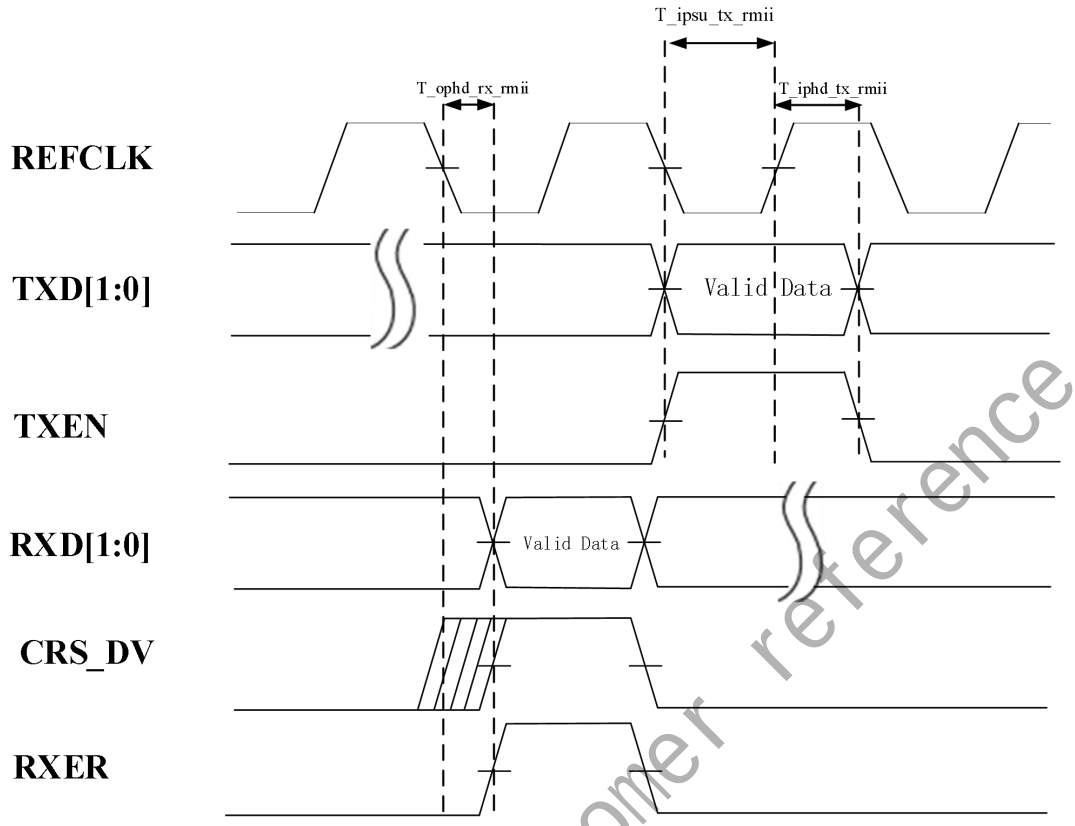


Figure 14. RMII2 Transmission and Reception Cycle Timing

Table 20. RMII2 Transmission and Reception Cycle Timing

Symbol	Description	Minimum	Typical	Maximum	Unit
REFCLK Frequency	Frequency of Reference Clock	–	50	–	MHz
REFCLK Duty Cycle	Duty Cycle of Reference Clock	35	–	65	%
T_ipsu_tx_rmii	TXD[1:0]/TXEN Setup Time to REFCLK	4	–	–	ns
T_iphd_tx_rmii	TXD[1:0]/TXEN Hold Time from REFCLK	2	–	–	ns
T_ophd_rx_rmii	RXD[1:0]/CRS_DV/RXER Output Delay Time from REFCLK	0	–	3	ns

8. Package information

8.1. RoHS–Compliant Packaging

Motor–comm offers a RoHS package that is compliant with RoHS

Table 24. RoHS-Compliant Packaging

Part Number	Status	Package	Op temp (℃)	Note
YT8522C	Active	QFN 32 5x5mm	0 to 70	
YT8522H	Active	QFN 32 5x5mm	–40 to 85	

8.2. Thermal resistance

Table 25. Thermal resistance

Symbol	Parameter	Conditon	Typ	Units
θ_{JA}	Thermal resistance – junction to ambient $\theta_{JA} = (T_J - T_A)/ P$ P = Total power dissipation	JEDEC 3 in. x 4.5 in. 4–layer PCB with no air flow T_A=25° C		° C/W
		JEDEC 3 in. x 4.5 in. 4–layer PCB with no air flow T_A=125° C		° C/W
θ_{JC}	Thermal resistance – junction to case $\theta_{JC} = (T_J - T_C)/ Ptop$ Ptop = Power dissipation from the top of the package	JEDEC with no air flow		° C/W
θ_{JB}	Thermal resistance – junction to board $\theta_{JB} = (T_J - T_B)/ Pbottom$ Pbottom = Power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		° C/W

9. Mechanical Information

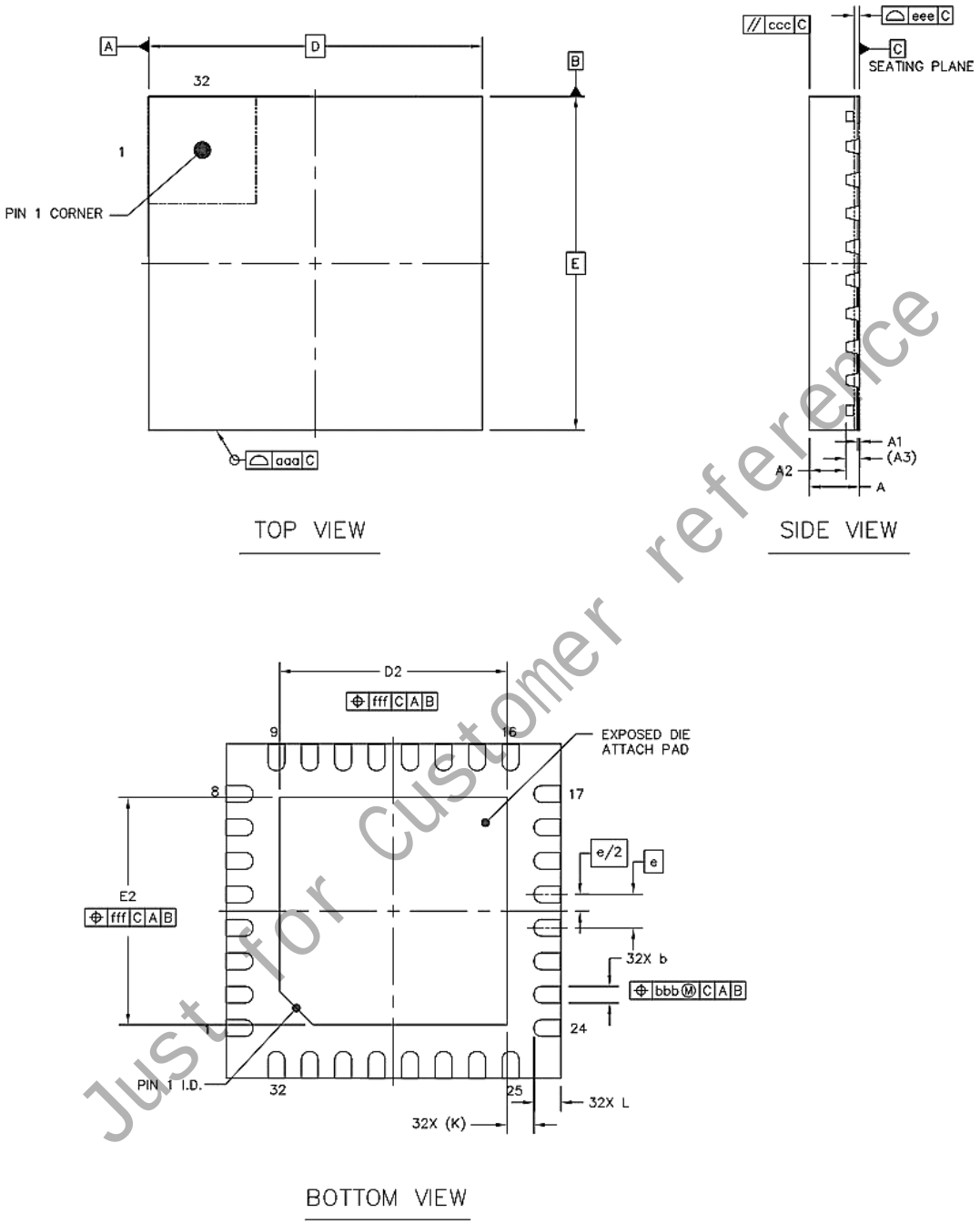


Figure 15. Mechanical Information

10. Ordering Information

Table 26. Ordering Information

Part Number	Grade	Package	Packaging	Status	Operation temp(℃)
YT8522C	Consumer	QFN 32 5x5mm			0 to 70 ℃
YT8522H	Industrial	QFN 32 5x5mm			–40 to 85 ℃