DSO311—High Performance All-silicon Oscillator

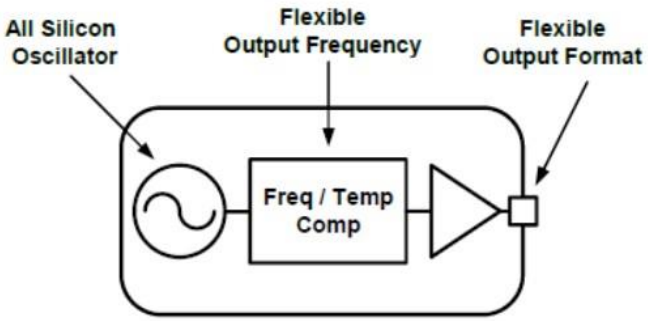
Key Features

- All-silicon without quartz and MEMS
- Total frequency stability ： ±50 ppm
- Single ended output：10 kHz ~ 212.5MHz
- Operating temperature ： -40℃~85℃
- Power supply：1.8V/2.5V/3.3V
- Output：CMOS
- Package：3225
- Low jitter: 350 fs Typ RMS (12 kHz – 20 MHz bandwidth)
- Built-in LDO and power filter circuit
- RoHS Compliant

Application

- Automotive electronics
- Intelligent terminal
- Ethernet
- Consumer electronics
- Communication equipment

Block Diagram



Overview

Dapu all silicon oscillator adopts unique frequency synthesis and sensor technology, which can output any clock from 10 kHz to 212.5 MHz without quartz and MEMS devices. The product can keep low jitter and frequency stability in the whole working range, and has high reliability in harsh environment and strong vibration.

Revision History

Version	Change Contents	Prepared by	Revised Date
V1.0.0	First Issued	Lin	2023.08.11

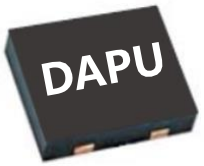
DAPU P/N: DSO311-32A-C13D-19M20000

Customer P/N: _____

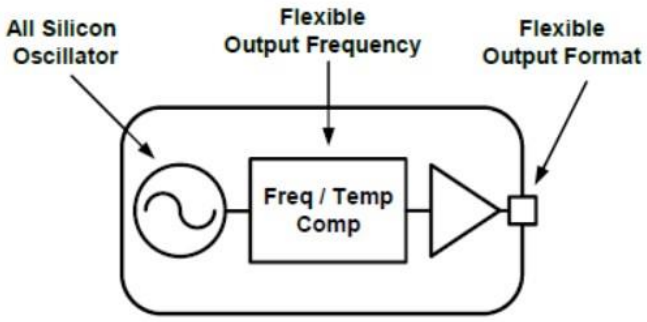
Index

1 Overview

DSO311 series all silicon oscillator is a clock free oscillator without quartz and MEMS devices. It is a high reliable clock oscillator which can still work normally under harsh environment and strong vibration. The device is factory-programmed to a fixedfrequency ranging from 10 kHz to 212.5 MHz with < 0.026 ppb resolution and maintains low jitter across its operating range. Thanks to the built-in temperature and stress sensors, the DSO311 all silicon oscillator can adapt to the harsh working environment. The built-in LDO and filter circuit greatly enhance the power supply noise suppression ability of the chip. Flexible clock frequency configuration provide maximum convenience for customer product design.



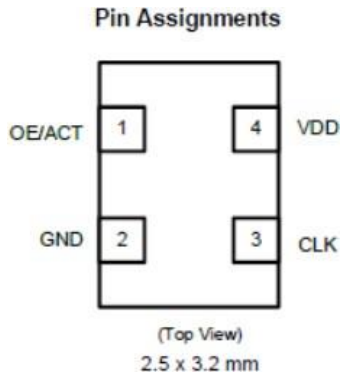
2 Block Diagram



3 Features

- All-silicon without quartz and MEMS
- Total frequency stability ： ±50 ppm
- Single ended output：10 kHz ~ 212.5MHz
- Operating temperature ： -40℃~85℃
- Power supply：1.8V/2.5V/3.3V
- Output：CMOS
- Package：3225
- Low jitter: 350 fs Typ RMS (12 kHz – 20 MHz bandwidth)
- Built-in LDO and power filter circuit
- RoHS Compliant

4 Pin Definition



PIN	Description
1	OE = Output Enable. Active High ACT = Device Active. Active High
2	GND = Ground
3	CLK=Clock output
4	VDD= Power supply

5 Electrical Specifications

Table 5.1 Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Unit
Operating Temperature	TA	-40 to 85	°C
Storage Temperature	T_S	-55 to 105	°C
Supply Voltage	V_{DD}	-0.5 to 3.8	V
Input Voltage	V_{IN}	-0.5 to V_{DD} + 0.3	V
ESD HBM (JESD22-A114)	HBM	4.0	kV
Solder Temperature[2]	T_{PEAK}	260	°C
Solder Time at T_{PEAK}[2]	T_P	20 - 40	sec

Notes:

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

2. The device is compliant with JEDEC J-STD-020.

Table 5.2 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition/Comment
Supply Voltage	V_{DD}	1.71	1.8	1.89	V	V_{DD} = 1.8 V
		2.375	2.5	2.625	V	V_{DD} = 2.5V
		3.135	3.3	3.47	V	V_{DD} = 3.3 V
Supply Current (F_{CLK} = 50 MHz)	I_{DD}		40	50	mA	Tristate Hi-Z (OE = 0, output disabled)
			1	2	mA	Ready State (ACT = 0, standby mode)
			40	55	mA	CMOS
Operating Temperature	TA	-40		85	℃	

Table5.3 Input Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition/Comment
Output Enable (OE)[1]	V_{IH}	0.7×V_{DD}			V	
	V_{IL}			0.3×V_{DD}	V	
	T_D			3	µs	Output Disable Time, F_{CLK} >10 MHz
	T_E			20	µs	Output Enable Time, F_{CLK} >10 MHz

Notes:

1.OE/ACT includes a 50 kΩ pull-up to V_{DD} for .OE/ACT active high. Includes a 50 kΩ pull-down to GND for.OE/ACT active low.

Table 5.4 Output Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition/Comment
Frequency Range	F_{CLK}	0.01		212.5	MHz	CMOS
Total Stability[1]	F_{STAB}	-50		50	ppm	Frequency stability
Rise/Fall Time (20% to 80% V_{PP})			0.5	1.5	ns	CMOS (C_L = 5 pF)
Powerup Time	t_{OSC}			4	ms	Time from 0.9 × V_{DD} until output frequency (F_{CLK}) within spec
Duty Cycle	DC	45		55	%	CMOS (CL = 5 pF)
CMOS Output Option	V_{OH}	0.83×V_{DD}			V	I_{OH} = 8/6/4 mA for 3.3/2.5/1.8V V_{DD}
	V_{OL}			0.17×V_{DD}	V	I_{OL} = 8/6/4 mA for 3.3/2.5/1.8V V_{DD}

Notes:

1.Total Stability, includes temperature stability, initial accuracy, load pulling, V_{DD} variation, and aging for 10 years at 40℃.

Table 5.5 Clock Output Phase Jitter and PSRR

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition/Comment
Phase Jitter (RMS, 12 kHz - 20 MHz)[1,2] $F_{CLK} \geq$ 10 MHz	ϕ_J		350		fs	CMOS
Spurs Induced by External Power Supply Noise, 50 mV_{pp} Ripple. CMOS 125 MHz Output V_{DD} = 1.8 V	PSRR		-76		dBc	100 kHz sine wave
			-75			200 kHz sine wave
			-75			500 kHz sine wave
			-75			1 MHz sine wave
Spurs Induced by External Power Supply Noise, 50 mV_{pp} Ripple. CMOS 125 MHz Output V_{DD} = 2.5 or 3.3 V	PSRR		83		dBc	100 kHz sine wave
			83			200 kHz sine wave
			83			500 kHz sine wave
			82			1 MHz sine wave

Notes:

1. Applies to output frequency: 50, 100, 125MHz.

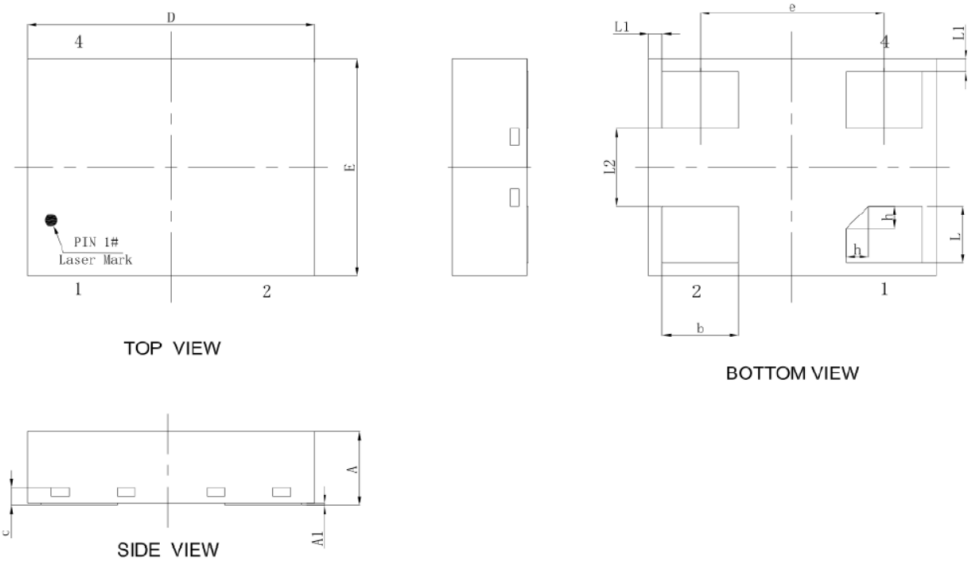
2. Guaranteed by characterization. Jitter inclusive of any spurs.

6 Environmental Conditions

Table 6.1. Environmental Conditions

Package	Symbol	Parameter	Test Condition	Value	Unit
	MSL	Moisture Sensitivity Level	1		
3225 4-pin DFN	Θ_{JA}	Thermal Resistance Junction to Ambient	Still Air	108	°C/W
	Θ_{JB}	Thermal Resistance Junction to Board	Still Air	84	°C/W
	T_J	Max Junction Temperature	Still Air	125	°C

7 Dimension and Pack



Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.80	0.85	0.90
c	0.203REF		
D	3.10	3.20	3.30
e	2.05BSC		
E	2.40	2.50	2.60

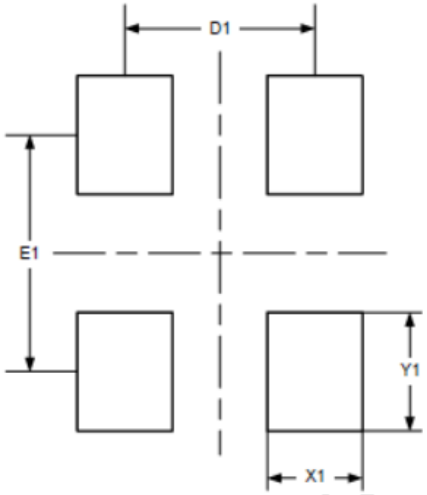
L	0.60	0.65	0.70
L1	0.10	0.15	0.20
L2	0.85	0.90	0.95
h	0.20	0.25	0.30

Notes:

1. The dimensions in parentheses are reference.
2. All dimensions in millimeters (mm).
3. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

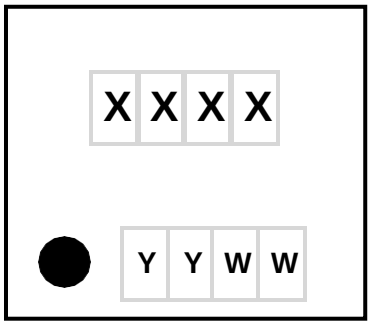
8 PCB

The figure below illustrates the PCB land pattern for the DSO311. The table below lists the values for the dimensions shown in the illustration.



Dimension	3225(mm)
X1	0.65
Y1	0.85
D1	1.55
E1	2.05

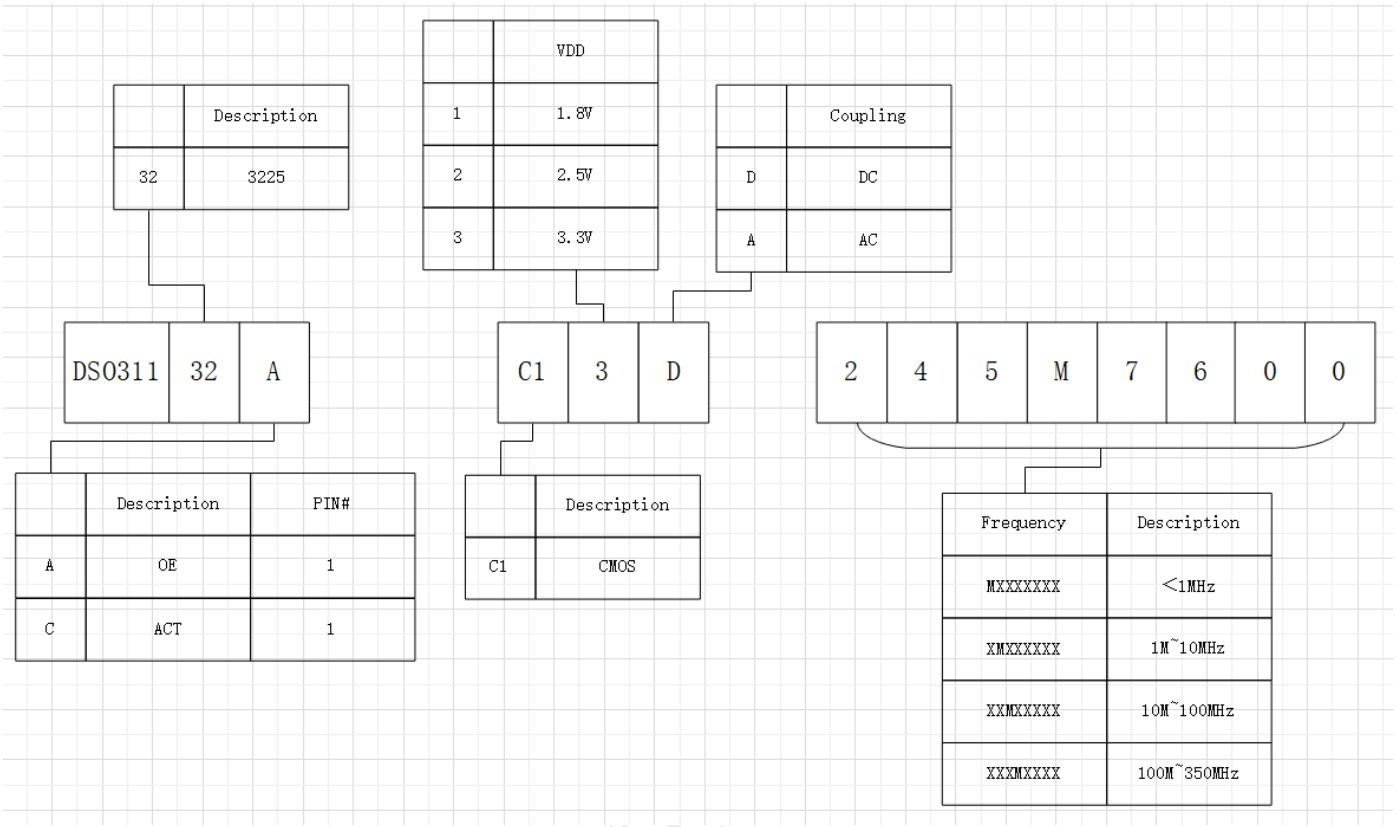
9 Marking



Line	Print	Description
1	XXXX	LOGO
2	YYWW	DATE

10 Ordering Guide

The naming rules and definitions of DSO311 are as follows:



Notes:

1. DSO311-32A-C13D-19M20000 means a silicon crystal with 3225 package, 1 pin defined as EN, input voltage 3.3V, output 19.2MHz DC-coupled CMOS signal.