Customer Code: _____

DATASHEET

DAPU P/N: **CM35P-S129-10.00Mhz-HHCv1**

Customer P/N: _____

DAPU			Customer Approval
Drew	Audited	Approved	
Amway.wei	Carry.Wang	Jason Zhao	
Date: 2021.09.03			Stamp, please! Thanks!

Guangdong Dapu Telecom Technology Co., Ltd

Building 5, No.24, Industrial East Road, Songshanhu Park, Dongguan, Guangdong, P.R. China

TEL：0086-0769-88010888 FAX：0086-0769-81800098

Building 5, No.24, Industrial East Road,
Songshanhu Park, Dongguan,
Guangdong, P.R. China
TEL:0086-0769-88010888
FAX:0086-0769-81800098

Table of Amendment

Version	Revision contents	Prepared by	Revised date
1.0	Based on CM35P-S129-10.00MHz V1.2，support SMPTE-2059	Amway	2021.09.03

Building 5, No.24, Industrial East Road,
Songshanhu Park, Dongguan,
Guangdong, P.R. China
TEL:0086-0769-88010888
FAX:0086-0769-81800098

Table of Content

Building 5, No.24, Industrial East Road,
Songshanhu Park, Dongguan,
Guangdong, P.R. China
TEL:0086-0769-88010888
FAX:0086-0769-81800098

1. General description

The figure below shows the CM35.

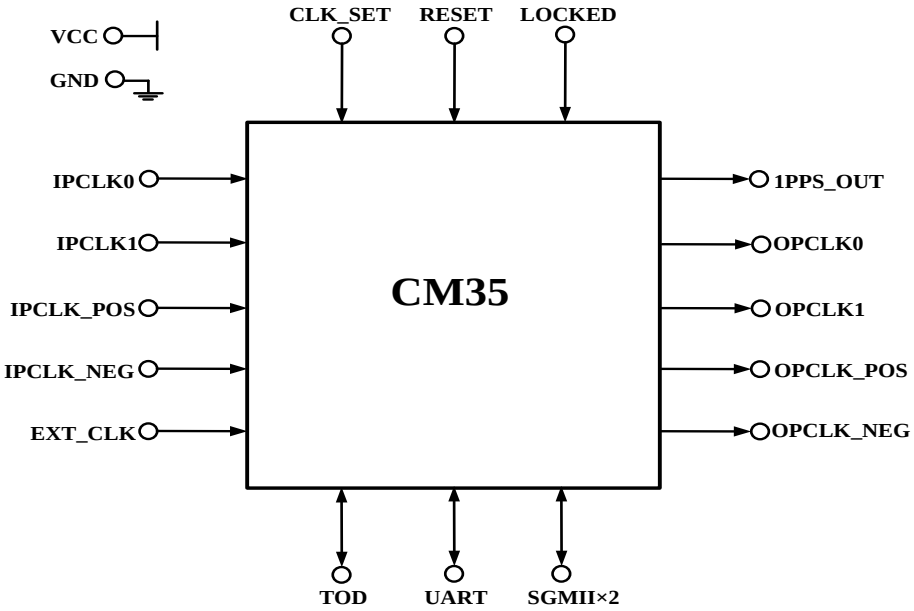

Figure 1 - CM35

1.1. About the CM35

The CM35 is a high-performance clock module designed to provide precise frequency, phase and time-of-day synchronization information for telecom and other applications. It combines the IEEE 1588-2008 (1588V2) with DAPU's advanced PTP IC and adaptive timing algorithms, which uses 1PPS retrieving from GNSS as a primary time reference. The module supports PTP Grandmaster, PTP Slave and BC.

1.2. Key features

- **Timebase derived from**: PTP slave, BITS/SSU input, GNSS timing satellite signal.
- **PTP Grandmaster**: PTP Grandmaster function supports multiple PTP slaves using multicast or unicast messaging. Timebase may be PTP or ARB.
- **PTP Slave**: Acting as a PTP Ordinary Clock in Slave mode, CM35 can lock to BCs, or it can use sophisticated packet delay filters and adaptation algorithms to lock to a remote PTP Grandmaster over a multi-hop legacy network which has no PTP support.
- **Time-aligned output pair**: 1 PPS and 125 MHz divided by n (n = 4 to 125000).
- **Frequency-aligned outputs**: 1 Hz and programmable frequency 1 kHz to 62.5MHz.
- **Supports ITU profiles**: G.8265.1, G.8275.1, and G.8275.2.
- **Supports SMPTE-2059**.
- **Clocks**: 3 clock inputs and 4 clock outputs.
- **Ports**: 2xSGMII and 2xUART (1xTOD).
- **Management Interface**: UART.

Building 5, No.24, Industrial East Road,
Songshanhu Park, Dongguan,
Guangdong, P.R. China
TEL:0086-0769-88010888
FAX:0086-0769-81800098

2. Pin description

The term “pin” used in the below table and throughout this document refers to one of the 48 edge castellation around the circumference of the CM35.

Pin 1 is located in the lower left corner mark point of the CM35, see Figure 4. The rest of the pins are enumerated counter-clockwise around the module from this pin.

The codes in the Type column below are: I for Input, O for Output, B for Bidirectional, P for Power.

Table 1 Pin Description

Pin group	Pin#	Pin name	Type	Description	
Supply Voltage	47,48	VCC	P	3V3 power supply	
	5,8,11,14,22,25, 28,31,34,41,45	GND	P	Ground	
Control and Alarm Pins	20	CLK_SEL	I	System clock select: 1: the system clock uses the local oscillator; 0: the system clock uses the external reference.	
	42	LOCKED	O	State output. Output high level when the CM is locked and stable, others low level.	
	46	RST	I	Reset the CM.	
SGMII Interface	9	SGMIITXP1	O	PTP port, SGMII interfaces.	
	10	SGMIITXN1	O		
	12	SGMIIRXP1	I		
	13	SGMIIRXN1	I		
	26	SGMIITXP0	O		
	27	SGMIITXN0	O		
	29	SGMIIRXP0	I		
	30	SGMIIRXN0	I		
UART	23	TOD0_RX	I	Time of day output /input	Asynchronous serial data output/input. 9600-N-8-1.
	24	TOD0_TX	O		
	39	UART0_RX	I	Configuration management	
	40	UART0_TX	O		

Input Clocks	43	IPCLK0	I	Single-ended input. Acceptable frequencies into the PTP module from: 1 PPS/1 Hz to 161MHz (input reference for PTP Master). The input frequencies must obey the following rule: Input Freq = k * 2^n, where 0 <= n <= 5 and 1 <= k <= 2^32 (upper limit of 170 MHz).
	44	IPCLK1	I	
	6	IPCLK_P	I	Differential input. TDM module only. Programmable input frequencies to a maximum of 155.52MHz. Default 19.44MHz. Default signal type LVDS.
	7	IPCLK_N	I	
Output Clocks	15	1PPS_OUT0	O	Pulses per second reference output.
	16	1PPS_OUT1	O	
	17	OPCLK0	O	Time-aligned output pair: 125 MHz divided by n (n = 4 to 125000); maximum of 25MHz MHz (divide by 4); minimum of 100 Hz (divide by 1249999). Frequency-aligned outputs: programmable frequency 1 kHz to 62.5MHz.
	18	OPCLK1	O	
	32	OPCLK_P	O	Differential output. Default frequency 77.76 MHz. Default signal type LVDS.
	33	OPCLK_N	O	
System Clock	21	EXT_CLK	I	External clock(support frequency 10MHz only) , back up for the local oscillator.
Reserve	1,2,3,4,19, 35,36,37,38	NC		Suspended, reserved.

3. Electrical Parameters

3.1. DC characteristics of the TTL ports

Table 2 DC characteristics of the TTL ports

Parameter	Symbol	Minimum	Typical	Maximum	Units
TTL input port					
V_{IN} High.	V_{IH}	2			V
V_{IN} Low.	V_{IL}			0.8	V
Input current.	I_{IN}			10	μA
TTL input port with internal pull-up					
V_{IN} High.	V_{IH}	2			V
V_{IN} Low.	V_{IL}			0.8	V
Pull-up resistor.	P_U	20		200	kΩ
Input current.	I_{IN}			100	μA
TTL input port with internal pull-down					

V_{IN} High.	V_{IH}	2			V
V_{IN} Low.	V_{IL}			0.8	V
Pull-down resistor.	P_D	20		200	kΩ
Input current.	I_{IN}			100	μA
TTL output port (OPCLK, 1PPSOUT)					
V_{OUT} Low (I_{OL} = 8 mA).	V_{OL}	0		0.4	V
V_{OUT} High (I_{OH}= 8 mA).	V_{OH}	2.4			V
Drive current.	I_D	-8		8	mA
TTL output port (other pins)					
V_{OUT} Low (I_{OL} = 4 mA).	V_{OL}	0		0.4	V
V_{OUT} High (I_{OH}= 4 mA).	V_{OH}	2.4			V
Drive current.	I_D			4	mA

3.2. DC characteristics of the LVDS ports

Table 3 DC characteristics of the LVDS ports

Parameter	Symbol	Minimum	Typical	Maximum	Units
LVDS input voltage range. Differential input voltage = 100 mV.	V_{VRLVDS}	0		2.4	V
LVDS differential input threshold.	V_{DITH}	-100		100	mV
LVDS input differential voltage.	$V_{IDLVTSDS}$	0.1		1.4	V
LVDS input termination resistance.	R_{TERM}	95	100	105	Ω
LVDS output high voltage.	V_{OHLVDS}			1.585	V
LVDS output low voltage.	V_{OLLVDS}	0.885			V
LVDS differential output voltage.	V_{ODLVDS}	250		450	mV
LVDS change in magnitude of differential output voltage for complementary states.	$V_{DOSLVDS}$			25	mV
LVDS output offset voltage. Temperature = 25℃	V_{OSLVD}	1.125		1.375	V

3.3. SGMII interface

The CM35 has two serial SGMII interfaces running with a 100 Mbps data rate and a 1.25Gbps line rate. The interfaces are IEEE 802.3 compliant for communication via a suitable packet PHY.

Table 4 SGMII output data AC characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Serial data rate	DR		1.25		Gbits/sec
Vod fall time (80% to 20%)	t_{FALL}	100		200	picosec
Vod rise time (20% to 80%)	t_{RISE}	100		200	picosec
Skew between two members of a differential pair:[tp_{HLP}- tp_{LHN}] or [tp_{LHP}- tp_{HLN}]	t_{SKEW}			±20	picosec

Table 5 SGMII output data DC characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Output voltage high state	V_{OH}			1525	mV
Output voltage low state	V_{OL}	875			mV
Output differential voltage	V_{OD}	150		400	mV

Table 6 SGMII input data AC characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Serial input data rate tolerance	D_{RT}	-300		+300	ppm

Table 7 SGMII input data DC characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input voltage range	V_I	675		1725	mV
Input differential threshold	V_{IDTH}	50		400	mV
Input differential voltage	V_{OD}	150		400	mV
Differential input impedance	R_{IN}	80		120	Ω

4. Performance

Table 8 Performance

Recovery Precision	**Recovery time**	**Minimum**	**Typical**	**Maximum**	**Units**	**Test Condition**
	24 Hours	-50		+50	ns	△T=±5℃，Test after Power on 30 min.
Holdover Capability	**Holdover time**	**Minimum**	**Typical**	**Maximum**	**Units**	**Test Condition**
	8Hours	-1.5		1.5	us	△T=±5℃，Test after Power on and lock 2 days.
			NA			Supports external clock with advanced holdover compensation algorithm
Power Supply	**Parameters**	**Minimum**	**Typical**	**Maximum**	**Units**	**Test Condition**
	Supply Voltage	3.13	3.3	3.47	V	
	Current Consumption (local oscillator)			2000	mA	During Warm-up
				1000	mA	During steady state operation @25℃
	Current Consumption (external reference)			1000	mA	During Warm-up
				1000	mA	During steady state operation @25℃
	AC Ripple			50	mVpk-pk	10Hz to 1MHz

5. UART

The UART is used for configuration management, which has a fixed baud rate (9600) using 1 stop bit and no parity. It is a LVTTL-compatible port and needs an external translator to work with other signal types (such as RS-232C or RS-485).

6. Time of day

A TOD port is used in PTP Timing modes only. In PTP GM mode, the port is an input comprising UARTRX and a 1 PPS signal. In PTP Slave mode, the port is an output comprising UARTTX and a PPnS signal, which gives a pulse every n seconds (t_W configurable for a minimum of 100 ns to a maximum of 400 ms). The UART has a fixed baud rate(9600) using 1 stop bit and no parity.

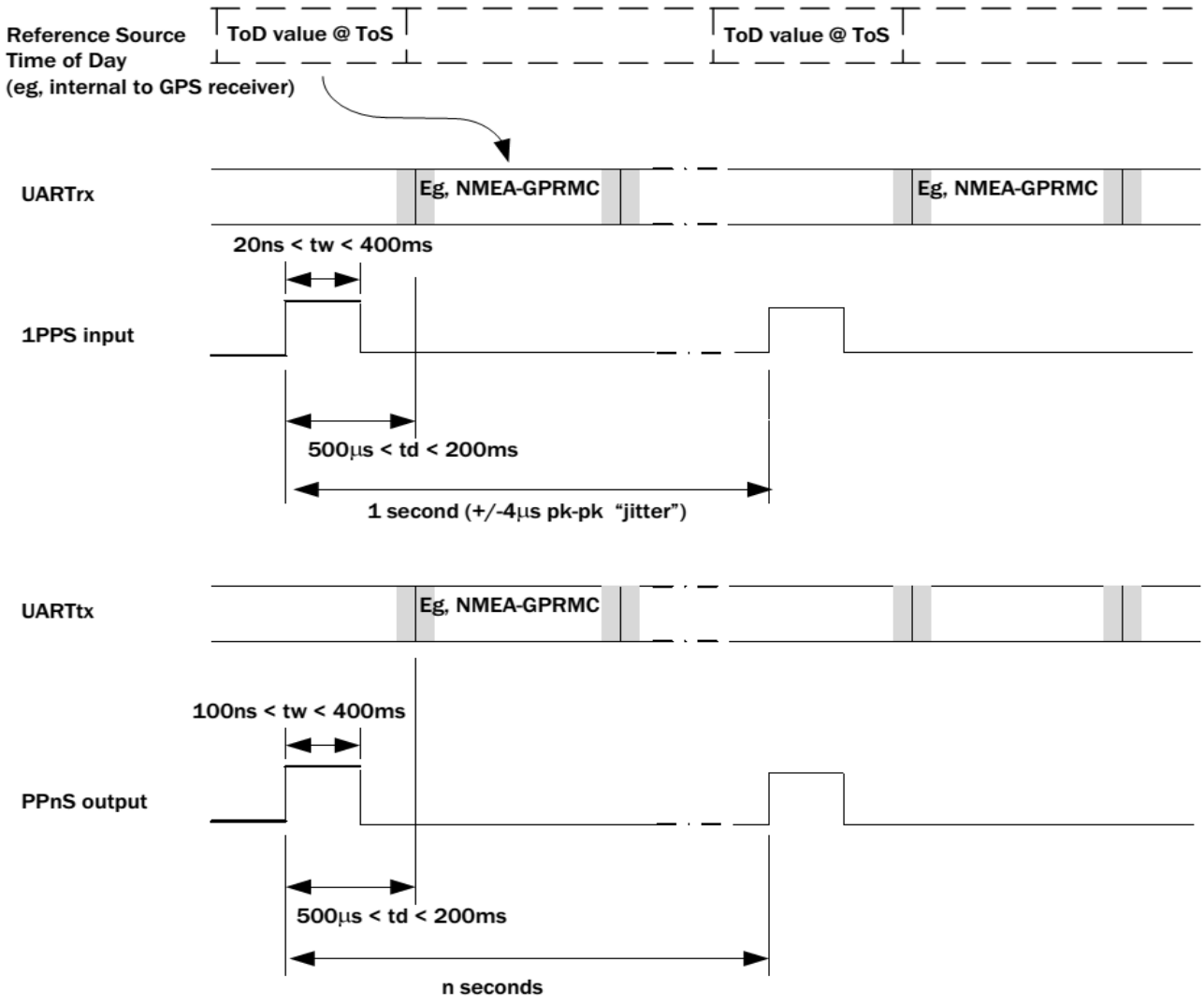

Figure 2 - TOD port timing

A TOD message format can be a GPRMC message or one of a group of other GPS messages or proprietary messages to suit specific causes.

A GPRMC message has the format $GPRMC,122356, A,0000.0000, N,00000.0000, W,0.0.0.0,120508,,,A*F6 in which the commas are separators. The architecture of the message is shown in Table 18. The message is 62

characters in length (i.e. 62 bytes). No parity bit is used, but each byte has a stop bit.

Table 9 Architecture of GPRMC message

Elements	Description
$GPRMC	Message header.
122356	UTC value.
A	Status (A = active, V = void).
0000.0000,N	Latitude, north (fixed to zero).
00000.0000,W	Longitude, west (fixed to zero).
0.0	Speed over ground (fixed to zero).
0.0	Track angle (fixed to zero).
120508	Date (ddmmyy).
A	A = autonomous, D = differential, E = estimated, S = simulation, N = not valid.
*F6	Checksum.

7. Jitter tolerance of the 1PPS input

The CM35 will reject a 1PPS signal if the jitter is greater than 4 μs peak-to-peak. However, it is strongly recommended that jitter on this signal is avoided as much as possible because the distribution of jitter on this signal is not known and so cannot be correctly attenuated by filtering. Any filtering applied to this signal will introduce a phase offset error. This treatment differs from that of more traditional reference sources because the phase of a 1PPS signal, relative to a recognized source of time such as UTC, is the parameter of most significance. For other references, the rate (frequency) is the more significant parameter.

8. Reset

Reset the CM (active low). Must be set low level for 2us (Min.). If Reset is forced low, all internal states are reset to default values.

9. Locked status

High level indicates that the device has achieved lock to the selected reference. The degree of lock indicated is software defined. The LOCKED pin is used in PTP only.

Building 5, No.24, Industrial East Road,
Songshanhu Park, Dongguan,
Guangdong, P.R. China
TEL:0086-0769-88010888
FAX:0086-0769-81800098

10. Environmental Conditions

Table 10 Environmental Conditions

Parameter	Conditions	
Operating Temperature	-20℃ to +75℃	
Storage Temperature	-55℃ to +105℃	
Storage Humidity	30%~80%	
ESD Level	Human Body Model, class2: 2000V to 4000V; ANSI/ESDA/JEDEC JS-001-2010.	
	Machine Model, class B: 200V to 400V; JEDEC JESD22-A115C.	
Moisture Sensitivity Level	Not humidity sensitive.	
Vibration	Test Condition: 0.75mm ;acceleration:10g;10Hz～500Hz, one cycle per 30 min, test 2 hour. (3 times for each 3 directions X ,Y , Z)，IEC 68-2-06 Test Fc.	
Shock	50g；11ms；half sine wave (3 times for each 3 directions X ,Y, Z),IEC 68-2-27 Test Ea/Severity 50A.	
Relative Humidity	20%～70%	Full Package Storage
Temperature	-10℃~35℃	

11. Typical Application

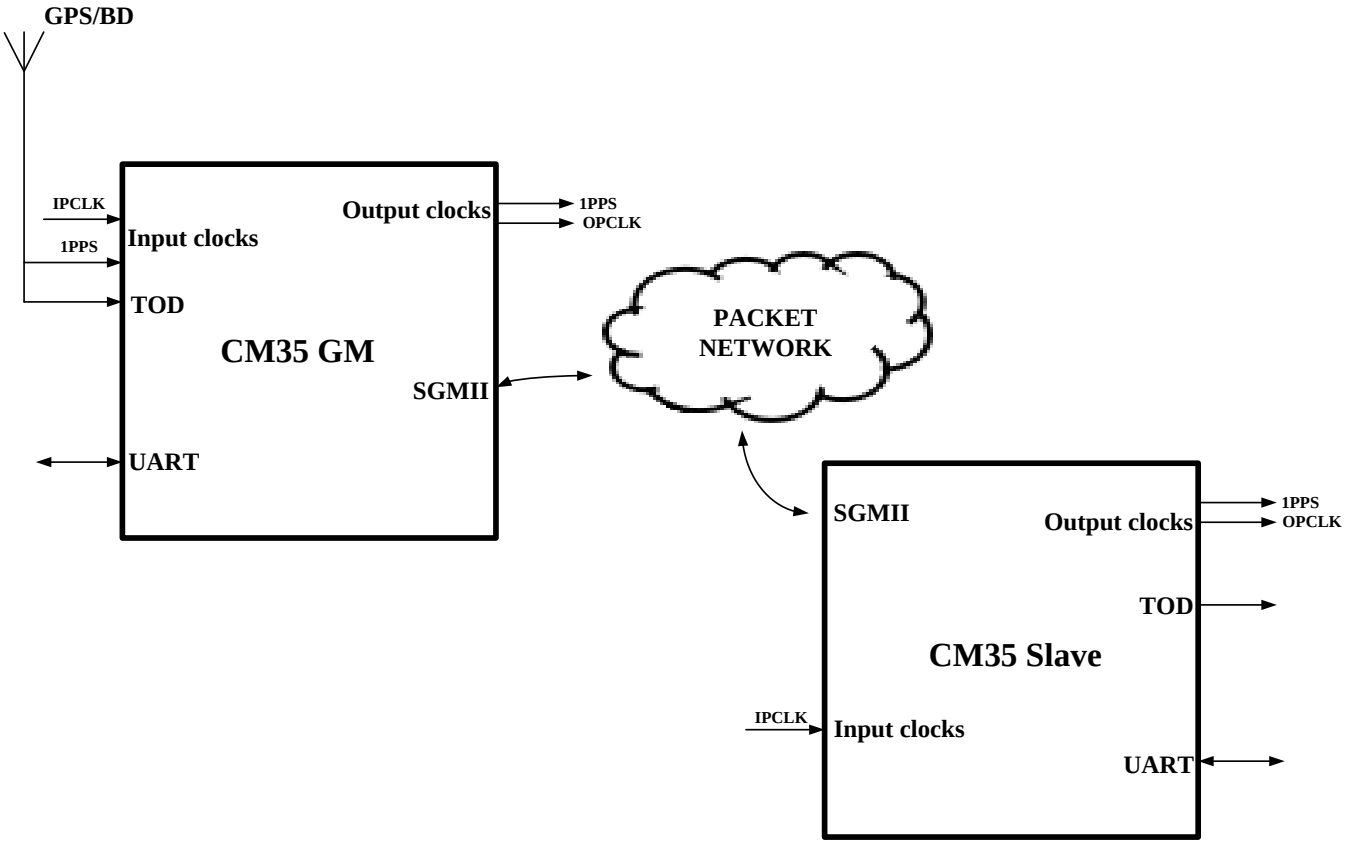

Figure 3 - CM35 in PTP GM and Slave modes

12. Mechanical Structure

Unit: mm

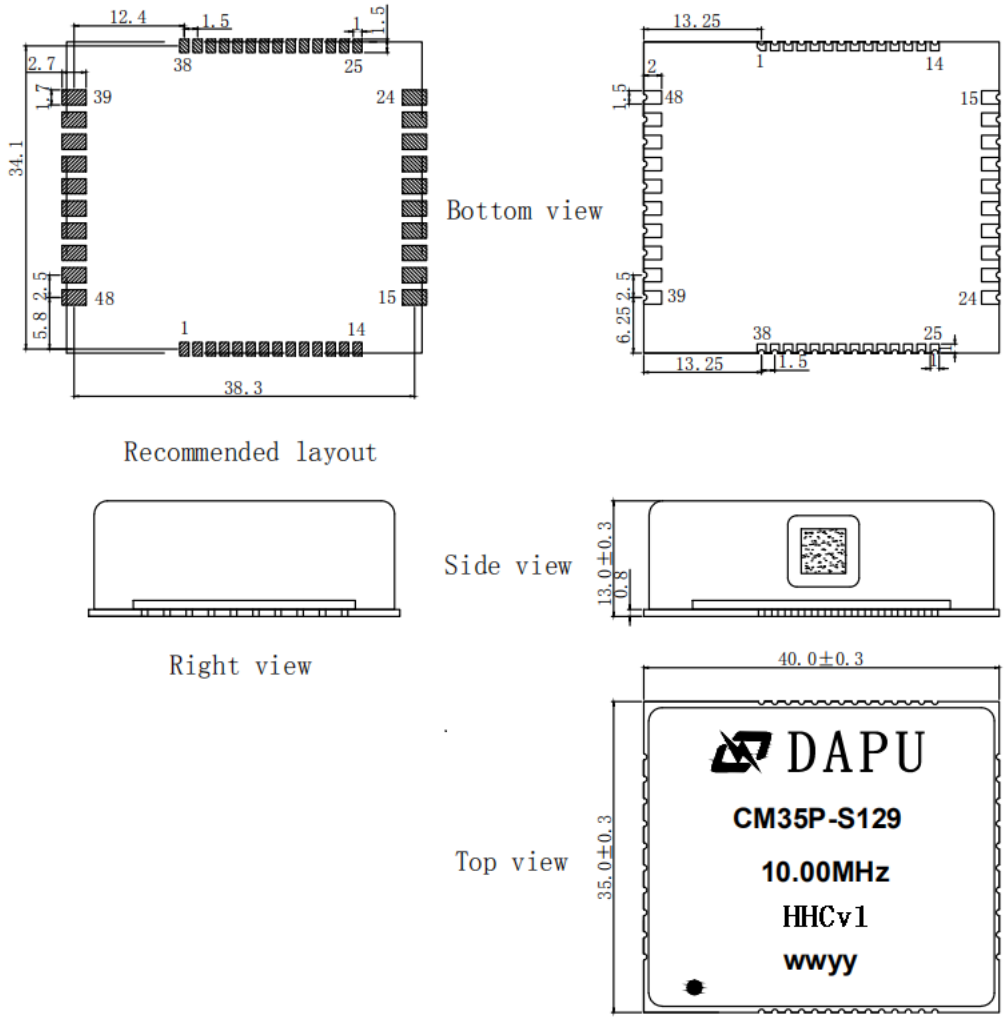

Figure 4 - Mechanical structure

Note1: Tolerance ± 0.2mm without mark.
The height of connector is optional.

Note2: The first two ww representative: week.
The last two yy representative: year.

13. Package

Unit: mm

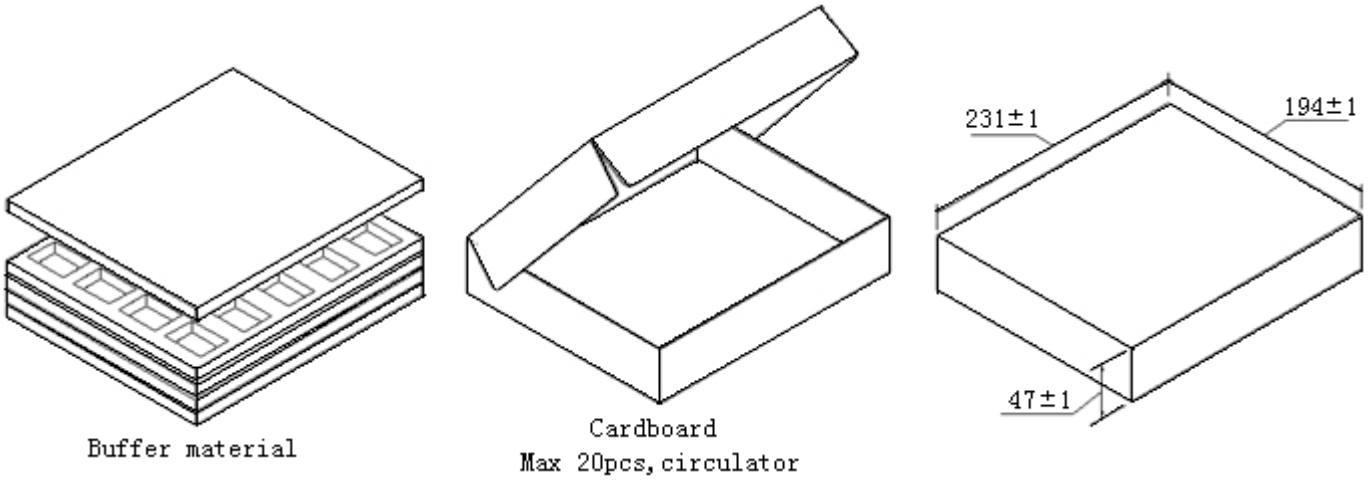

Figure 5 – Package

14. Reflow Soldering Curve (RoHS)

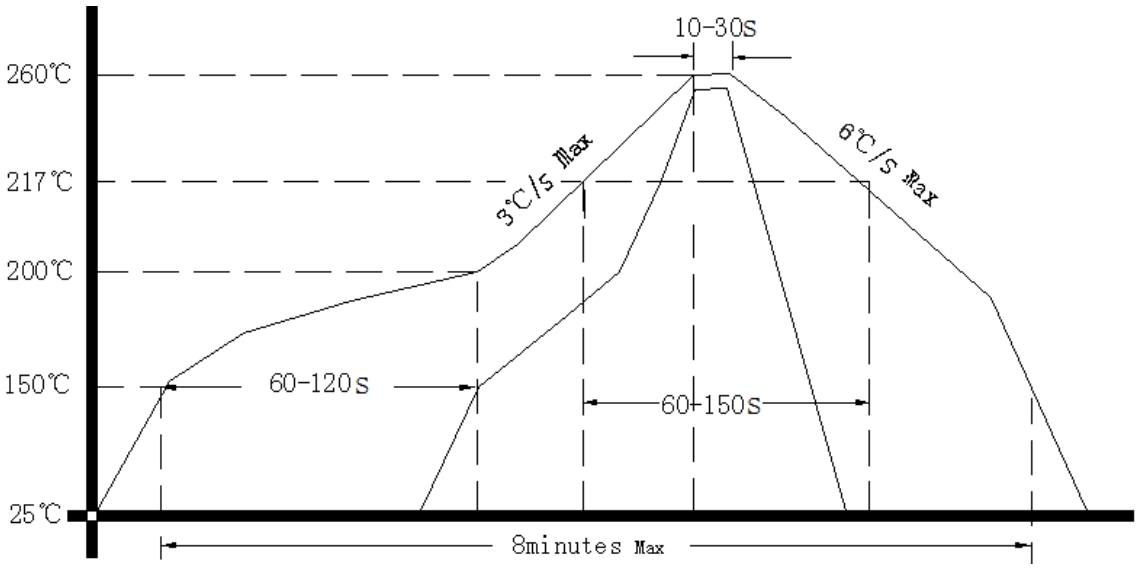

Figure 6 Reflow Soldering Curve