# ABOUT THE ACS9528

This is the datasheet for the DPSync ASSP ACS9528.

The ACS9528 is a fully-integrated, single-chip, IEEE 1588-2008 (Precision Time Protocol) master. With the addition of an external oscillator and a time-of-day source, such as a GPS receiver, a full-featured PTP master can be implemented.

The datasheet should be read in conjunction with the ACS9528 user guide, API documentation and other information available at the DPSync Resource Center[1].

The ACS9528 features two separate PTP master blocks, driven from a common timebase, and two independent SGMII Ethernet ports. Each master block can be associated with either SGMII port for maximum flexibility. The master blocks can be individually configured to support different operating parameters of PTP, such as layer 2 (Ethernet) or layer 3 (UDP/IP), different PTP domains and one or two-step operation. Each SGMII port has individually programmable Ethernet MAC and IP addresses. By associating both master blocks to a single SGMII port, both layer 2 and layer 3 master functionality can be provided on one port.

To maximize precision and eliminate delay variation internal to the system. support for external timestamping is provided. This takes advantage of the timestamping capability built into many newer Ethernet phys and switches to allow packet ingress and egress timestamping to occur as close to the edge of the system as possible.

As well as synchronizing internal operation, the local reference oscillator can be used to provide a holdover capability in the event of the external references failing. The holdover performance is determined directly by the stability of the local oscillator, which will typically need to be a temperature-compensated or oven-controlled part if holdover capability is required.

Control of the ACS9528 can be performed over an SPI port, or the provided Windows-based GUI can be used in conjunction with the configurable plug-and-play mode to allow autonomous operation directly from reset. Since the ACS9528 contains a powerful in-built CPU complete with RAM and Flash memory, no real-time external CPU power is needed for normal operation.

# FEATURES

- Part of DAPU's market-leading DPSync device family
- Field-proven performance
- Complete dual IEEE1588-2008 master function in a single device
- Ideal for applications such as:
  - PTP grandmaster
  - xPON ONU
  - Wireless backhaul aggregator
- Suitable for delivery of time-of-day or frequency
- 1PPS and NMEA serial port for interfacing to common GPS receivers
- Dual frequency inputs up to 160 MHz for received Synchronous Ethernet clock
- Can be used as reference for frequency-only delivery or to provide holdover stability
- Layer 2 or layer 3 operation
- Simultaneous multicast and unicast operation
- One or two-step PTP Sync messages
- Operates at up to 128 packets per second
- Supports up to 1024 slave devices
  - 1024 at 8 pkts/sec
  - 512 at 16 pkts/sec
  - 256 at 8pkts/sec
- Acceptable slave table (Restricts operation to known slaves)
- Support for external timestamping
- SPI interface for control
- Dual SGMII Ethernet interfaces
- DAPU-provided Windows GUI ( Can ease initial bring-up effort and reduce time-to-market ).
- Configurable plug-and-play option allows autonomous operation from reset
- Works with 10, 12.8 or 20 MHz local oscillator
- Master $I^2C$ port to control companion ACS1790 (For Synchronous Ethernet clocking)
- 324 ball, 19 x 19 mm, 1 mm pitch LBGA
- 3.3V and 1.2V power supplies
- Power consumption less than 0.5W typical
- Operating temperature – -40°C to +85°C
- Fully RoHS (6 of 6) and WEEE compliant

# System diagram

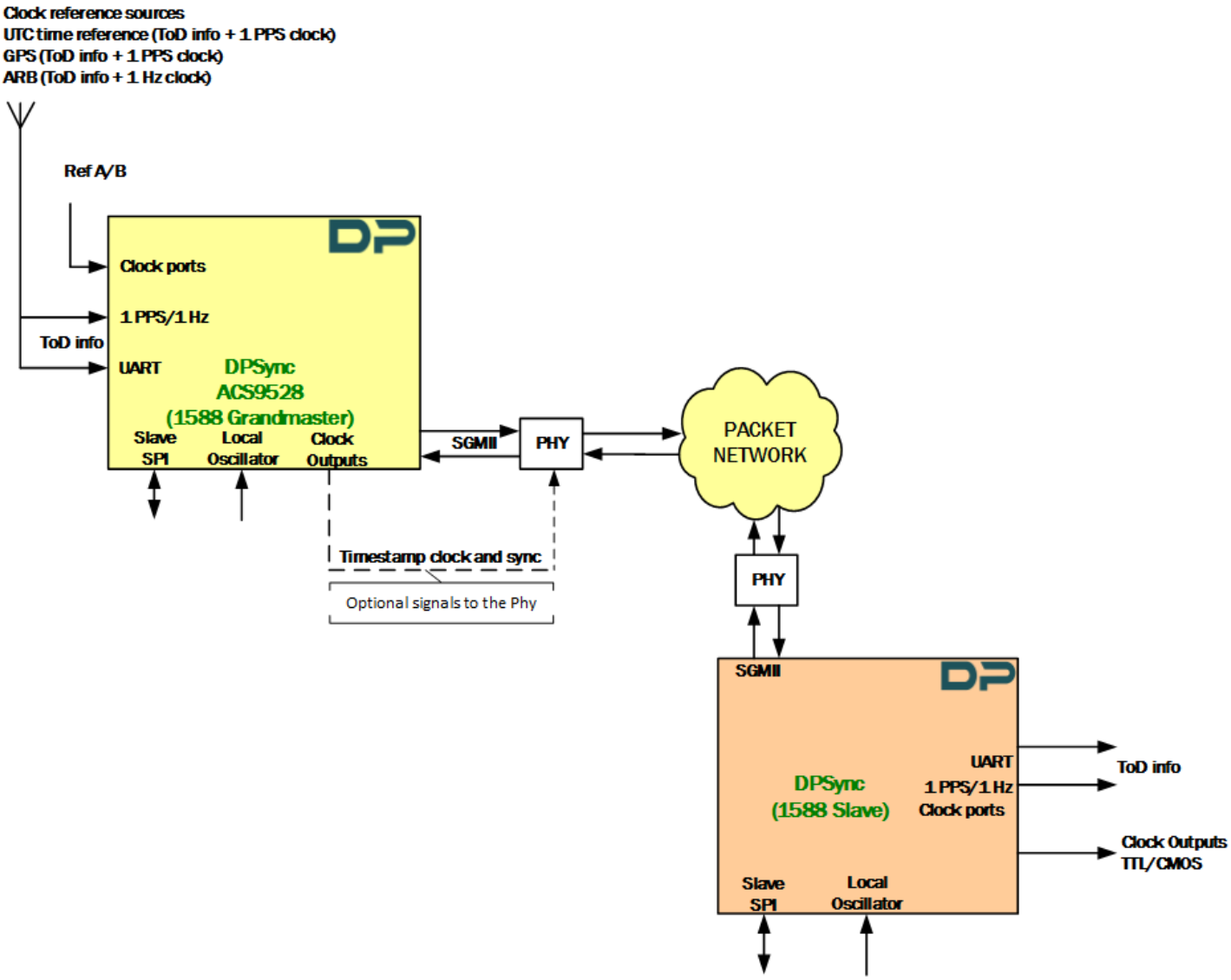


*Figure 1 - Simplified system diagram - ACS9528 Grandmaster and DPSync Slave*

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# PIN DIAGRAM

Figure 2 shows the pinout arrangement of the ACS9528. Click on a pad for more detailed information.

Pins of the same color in Figure 2 may be grouped into buses in the Boundary Scan Description Language (BSDL) file.

| | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSSVSS | IC 04 | NC | NC | NC | IC 03 | NC | NC | NC | NC | NC | NC | NC | IC 02 | IC 01 | VSS | VSS | VSS |
| B | VSSVSS | VDDIO | VDDIO | VDDIO | VDDIO | VDDIO | VDDIO | NC | NC | NC | NC | NC | VSS | VSS | VSS | VSS | VDDIO | VSS |
| C | VSSVSSVSS | VSS | VSS | VSS | VSS | VSS | VDDIO | IC 05 | REFCLK | NC | NC | NC | VSS | VSS | VSS | VSS | VDDIO | SGMIICLKP |
| D | VDDIO | VSS | VSS | VSS | VSS | VSS | VDDIO | IPCLK1 | IC62 | IC64 | IC 06 | NC | VSS | VSS | VSS | VSS | VDDIO | SGMIICLKN |
| E | VDDIO | VSS | VSS | VSS | VSS | VSS | VDDIO | IPCLK0 | IPCLK2 | IC60 | IC 09 | IC65 | VSS | VSS | VSS | IC 08 | IC 07 | SGMIICLK |
| F | VDDIO | VSS | VSS | VSS | VSS | VSS | VDDIO | IC63 | IC61 | LOCKED | SGMIICLKSEL | IC68 | VDDIO | VDDIO | IC 11 | NC | IC 10 | VSS |
| G | NC | NC | NC | VDDIO | VDDIO | IC 15 | VDDIO | SYSMODE0 | IC 14 | IC 13 | SYSMODE1 | IC53 | VDDIO | VDDIO | VDDIO | IC 12 | VDDASGMIITX1 | VSS |
| H | NC | NC | NC | IC 20 | IC 19 | IC 18 | NC | VDDIO | PORB | ALARM | SLVINT | TRST | VDDIO | VDDIO | IC 17 | IC 16 | VDDHASGMIITX1 | TX1POS |
| J | NC | NC | NC | IC 22 | VDDIO | IC 21 | TDI | VSS | VSS | SLVCSB | VDDCORE | OSCFSEL1 | VDDCORE | VDDCORE | VDDCORE | VSSSGMII1 | VDDHASGMIIRX1 | TX1NEG |
| K | NC | NC | NC | NC | NC | IC 23 | SCL | VDDIO | VDDIO | SLVMISO | SDA | VDDIO | VDDIO | VDDIO | VSSSGMII1 | VDDSGMII1 | VDDASGMIIRX1 | RX1POS |
| L | NC | NC | VSS | VSS | VSS | VSS | NC | VSS | SLVCFGSPI | VDDCORE | VSS | VSS | VSS | VSS | VSS | VSSSGMII0 | VDDASGMIIRX0 | RX1NEG |
| M | NC | NC | NC | VSS | VSS | VSS | OSCFSEL0 | VSS | SLVCFGCLKE | SLVSCLK | VSS | VSS | VSS | VSS | VSS | VDDSGMII0 | VDDHASGMIIRX0 | RXONEG |
| N | NC | NC | NC | VSS | VSS | VSS | IC 25 | IC 24 | VDDIO | VSS | VSS | VSS | VSS | VSS | VSS | VSSSGMII0 | VDDHASGMIITX0 | RXOPOS |
| P | NC | NC | NC | VSS | VSS | NC | NC | PPNS0 | VDDIO | IC 26 | VDDIO | VDDCORE | VDDIO | VDDCORE | VDDIO | GNDCMU | VDDASGMIITX0 | TXONEG |
| R | NC | IC 30 | NC | VSS | VSS | NC | IC 29 | OPCLK0 | IC54 | IC 28 | IC 27 | VDDCORE | MDC | VDDCORE | UARTRX0 | VDDIO | IC58 | TXOPOS |
| T | NC | IC 37 | VSS | VSS | VSS | VSS | IC 36 | IC66 | IC55 | IC 35 | SLVMOSI | IC 34 | IC 33 | IC 32 | IC69 | IC 31 | VDDCMUD | VDDCMUD |
| U | NC | NC | TDO | IC 44 | NC | NC | NC | IC67 | IC 43 | IC 42 | IC56 | IC 41 | IC 40 | IC 39 | VDDIO | IC 38 | VDDCMU | VDDCMU |
| V | VSS | NC | TCK | IC 52 | TMS | NC | IC 51 | VDDIO | IC57 | IC 50 | IC 49 | IC 48 | IC 47 | IC 46 | MDIO | IC 45 | IC59 | VSS |

JTAG Control/alarms SGMII ToD I²C Input clocks

Output clocks SPI Power Ground Internally connected

Not connected

***Figure 2 - ACS9528 pin diagram (as viewed from the underside of the device)***

# Pin descriptions

This section contains tables of descriptions in which the details of every pin of the ACS9528 are declared.

In the pin description tables, the following acronyms appear in the I/O column:

I = input.
O = output.
I/O = bi-directional.

The following acronyms appear in the Signal Type column:

P = power.
G = ground.

$TTL^U$ = TTL input with internal pull-up resistor greater than 20 kΩ.

$TTL_D$ = TTL input with internal pull-down resistor greater than 20 kΩ.

*NOTE: All pins are 5 V tolerant except where stated otherwise.*

***Table 1 JTAG interface***

| Pin | Symbol | I/O | Signal type | Description |
|---|---|---|---|---|
| J12 | TDI | I | $TTL^U$ | Boundary scan serial test data input<br>Sampled on rising edge of TCK. |
| V14 | TMS | I | $TTL^U$ | Boundary scan test mode select.<br>Sampled on rising edge of TCK.<br>If not used, connect to $V_{DD}$ or leave floating. |
| V16 | TCK | I | TTL | Boundary scan test clock input. |
| U16 | TDO | O | TTL | Boundary scan serial test data output.<br>Sampled on rising edge of TCK. |
| H7 | TRST | I | $TTL_D$ | Test reset input.<br>0 = boundary scan standby mode, allowing correct device operation.<br>1 = enable JTAG boundary scan mode.<br>If not used, connect to GND or leave floating. |

*Table 2 Control and alarm pins*

| Pin | Symbol | I/O | Signal type | Description |
|---|---|---|---|---|
| H10 | PORB | I | $TTL^U$ | Power-on master reset (active-low).<br>0 = all internal states reset to default values.<br>1 = not reset. |
| F9 | LOCKED | O | TTL/CMOS | Device locked status pin:<br>0 = ACS9528 not in lock.<br>1 = ACS9528 in lock. |
| H9 | ALARM | O | $TTL^U/CMOS^U$ | Use subject to firmware version.<br>If not used, leave to float. |
| J7 | OSCFSEL1 | I | $TTL_D$ | Oscillator frequency select pins, which set the expected local oscillator frequency. |
| M12 | OSCFSEL0 | I | $TTL_D$ | |

*Table 3 SGMII interface*

| Pin | Symbol | I/O | Signal type | Description |
|---|---|---|---|---|
| R1 | TX0POS | O | LVDS | SGMII Port 0, TX data output. |
| P1 | TX0NEG | | | |
| N1 | RX0POS | I | LVDS | SGMII Port 0, RX data input. |
| M1 | RX0NEG | | | |
| H1 | TX1POS | O | LVDS | SGMII Port 1, TX data output. |
| J1 | TX1NEG | | | |
| K1 | RX1POS | I | LVDS | SGMII Port 1, RX data input. |
| L1 | RX1NEG | | | |
| C1 | SGMIICLKP | I | LVDS | 125 MHz clock input to the SGMII PLL. |
| D1 | SGMIICLKN | | | |
| E1 | SGMIICLK | I | TTL/CMOS | SGMII clock input. Maximum frequency 125 MHz + 100 ppm. |
| F8 | SGMIICLKSEL | I | $TTL^U/CMOS^U$ | SGMII clock select input.<br>Pull low for differential clock. Leave unconnected for single-ended clock. |
| R6 | MDC | O | TTL | MII clock. |
| V4 | MDIO | I/O | TTL | MII data input/output. |

The pins of the SGMII interface are not 5 V tolerant.

*NOTE: The SGMII data TX and RX differential pairs have 100 Ω resistors across them. External resistors are unnecessary.*

*Table 4 Time of day ports*

| Pin | Symbol | I/O | Signal type | Description |
|---|---|---|---|---|
| R4 | UARTRX0 | I | $TTL_D$ | ToD receive data. |

*Table 5 Configuration pins*

| Pin | Symbol | I/O | Signal type | Description |
|---|---|---|---|---|
| G11 | SYSMODE0 | I | $TTL_D$ | Operating mode selection signal, bit 0. |
| G8 | SYSMODE1 | I | $TTL_D$ | Operating mode selection signal, bit 1. |

*Table 6 Input reference clocks (IPCLK0 to IPCLK7 are not 5 V tolerant and must be pulled low if not used)*

| Pin | Symbol | I/O | Signal type | Description |
|---|---|---|---|---|
| E11 | IPCLK0 | I | TTL | Clock reference input 0.<br>Default: 1 PPS |
| D11 | IPCLK1 | I | TTL | Clock reference input 1.<br>Default: SyncE A |
| E10 | IPCLK2 | I | TTL | Clock reference input 2.<br>Default: SyncE B |

*Table 7 Output reference clocks*

| Pin | Symbol | I/O | Signal type | Description |
|---|---|---|---|---|
| R11 | OPCLK0 | O | TTL/CMOS | Clock reference Output<br>Default: Timestamp clock |

*Table 8 PPnS*

| Pin | Symbol | I/O | Signal type | Description |
|---|---|---|---|---|
| P11 | PPNS0 | O | TTL/CMOS | Timestamp Sync.<br>Pulses per n second reference output. Default 1 pps.<br>Fully programmable high time: default 100 ms. [1]<br>Rising edge specifies seconds rollover. |

1. May vary with software revision.

*Table 9 Serial interfaces*

| Pin | Symbol | I/O | Signal type | Description |
|---|---|---|---|---|
| Slave SPI | | | | |
| K9 | SLVMISO | O | TTL/CMOS | Master in/slave out data output. |
| T8 | SLVMOSI | I | $TTL_D$ | Master out/slave in data input. |
| M9 | SLVSCLK | I | $TTL_D$ | Slave mode serial clock. |
| J9 | SLVCSB | I | $TTL^U$ | Chip select (slave):<br>0 = slave serial interface enabled.<br>1 = slave serial interface disabled.<br>Asserted by the microprocessor. |
| H8 | SLVINT | O | TTL/CMOS | Slave interrupt output:<br>0 = no interrupt.<br>1 = interrupt. |
| M10 | SLVCFGCLKE | I | $TTL_D$ | Clock control for slave serial interface:<br>0 = sampling of SLVMOSI occurs on the rising edge and clocking out of SLVMISO occurs on the falling edge of SLVSCLK.<br>1 = sampling of SLVMOSI occurs on the falling edge and clocking out of SLVMISO occurs on the rising edge of SLVSCLK. |
| L10 | SLVCFGSPI | I | $TTL_D$ | For future use. Must be fitted with a 10 kΩ pull-down resistor. |
| $I^2C$ | | | | |
| K12 | SCL | O | CMOS open drain | $I^2C$ SCL for the interface to ACS1790. |
| K8 | SDA | I/O | CMOS open drain | $I^2C$ SDA for the interface to ACS1790. |

*Table 10 System clocks*

| Pin | Symbol | I/O | Signal type | Description |
|---|---|---|---|---|
| Local oscillator | | | | |
| C10 | REFCLK | I | TTL | Input for local oscillator in normal operating mode.<br>Expected input frequency set by OSC_SEL[1:0]. |

If REFCLK is not supplied by a good quality oscillator, the ACS9528 will still operate but holdover quality may be seriously compromised.

*Table 11 Power supply pins*

| Pin | Symbol | Description |
|---|---|---|
| L2 | VDDASGMIIRX0 | 1.2 V SGMII RX analogue supply. |
| P2 | VDDASGMIITX0 | 1.2 V SGMII TX analogue supply. |
| M2 | VDDHASGMIIRX0 | 3.3 V SGMII RX analogue supply. |
| N2 | VDDHASGMIITX0 | 3.3 V SGMII TX analogue supply. |
| M3 | VDDSGMII0 | 1.2 V SGMII digital supply. |
| K2 | VDDASGMIIRX1 | 1.2 V SGMII RX analogue supply. |
| G2 | VDDASGMIITX1 | 1.2 V SGMII TX analogue supply. |
| J2 | VDDHASGMIIRX1 | 3.3 V SGMII RX analogue supply. |
| H2 | VDDHASGMIITX1 | 3.3 V SGMII TX analogue supply. |
| K3 | VDDSGMII1 | 1.2 V SGMII digital supply. |
| J4 | VDDCORE | 1.2 V digital supply. |
| J5 | | |
| J6 | | |
| J8 | | |
| L9 | | |
| P5 | | |
| P7 | | |
| R5 | | |
| R7 | | |
| T1 | VDDCMUD | 1.2 V digital supply for CMU |
| T2 | | |
| U1 | VDDCMU | 3.3 V analogue supply for CMU |
| U2 | | |
| B2 | VDDIO | 3.3 V I/O supply |
| B12 | | |
| B13 | | |
| B14 | | |
| B15 | | |
| B16 | | |
| B17 | | |
| C2 | | |
| C12 | | |
| D2 | | |

| Pin | Symbol | Description |
|---|---|---|
| D12 | VDDIO | 3.3 V I/O supply |
| D18 | | |
| E12 | | |
| E18 | | |
| F5 | | |
| F6 | | |
| F12 | | |
| F18 | | |
| G4 | | |
| G5 | | |
| G6 | | |
| G12 | | |
| G14 | | |
| G15 | | |
| H5 | | |
| H6 | | |
| H11 | | |
| J14 | | |
| K5 | | |
| K6 | | |
| K7 | | |
| K10 | | |
| K11 | | |
| N10 | | |
| P4 | | |
| P6 | | |
| P8 | | |
| P10 | | |
| R3 | | |
| U4 | | |
| V11 | | |

*Table 12 Ground pins*

| Pin | Symbol | Description |
|---|---|---|
| P3 | GNDCMU | Digital PLL ground. |
| A1 | VSS | |
| A2 | | |
| A3 | | |
| A18 | | |
| B1 | | |
| B3 | | |
| B4 | | |
| B5 | | |
| B6 | | |
| B18 | | |
| C3 | | |
| C4 | | |
| C5 | | |
| C6 | | |
| C13 | | |
| C14 | | |
| C15 | | |
| C16 | | |
| C17 | | |
| C18 | | |
| D3 | | |
| D4 | | |
| D5 | | |
| D6 | | |
| D13 | | |
| D14 | | |
| D15 | | |
| D16 | | |
| D17 | | |
| E4 | | |
| E5 | | |
| E6 | | |
| E13 | | |

| Pin | Symbol | Description |
|---|---|---|
| E14 | VSS | |
| E15 | | |
| E16 | | |
| E17 | | |
| F1 | | |
| F13 | | |
| F14 | | |
| F15 | | |
| F16 | | |
| F17 | | |
| G1 | | |
| J10 | | |
| J11 | | |
| L4 | | |
| L5 | | |
| L6 | | |
| L7 | | |
| L8 | | |
| L11 | | |
| L13 | | |
| L14 | | |
| L15 | | |
| L16 | | |
| M4 | | |
| M5 | | |
| M6 | | |
| M7 | | |
| M8 | | |
| M11 | | |
| M13 | | |
| M14 | | |
| M15 | | |
| N4 | | |
| N5 | | |

*Table 12 Ground pins*

| Pin | Symbol | Description |
|---|---|---|
| N6 | VSS | |
| N7 | | |
| N8 | | |
| N9 | | |
| N13 | | |
| N14 | | |
| N15 | | |
| P14 | | |
| P15 | | |
| R14 | | |
| R15 | | |
| T13 | | |

| Pin | Symbol | Description |
|---|---|---|
| T14 | VSS | |
| T15 | | |
| T16 | | |
| V1 | | |
| V18 | | |
| L3 | VSSSGMII0 | |
| N3 | | |
| J3 | VSSSGMII1 | |
| K4 | | |

*Table 13 Internally connected pins*

| Pin | Symbol | Description |
|---|---|---|
| A4 | IC 01 | Leave to float. |
| A5 | IC 02 | |
| A13 | IC 03 | |
| A17 | IC 04 | |
| C11 | IC 05 | |
| D8 | IC 06 | |
| E2 | IC 07 | |
| E3 | IC 08 | |
| E8 | IC 09 | |
| F2 | IC 10 | |
| F4 | IC 11 | |
| G3 | IC 12 | |
| G9 | IC 13 | |
| G10 | IC 14 | |
| G13 | IC 15 | |
| H3 | IC 16 | |
| H4 | IC 17 | |
| H13 | IC 18 | |
| H14 | IC 19 | |
| H15 | IC 20 | |
| J13 | IC 21 | |
| J15 | IC 22 | |
| K13 | IC 23 | |
| N11 | IC 24 | |
| N12 | IC 25 | |
| P9 | IC 26 | |
| R8 | IC 27 | |
| R9 | IC 28 | |
| R12 | IC 29 | |
| R17 | IC 30 | |
| T3 | IC 31 | |
| T5 | IC 32 | |
| T6 | IC 33 | |
| T7 | IC 34 | |
| T9 | IC 35 | |
| T12 | IC 36 | Leave to float. |
| T17 | IC 37 | |
| U3 | IC 38 | |
| U5 | IC 39 | |
| U6 | IC 40 | |
| U7 | IC 41 | |
| U9 | IC 42 | |
| U10 | IC 43 | |
| U15 | IC 44 | |
| V3 | IC 45 | |
| V5 | IC 46 | |
| V6 | IC 47 | |
| V7 | IC 48 | |
| V8 | IC 49 | |
| V9 | IC 50 | |
| V12 | IC 51 | |
| V15 | IC 52 | |
| G7 | IC53 | |
| R10 | IC54 | |
| T10 | IC55 | |
| U8 | IC56 | |
| V10 | IC57 | |
| R2 | IC58 | |
| V2 | IC59 | |
| E9 | IC60 | |
| F10 | IC61 | |
| D10 | IC62 | |
| F11 | IC63 | |
| D9 | IC64 | |
| E7 | IC65 | |
| T11 | IC66 | |
| U11 | IC67 | |
| F7 | IC68 | |
| T4 | IC69 | |

*Table 14 Not connected pins*

| Pin | Symbol | Description |
|---|---|---|
| A6 | NC | Leave to float |
| A7 | | |
| A8 | | |
| A9 | | |
| A10 | | |
| A11 | | |
| A12 | | |
| A14 | | |
| A15 | | |
| A16 | | |
| B7 | | |
| B8 | | |
| B9 | | |
| B10 | | |
| B11 | | |
| C7 | | |
| C8 | | |
| C9 | | |
| D7 | | |
| F3 | | |
| G16 | | |
| G17 | | |
| G18 | | |
| H12 | | |
| H16 | | |
| H17 | | |
| H18 | | |
| J16 | | |
| J17 | | |
| J18 | | |

| Pin | Symbol | Description |
|---|---|---|
| K14 | NC | Leave to float |
| K15 | | |
| K16 | | |
| K17 | | |
| K18 | | |
| L12 | | |
| L17 | | |
| L18 | | |
| M16 | | |
| M17 | | |
| M18 | | |
| N16 | | |
| N17 | | |
| N18 | | |
| P12 | | |
| P13 | | |
| P16 | | |
| P17 | | |
| P18 | | |
| R13 | | |
| R16 | | |
| R18 | | |
| T18 | | |
| U12 | | |
| U13 | | |
| U14 | | |
| U17 | | |
| U18 | | |
| V13 | | |
| V17 | | |

# Interfaces

This section describes the various interfaces provided on the ACS9528.

## Input reference clocks

There are 3 LVTTL clock reference inputs denoted IPCLK[2:0].

## Time of day port

This port is an input comprising UARTRX and a 1 PPS signal.

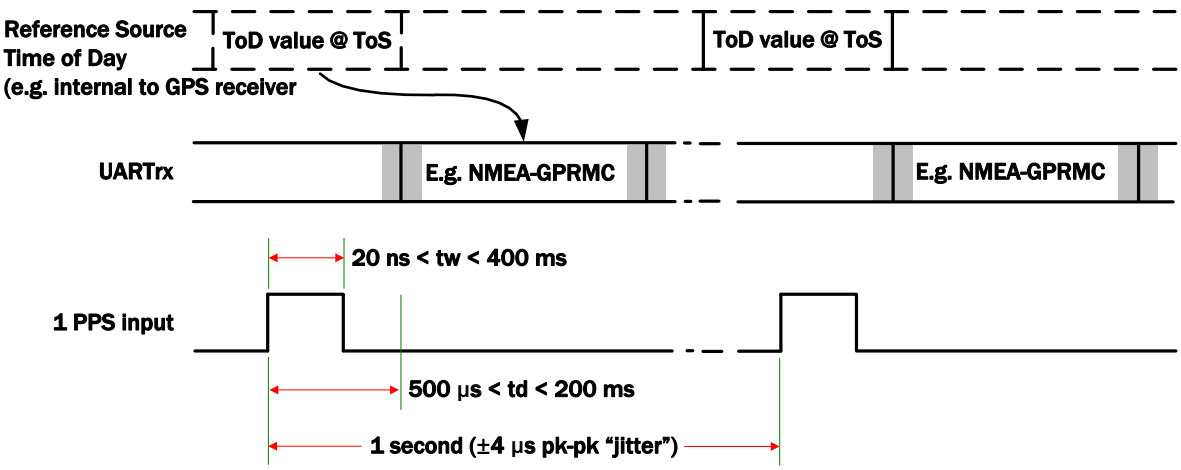



*Figure 3 - ToD port timing*

## Jitter tolerance of the 1PPS input

The ACS9528 will reject a 1PPS signal if the jitter is greater than 4 μs peak-to-peak. However, it is strongly recommended that jitter on this signal is avoided as much as possible because the distribution of jitter on this signal is not known and so cannot be correctly attenuated by filtering. Any filtering applied to this signal will introduce a phase offset error. This treatment differs from that of more traditional reference sources because the phase of a 1PPS signal, relative to a recognized source of time such as UTC, is the parameter of most significance. For other references, the rate (frequency) is the more significant parameter.

## Time of day message format

The ToD message format can be a GPRMC message or one of a group of other GPS messages or proprietary messages to suit specific causes. Refer to the DPSync Resource Center[1] for more details.

### GPRMC message format

A GPRMC message has the format $GPRMC,122356,A,0000.0000,N,00000.0000,W,0.0.0.0,120508,,,A*F6 in which the commas are separators. The architecture of the message is shown in Table 15. The message is 62 characters in length (i.e. 62 bytes). No parity bit is used, but each byte has a stop bit.

*Table 15 Architecture of GPRMC message*

| Element | Description |
|---|---|
| $GPRMC | Message header. |
| 122356 | UTC value. |
| A | Status (A = active, V = void). |
| 0000.0000,N | Latitude, north (fixed to zero). |
| 00000.0000,W | Longitude, west (fixed to zero). |
| 0.0 | Speed over ground (fixed to zero). |
| 0.0 | Track angle (fixed to zero). |
| 120508 | Date (ddmmyy). |
| A | A = autonomous, D = differential, E = estimated, S = simulation, N = not valid. |
| *F6 | Checksum. |

## Serial peripheral interface

The serial peripheral interface (SPI) is a slave port for communication with a serial microprocessor bus, allowing the ACS9528 to be controlled by an external processor. The serial interface header must be connected to the host processor, which acts as the master. The ACS9528 requires data to be transmitted LSB first, MSB first is not supported.

Figure 4 and Table 16 show the read access timing for the serial interface. Figure 4 shows two clock configurations. When SLVCFGCLKE = 1 (CPOL =1), the data is sampled on the falling edge and driven on the rising edge. When SKLVCFGCLKE = 0 (CPOL=0), the data is sampled on the rising edge and driven on the falling edge

Figure 5 and Table 17 show the write access timing for the serial interface. Figure 5 shows two clock configurations. When SLVCFGCLKE = 1 (CPOL =1), the data is sampled on the falling edge and driven on the rising edge. When SKLVCFGCLKE = 0 (CPOL=0), the data is sampled on the rising edge and driven on the falling edge.

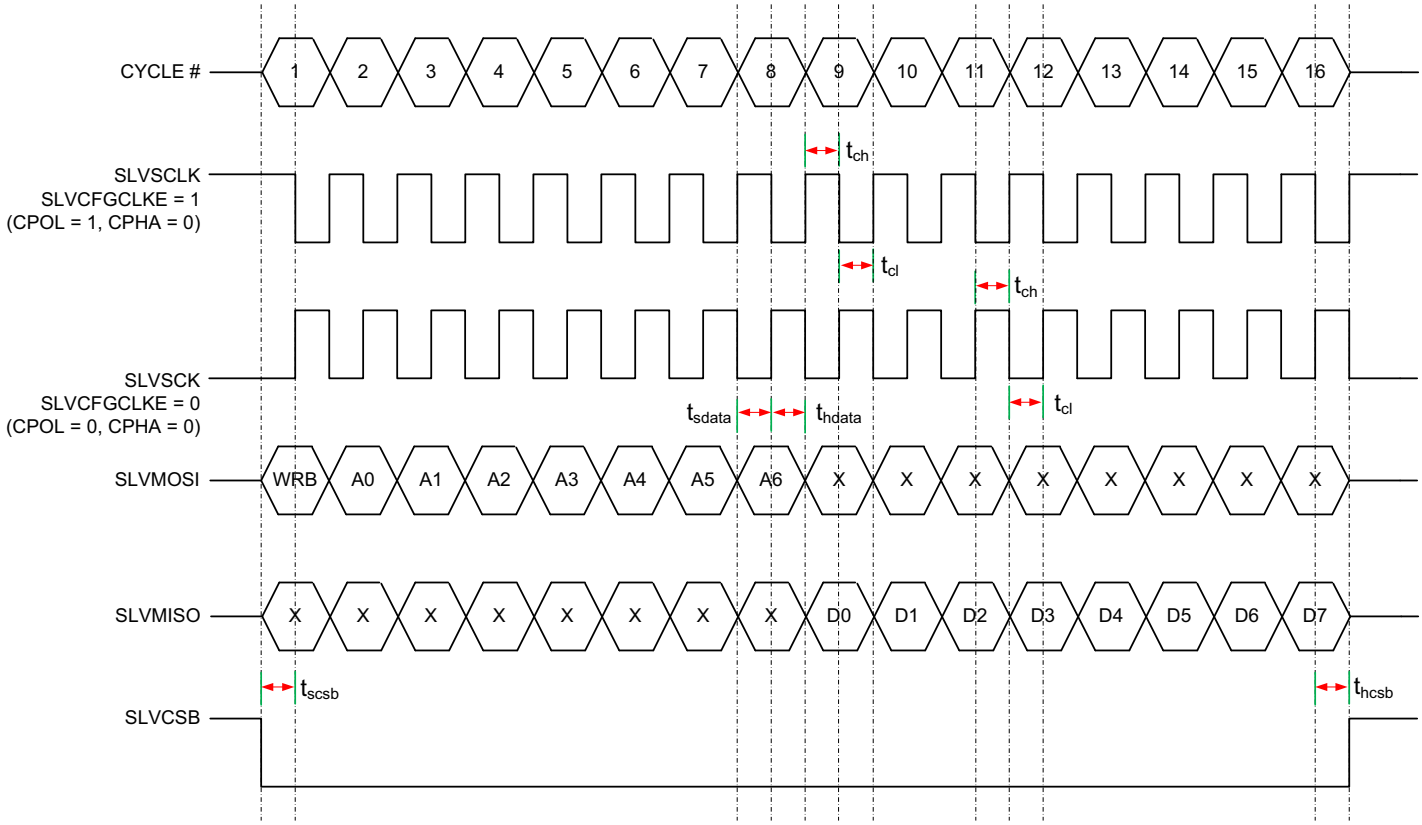



*Figure 4 - Read access timing of the serial interface*

*Table 16 Serial interface read access timing data*

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| $F_{sck}$ | SPI clock frequency | - | - | 10 | MHz |
| $t_{sdata}$ | Setup MOSI valid to $SCK_{rising\ edge}$ | 4 | - | - | ns |
| $t_{scsb}$ | Setup $CSB_{falling\ edge}$ to $SCK_{rising\ edge}$ | 14 | - | - | ns |
| $t_{d1}$ | Delay $SCK_{falling\ edge}$ to MISO valid | - | - | 45 | ns |
| $t_{d2}$ | Delay $CSB_{rising\ edge}$ MISO high-Z | - | 45 | - | ns |
| $t_{cl}$ | SCK Low time | 45 | - | - | ns |
| $t_{ch}$ | SCK High time | 45 | - | - | ns |
| $t_{hdata}$ | Hold MOSI valid after $SCK_{rising\ edge}$ | 6 | - | - | ns |
| $t_{hcsb}$ | Hold CSB low after $SCK_{rising\ edge}$ | 6 | - | - | ns |
| $t_p$ | Time between accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$) | 45 | - | - | ns |

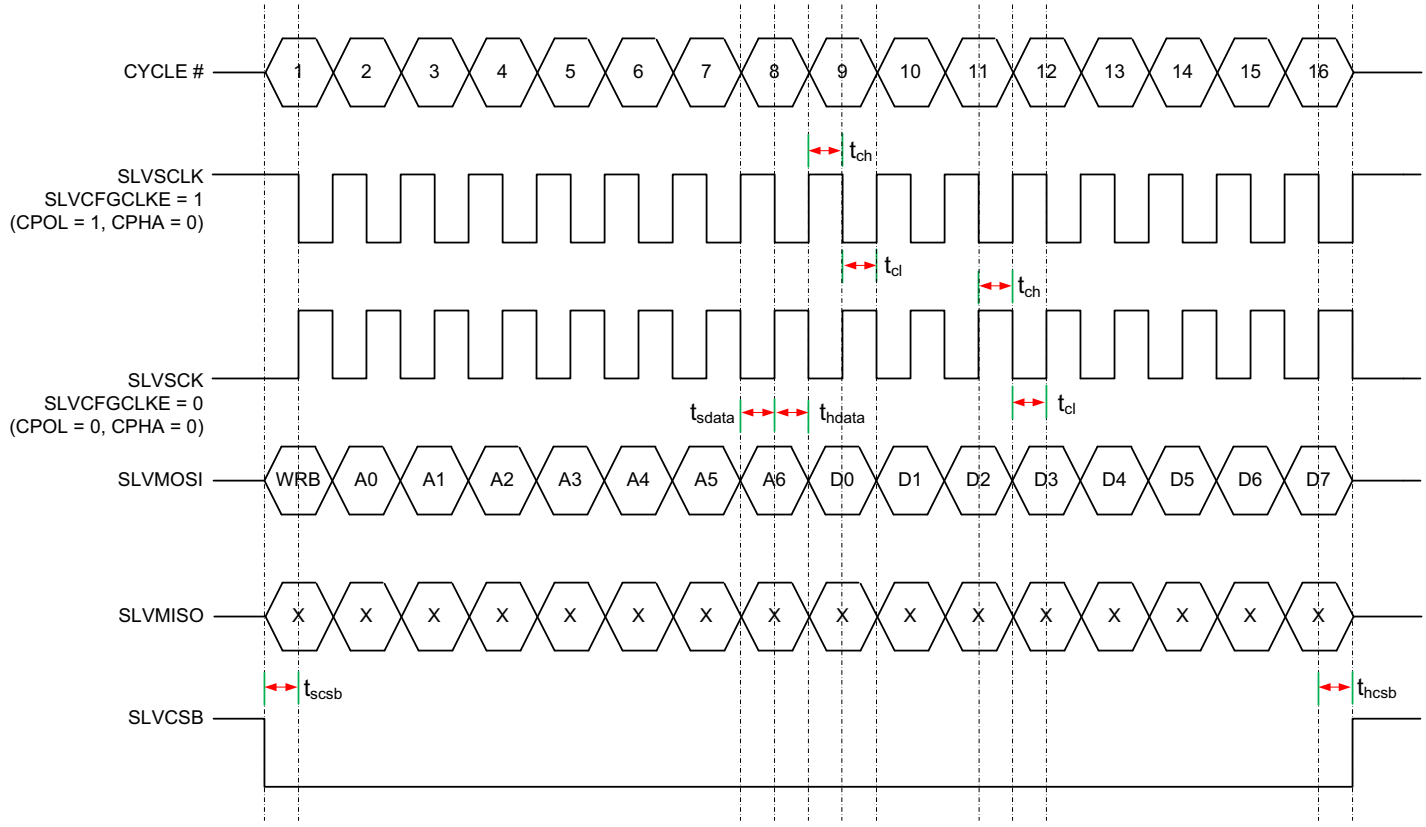



*Figure 5 - Write access timing of the serial interface*

*Table 17 Serial interface write access timing data*

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| $F_{sck}$ | SPI clock frequency | - | - | 10 | MHz |
| $t_{sdata}$ | Setup MOSI valid to $SCK_{rising\ edge}$ | 4 | - | - | ns |
| $t_{scsb}$ | Setup $CSB_{falling\ edge}$ to $SCK_{rising\ edge}$ | 14 | - | - | ns |
| $t_{d1}$ | Delay $SCK_{falling\ edge}$ to MISO valid | - | - | 45 | ns |
| $t_{d2}$ | Delay $CSB_{rising\ edge}$ MISO high-Z | - | 45 | - | ns |
| $t_{cl}$ | SCK Low time | 45 | - | - | ns |
| $t_{ch}$ | SCK High time | 45 | - | - | ns |
| $t_{hdata}$ | Hold MOSI valid after $SCK_{rising\ edge}$ | 6 | - | - | ns |
| $t_{hcsb}$ | Hold CSB low after $SCK_{rising\ edge}$ | 6 | - | - | ns |
| $t_p$ | Time between accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$) | 45 | - | - | ns |

## SGMII interfaces

The ACS9528 has two serial SGMII interfaces running with a 100 Mbps data rate and a 1.25 Gbps line rate. The interfaces are IEEE 802.3[7] compliant for communication via a suitable packet PHY. SGMII functional, timing, electrical and mechanical requirements are supported as defined in IEEE 802.3[7] part 3, section two, sub-section 22 and annexes 22A, 22B and 22C. (See also[12] clauses 36 and 37). The timing arrangements of both interfaces are identical. See [30] for more information. Note that this interface may be clocked via differential or single-ended SGMIICLK input ports.

*Table 18 SGMII clock timing characteristics*

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| FIN | SGMIICLK frequency | - | 125 | - | MHz |
| FT | SGMIICLK frequency tolerance | -100 | - | +100 | ppm |
| DuCy | SGMIICLK duty cycle | 40 | - | 60 | % |
| $T_{JTRIN}$ | SGMIICLK peak-to-peak input jitter | - | - | 40 | picosec |
| $T_{RCR}$, $T_{RCF}$ | SGMIICLK rise and fall time (20% to 80%) | - | - | 1 | nanosec |

*Table 19 SGMII output data AC characteristics*

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| DR[1] | Serial data rate | - | 1,25 | - | Gbits/sec |
| $t_{FALL}$ | Vod fall time (80% to 20%) | 100 | - | 200 | picosec |
| $t_{RISE}$ | Vod rise time (20% to 80%) | 100 | - | 200 | picosec |
| $t_{skew}$[2] | Skew between two members of a differential pair: $[tp_{HLP} - tp_{LHN}]$ or $[tp_{LHP} - tp_{HLN}]$ | - | - | ±20 | picosec |

1. Packets will be delivered by DPSync at the data rate DR, but DPSync can only support a sustained data rate of 100 Mbit/s (as per Fast Ethernet).
2. SGMIIRX differential input pairs have an internal 100 ? resistor between the input pins. No external resistor is needed. Damage to the internal resistor may occur if the differential voltage, Vidth, exceeds the maximum allowed value of 400 mV.

*Table 20 SGMII output data DC characteristics*

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Voh | Output voltage high state | - | - | 1525 | mV |
| Vol | Output voltage low state | 875 | - | - | mV |
| Vod | Output differential voltage | 150 | - | 400 | mV |

*Table 21 SGMII input data AC characteristics*

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| DRT[1] | Serial input data rate tolerance | -300 | - | +300 | ppm |

1. Packets may be delivered to DPSync at the data rate DR, but DPSync can only support a sustained data rate of 100 Mbit/s (as per Fast Ethernet).

*Table 22 SGMII input data DC characteristics*

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Vi | Input voltage range | 675 | - | 1725 | mV |
| Vidth | Input differential threshold | -50 | - | 50 | mV |
| Vid[1] | Input differential voltage | - | - | 650 | mV |
| Rin | Differential input impedance | 80 | - | 120 | Ω |

1. SGMIIRX differential input pairs have internal 100 Ω resistors between the input pins. No external resistor is needed. Damage to the internal resistor may occur if the differential voltage, Vid, exceeds the maximum allowed value of 650 mV.

## I²C interface

The characteristics of this interface are defined in the Philips-NXP I²C specification[31].

## JTAG port

The JTAG port is provided to allow a full boundary scan to be made.

JTAG implementation is fully compliant with IEEE 1149.1[6], with the following minor exceptions:

1) The output boundary scan cells do not capture data from the core, and do not therefore support INTEST. However this does not affect board testing.
2) The polarity of TRST complies with the standard:
   0 = normal operation.
   1 = enable JTAG boundary scan mode.

Refer to the standard for more information.

Figure 6 and Table 23 show the JTAG boundary scan timing.

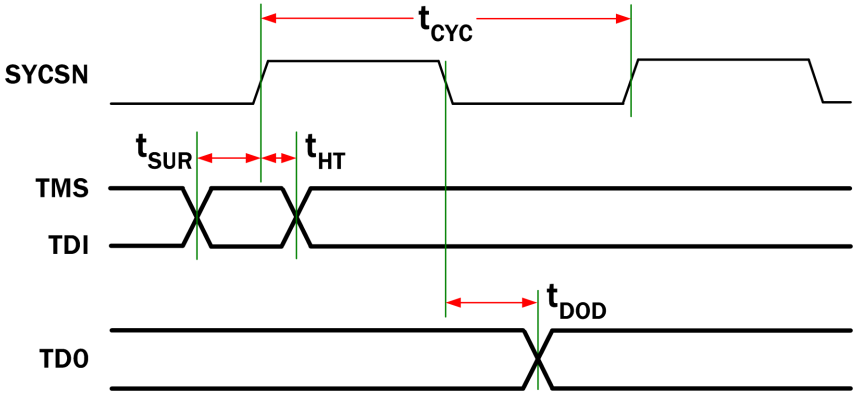



*Figure 6 - JTAG boundary scan timing diagram*

*Table 23 JTAG timing data (for use with Figure 6)*

| Symbol | Parameter | Minimum | Maximum | Units |
|---|---|---|---|---|
| $t_{CYC}$ | Cycle time. | 50 | - | ns |
| $t_{SUR}$ | TMS/TDI to TCK rising edge time. | 3 | - | ns |
| $t_{HT}$ | TCK rising to TMS/TDI hold time. | 30 | - | ns |
| $t_{DOD}$ | TCK falling to TDO valid. | - | 5 | ns |

*Table 24 DC characteristics of the JTAG ports*

| Parameter | Symbol | Minimum | Nominal | Maximum | Units |
|---|---|---|---|---|---|
| $V_{IN}$ High | $V_{IH}$ | 2 | - | - | V |
| $V_{IN}$ Low | $V_{IL}$ | - | - | 0.8 | V |

## Operating mode selection port

Mode select pins SYSMODE1 and SYSMODE0 set the operating mode of the ACS9528 as shown in Table 25. Mode selection changes on reset only.

*Table 25 Operating mode selection truth table*

| SYSMODE1 | SYSMODE0 | Operating mode |
|---|---|---|
| 0 | 0 | PTP Master. |
| 0 | 1 | SGMII/Ethernet self test (both ports). |
| 1 | 0 | SGMII/Ethernet self test (both ports and verbose debug via UART 0). |
| 1 | 1 | Restore default factory-programmed device settings. |

## Local oscillator clock

The master system clock on the ACS9528 should be provided by an external clock signal selected according to Table 28. The clock specification is important for meeting the ITU/ETSI and Telcordia performance requirements for holdover mode however a low cost relatively low stability oscillator may be used if stable holdover is not a requirement. ITU and ETSI specifications permit a combined drift characteristic of all non-temperature-related parameters of up to 10 ppb per day, at constant temperature. The same specifications allow a drift of 1 ppm over a temperature range of 0 to +70°C.

*Table 26 ITU and ETSI specification*

| Parameter | Value |
|---|---|
| Tolerance. | ±4.6 ppm over 20-year lifetime. |
| Drift<br>(Frequency drift over supply voltage range of +2.7 V to +3.3 V). | ±0.01 ppm/day @ constant temperature. |
| | ±1 ppm over temperature range 0°C to +70°C. |

Telcordia specifications require a non-temperature-related drift of less than 40 ppb per day and a drift of 280 ppb over the temperature range 0°C to +50°C.

*Table 27 Telcordia GR-1244 CORE specification*

| Parameter | Value |
|---|---|
| Tolerance. | ±4.6 ppm over 20 year lifetime. |
| Drift<br>(Frequency drift over supply voltage range of +2.7 V to +3.3 V). | ±0.28 ppm/over temperature range 0°C to +50°C. |

Please contact DAPU for information on recommended crystal oscillator suppliers.

### Oscillator frequency selection

Two oscillator frequency select pins (OSCFSEL1 and OSCFSEL0) set the expected local oscillator frequency, as shown in Table 28.

*Table 28 Oscillator frequency selection truth table*

| OSCFSEL1 | OSCFSEL0 | Selection |
|---|---|---|
| 0 | 0 | XTAL source 20 MHz. |
| 0 | 1 | XTAL source 10 MHz. |
| 1 | 0 | XTAL source 12.8 MHz. |
| 1 | 1 | Not used. |

## Reset (PORB)

Active low. Must be active low for a minimum of 100 ns. The ACS9528 will internally hold reset on until the PLLs have settled, after which the device enters the operating mode selected on the SYSMODE[1:0] port (see Table 25). If PORB is forced low, all internal states are reset to default values.

## Locked status

Indicates (active high) that the device has achieved lock to the selected reference. The degree of lock indicated is software defined. The LOCKED pin (F9) is used in PTP and self test modes only.

## Firmware specific input/output (IO)

Use subject to firmware version. If not used, leave to float.

## Power supply and internally connected pins and grounds

### Power supply and grounds

The ACS9528 is supplied with +3.3 V and 1.2 V (see Table 11 and Table 12).

### Internally connected pins

All other pins are internally connected. They should be connected to ground or left to float as described in Table 13.

# ELECTRICAL SPECIFICATIONS

## Electrical protection

### Over-voltage protection

The ACS9528 may require over-voltage protection on input reference clock ports according to ITU Recommendation K.41[21]. DAPU protection devices are recommended for this purpose. See the protection section at www.DAPU.com for appropriate parts.

### ESD protection

Suitable precautions should be taken to protect against electrostatic damage during handling and assembly. This device incorporates ESD protection structures that protect the device against ESD damage at ESD input levels up to at least ±4 kV using the human body model (HBM) ANSI/ESDA/JEDEC standard JS-001-2012 for all pins. In addition, the device is protected to at least ±1000 V using the Charged Device Model (CDM) to JEDEC standard JESD22-C101-E.

### Latchup protection

This device is protected against latchup for input current pulses of magnitude up to at least ±100 mA at JEDEC Standard No. 78C September 2010.

## Absolute maximum ratings

The absolute maximum ratings of the ACS9528 are shown in Table 29. When these values are the same as the operating conditions given in Table 30, the device will operate at the maximum ratings

***Table 29 Absolute maximum ratings***

| Parameter | Symbol | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Supply voltage DC, 3.3 V, input/output | $V_{DDIO}$ | -0.5 | - | 3.7 | V |
| Supply voltage DC, 3.3 V, CMU | $V_{DDCMU}$ | -0.5 | - | 3.7 | V |
| Supply voltage DC, 1.2 V, CMU, digital | $V_{DDCMUD}$ | -0.5 | - | 1.4 | V |
| Supply voltage DC, 1.2 V, CORE | $V_{DDCORE}$ | -0.5 | - | 1.4 | V |
| SGMII Rx analogue supply voltage DC, 1.2 V. | $VDD_{ASGMIIRX0}$ | -0.5 | - | 1.4 | V |
| SGMII Tx analogue supply voltage DC. 1.2 V | $VDD_{ASGMIITX0}$ | -0.5 | - | 1.4 | V |
| SGMII Rx analogue supply DC, 3.3 V. | $VDD_{HASGMIIRX0}$ | -0.5 | - | 3.7 | V |
| SGMII TX analogue supply DC, 3.3 V. | $VDD_{HASGMIITX0}$ | -0.5 | - | 3.7 | V |
| SGMII digital supply DC, 1.2 V. | $VDD_{SGMII0}$ | -0.5 | - | 1.4 | V |
| SGMII RX analogue supply DC, 1.2 V. | $VDD_{ASGMIIRX1}$ | -0.5 | - | 1.4 | V |
| SGMII TX analogue supply DC, 1.2 V. | $VDD_{ASGMIITX1}$ | -0.5 | - | 1.4 | V |
| SGMII RX analogue supply DC, 3.3 V. | $VDD_{HASGMIIRX1}$ | -0.5 | - | 3.7 | V |
| SGMII TX analogue supply DC, 3.3 V. | $VDD_{HASGMIITX1}$ | -0.5 | - | 3.7 | V |
| SGMII digital supply DC, 1.2 V. | $VDD_{SGMII1}$ | -0.5 | - | 1.4 | V |
| Input voltage, non-supply pins | $V_{IN}$ | -0.3 | - | $V_{DDIO}$ | V |
| Output voltage, non-supply pins | $V_{OUT}$ | -0.5 | - | $V_{DDIO}$ | V |
| Storage temperature | $T_{STOR}$ | -50 | - | +125 | °C |

CAUTION!
To avoid potentially damaging internal currents, the power rails should be applied to the device simultaneously (no more than 100 ms apart). See Figure 7.

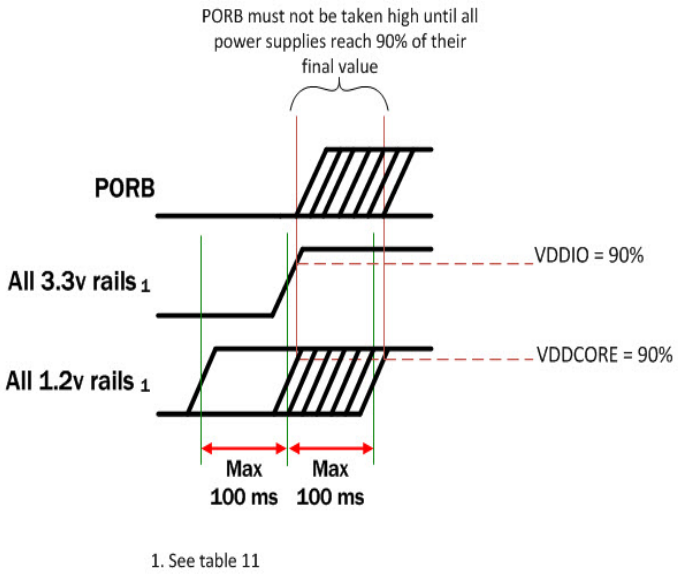



*Figure 7 - Power rail application timing*

# Operating conditions

*Table 30 Operating conditions*

| Parameter | Symbol | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Power supply DC voltage, 3.3 V, input/output | $V_{DDIO}$ | 3.135 | 3.3 | 3.465 | V |
| Power supply DC voltage, 3.3 V, CMU | $V_{DDCMU}$ | 3.135 | 3.3 | 3. 465 | V |
| Power supply DC voltage, 1.2 V, CMU, digital | $V_{DDCMUD}$ | 1.14 | 1.2 | 1.26 | V |
| Power supply DC voltage, 1.2 V, CORE | $V_{DDCORE}$ | 1.14 | 1.2 | 1.26 | V |
| SGMII Rx analogue supply voltage DC, 1.2 V. | $VDD_{ASGMIIRX0}$ | 1.14 | - | 1.26 | V |
| SGMII Tx analogue supply voltage DC. 1.2 V | $VDD_{ASGMIITX0}$ | 1.14 | - | 1.26 | V |
| SGMII Rx analogue supply DC, 3.3 V. | $VDD_{HASGMIIRX0}$ | 3.135 | - | 3. 465 | V |
| SGMII TX analogue supply DC, 3.3 V. | $VDD_{HASGMIITX0}$ | 3.135 | - | 3. 465 | V |
| SGMII digital supply DC, 1.2 V. | $VDD_{SGMII0}$ | 1.14 | - | 1.26 | V |
| SGMII RX analogue supply DC, 1.2 V. | $VDD_{ASGMIIRX1}$ | 1.14 | - | 1.26 | V |
| SGMII TX analogue supply DC, 1.2 V. | $VDD_{ASGMIITX1}$ | 1.14 | - | 1.26 | V |
| SGMII RX analogue supply DC, 3.3 V. | $VDD_{HASGMIIRX1}$ | 3.135 | - | 3. 465 | V |
| SGMII TX analogue supply DC, 3.3 V. | $VDD_{HASGMIITX1}$ | 3.135 | - | 3. 465 | V |
| Ambient operating temperature range | $T_A$ | -40 | - | +85 | °C |
| Supply current (3.3 V) | $I_{DDHASGMIIRX0}+I_{DDHASGMIITX0}+I_{DDHASGMIIRX1}+I_{DDHASGMIITX1}+I_{A1} + I_{A2} + I_{A3} + + I_{DDCMU} + I_{DDIO} + I_{DD\_RAM}$ | - | 49[1] | 68[2] | mA |
| Supply current (1.2 V) | $I_{DDCORE} +I_{DDASGMIIRX0}+I_{DDASGMIITX0} +I_{DDASGMIIRX1}+I_{DDASGMIITX1} +I_{DDSGMII0}+I_{DDSGMII1} +I_{DDCMUD}$ | - | 230[1] | 231[2] | mA |
| Total power dissipation | $P_{TOT}$ | - | 0.44[1] | 0.55[2] | W |

1. Master configuration, locking to a 1PPS reference and supporting a single Slave.
2. Master configuration supporting 128 Slaves.

# DC characteristics

Unless otherwise stated, the DC characteristics apply to all operating conditions.

***Table 31 DC characteristics of the TTL ports***

| Parameter | Symbol | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| TTL input port | | | | | |
| $V_{IN}$ High. | $V_{IH}$ | 2 | - | - | V |
| $V_{IN}$ Low. | $V_{IL}$ | - | - | 0.8 | V |
| Input current. | $I_{IN}$ | - | - | 10 | µA |
| TTL input port with internal pull-up | | | | | |
| $V_{IN}$ High. | $V_{IH}$ | 2 | - | - | V |
| $V_{IN}$ Low. | $V_{IL}$ | - | - | 0.8 | V |
| Pull-up resistor. | PU | 20 | - | 200 | kΩ |
| Input current. | $I_{IN}$ | - | - | 100 | µA |
| TTL input port with internal pull-down | | | | | |
| $V_{IN}$ High. | $V_{IH}$ | 2 | - | - | V |
| $V_{IN}$ Low. | $V_{IL}$ | - | - | 0.8 | V |
| Pull-down resistor. | PD | 20 | - | 200 | kΩ |
| Input current. | $I_{IN}$ | - | - | 100 | µA |
| TTL output port (OPCLKx, PPNSx) | | | | | |
| $V_{OUT}$ Low ($I_{OL}$ = 8 mA). | $V_{OL}$ | 0 | - | 0.4 | V |
| $V_{OUT}$ High ($I_{OH}$ = 8 mA). | $V_{OH}$ | 2.4 | - | - | V |
| Drive current. | $I_D$ | -8 | - | 8 | mA |
| TTL output port (other pins) | | | | | |
| $V_{OUT}$ Low ($I_{OL}$ = 4 mA). | $V_{OL}$ | 0 | - | 0.4 | V |
| $V_{OUT}$ High ($I_{OH}$ = 4 mA). | $V_{OH}$ | 2.4 | - | - | V |
| Drive current. | $I_D$ | - | - | 4 | mA |

# BLOCK DIAGRAM

Figure 8 shows a block diagram of the PTP Block. The main functions are described below. Control of the blocks is achieved via registers accessed over the SPI using functions provided by DAPU. For details, please refer to the API documentation in the DPSync Resource Center[1].

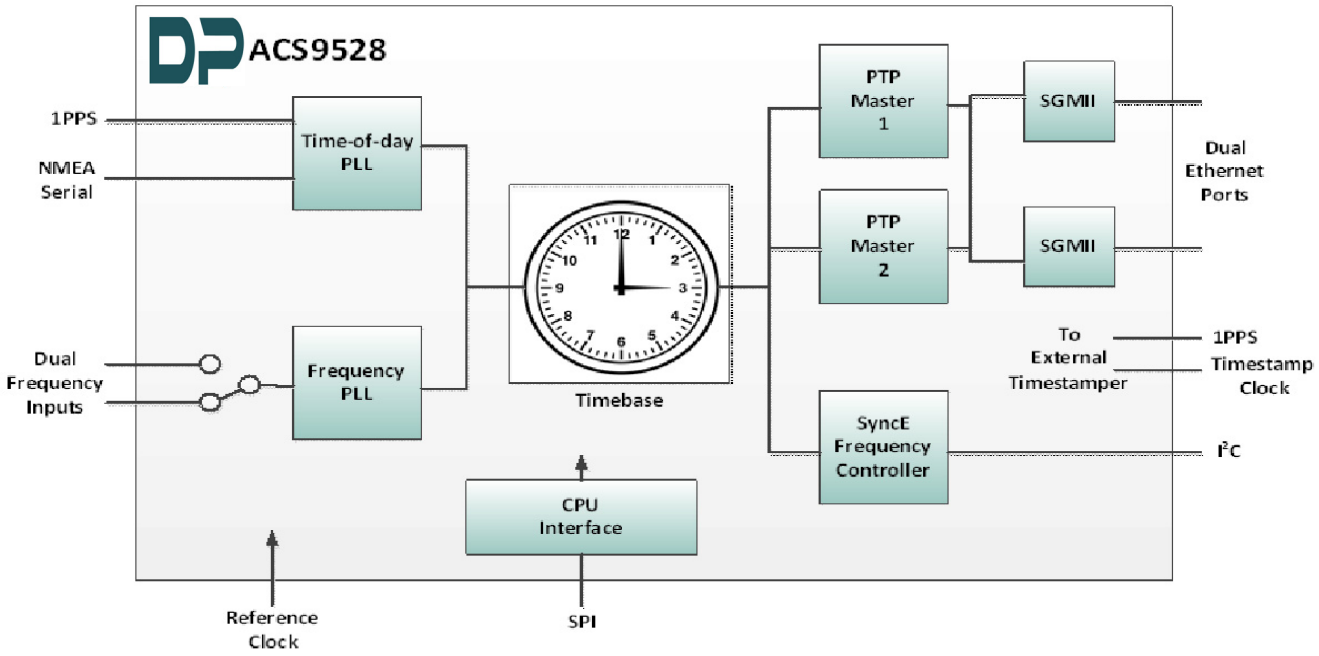



*Figure 8 - Block diagram*

## PTP Master ports

The PTP Master ports are the interface to the rest of the PTP network. They handle PTP controls and perform hardware timestamping. The PTP ports have many configurable functions involved in interfacing with the network. These functions have sensible defaults which suit many situations. If specific configurations are required, these can be performed using appropriate API calls, the most important of which are listed in PTP port API calls.

The PTP Master Ports operate at the MAC layer of the Ethernet stream. It is responsible for generating PTP timestamps for all PTP event messages. The timestamps use the local timebase generated by the frequency and time generator.

The PTP Master Ports generate the timestamps for all outgoing Sync messages (the t1 timestamp) and the timestamps of all incoming delay-request messages (the t4 timestamp). they also insert the timestamps of all received delay-request messages into the timestamp field of the corresponding delay-response messages.

## Time and frequency PLLs

The PTP Input Reference Port is used to supply a local source clock. It is responsible for selecting the reference source which should be used to drive the rate of the local timebase. The selection is controlled by host code. The PTP Input Reference Port accepts up to 2 input clock signals. They can be independent signals and can operate at individual frequencies, but they must obey the following rule:

Input Freq = k * 2^n, where 0 <= n <= 5 and 1 <= k <= 2^32 (upper limit of 170 MHz)

(For example, for an input frequency of 2.048 MHz, k would be 64,000 and n would be 5, so 64,000 x 2^5 = 2,048,000).

Under software control, one of the active inputs will be selected and passed to the Frequency and Time Generator to control the rate of change of the local timebase. Whatever its rate, the input clock signal or a clock derived from the input clock signal is supplied to the Frequency and Time Generator to control the rate of change of the local timebase. If the Master is to provide a frequency delivery service, there is no need to align the local timebase to any external timebase and its epoch will be the

beginning of the PTP timebase (in other words, the first timestamp generated after power-on will indicate 1st January 1970, whatever the actual time and date).

If the selected input clock signal is a 1PPS signal, and if the Master timebase should be aligned to Temps Atomic International (TAI, International Atomic Time), then the ingoing 1PPS signal should indicate the top-of-second point and the current second will be indicated in a timing message going in on the UART. Similarly, if the Master should be aligned to an external timebase which is not traceable to TAI, the timing message will hold the current seconds count of the external timebase but neither this value, nor the 1PPS signal, will necessarily be aligned to TAI.

### UART

The ACS9528 includes a UART to which the timing message is written . This is only needed when a PTP GM must be aligned with an external timebase (TAI or arbitrary). .

The timing message should be provided regularly; a consecutive sequence of 3 missing timing messages is taken to indicate that the reference source timebase has failed. This will activate an alarm which can be accessed using an API call; the time-traceable flag in outgoing Sync messages will be cleared. The timing message carries GPS time and not TAI. If the PTP Master is to be aligned to TAI, then it must convert GPS time to PTP time (derived from TAI), but the Master must know the current count of leap seconds since the GPS epoch. The PTP Master obtains this from host code using an API call. The PTP Master must also know when a leap second event is pending, and this is also obtained from host code using an API call.

### Timebase

The Frequency and Time Generator is the heart of the ACS9528 PTP Block. This function generates the local timebase at a rate determined by the clock signal supplied to it by the PTP Input Reference Port (or by the local oscillator if no such signal is available). If the Master timebase is required to be aligned to an external timebase, then the signal supplied should be a 1PPS signal and the rising edge should indicate the top-of-second point of the external timebase. The function will align the timebase so that the beginning of each new second occurs coincidentally with the top-of-second point.

The 1PPS signal is checked for consistency and low jitter before being accepted. It requires three consecutive pulses spaced at a nominal 1-second interval and is rejected if a pulse is missed. The timebase time and date will be aligned to the external timebase using the values presented in the timing message on the UART, but converted to the PTP epoch. If the external timebase is TAI, the leap second information will also be used.

Holdover performance depends on two characteristics: adequate stability of the local oscillator and adequate holdover data acquired whilst locked to a stable reference source. The former is satisfied by selecting a suitable oscillator. The latter is satisfied by ensuring that the ACS9528 is adequately locked to a suitable reference source for an adequate period of time.

The selection of the reference source is determined by factors outside the ACS9528, but making sure that the device is adequately locked before it begins to acquire holdover data, and then acquiring holdover data for a long enough period, are actions that the device can execute.

Firstly, the device will not begin to acquire holdover data until it is adequately locked.

Secondly, the device will acquire holdover data for a rolling period set by the software.

.To determine whether a particular value of $F_{OUT}$ is supported, apply the following test:

M must be an integer less than $2^{17}$ (131072) where M is calculated as below:

GCD = greatest common divisor of $125 \times 10^6$ and $F_{OUT}$

$M = 125 \times 10^6/GCD$

Refer to the ACS9528 User Guide, the Application Programmers Interface Document and the DPSync Resource Center.

## Self test

The ACS9528 device includes a software module which tests the Ethernet PHYs connected to it. Full details are contained in associated document Application Note AN-TS 2 5.0 Self Test Module Test Specification.

The self-test software module is instigated by controlling mode selection pins SYSMODE[1:0] as shown in Table 25, and performing a power-on reset cycle.

# APPLICATIONS

Figure 9 shows three different ways in which timing (that is, frequency stability) can be delivered to the end-points of a transmission link.

The PTP method uses the Precision Timing Protocol to carry timing information in the form of timestamps contained in special PTP frames. This method has the advantage of being able to operate on legacy Ethernet equipment. However, the performance can be affected by traffic loading. The ITU have defined a new PTP profile to suit frequency delivery over legacy packet networks; this is defined in ITU Recommendation G.8265.1[33].

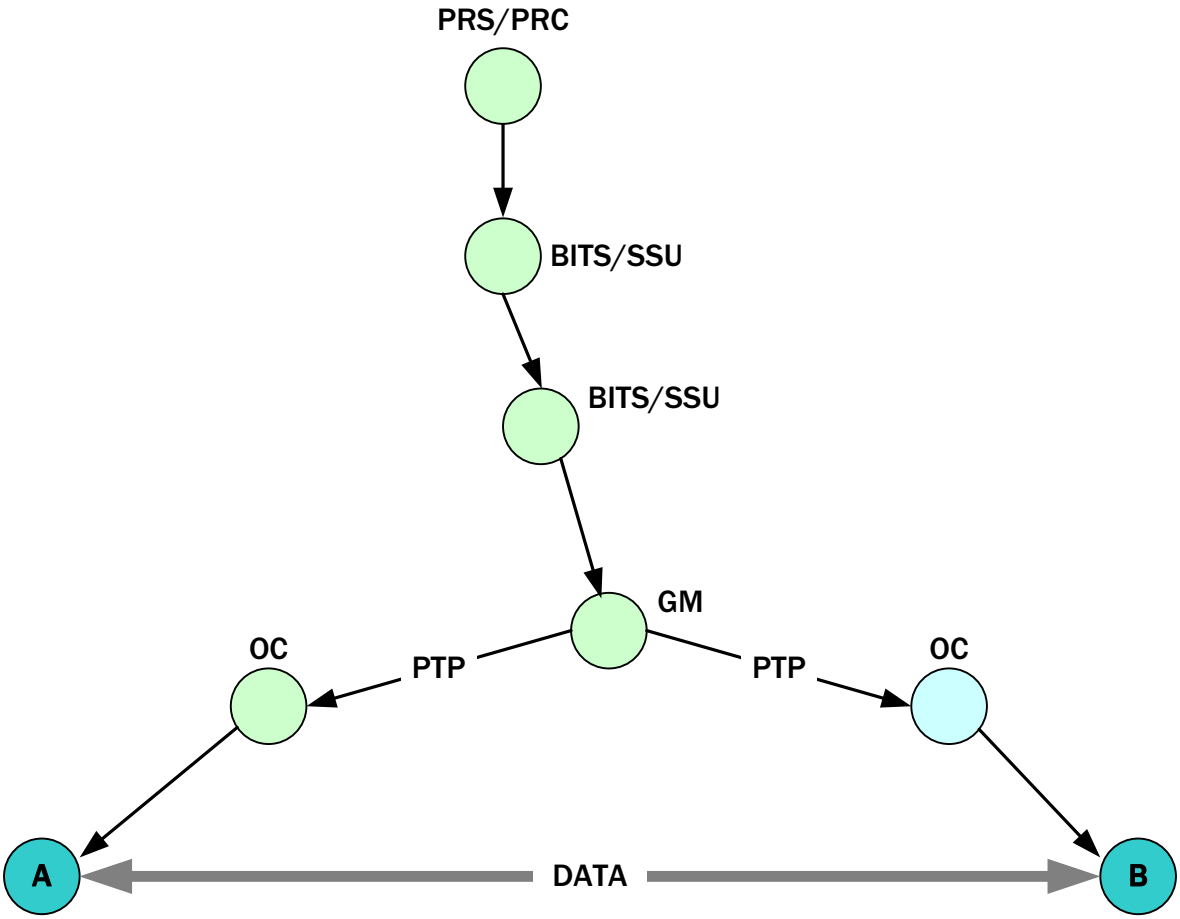



*Figure 9 - Timing techniques for different networks*

The ACS9528 contains timing functions that can be used in many ways to support a variety of situations. The device can generate output clock signals and/or timing packets allowing it to optionaly support dual Master system architectures implementing synchronous Ethernet as well as external timestamping.

Refer to Figure 2 for a block diagram of the ACS9528.

## Packet based timing

Packet-based timing methods can provide the usual frequency transfer, or they can also provide ToD transfer, or the transfer of a common phase. The second version of the Precision Time Protocol (PTP), IEEE 1588-2008[13], has been developed with many telecommunication applications in mind, and DPSync, uses PTP as the transport method to carry timing data between the GM clock and the ordinary clocks.

The basic principle by which PTP performs time transfer is described in the PTP standard. However, the standard does not stipulate how to operate in the presence of packet delay variation. DPSync adds its own proprietary filtering algorithms to provide accurate timing transfer in the presence of PDV, network re-routes and other conditions.

The ACS9528 DPSync can act as either a single or dual channel. The configuration is controlled by the host code.

## PTP messages

Figure 10 shows the three main messages used to transfer timing data between a GM and its OCs.

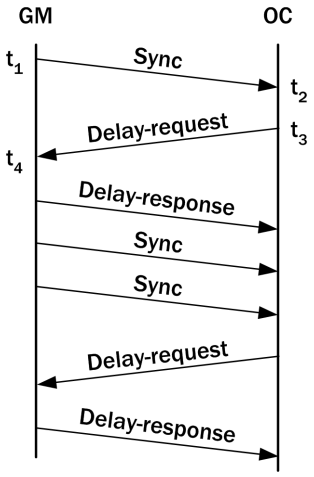



*Figure 10 - Message triplet of PTP*

The Sync message is sent most frequently and carries the time t1 at which the timestamp point of the message crossed the MII of the GM. The time at which the Sync message crosses the MII of the OC is t2 and is measured using the timebase of the OC. The rate of Sync messages should be high enough to overcome drift in the local reference of the OC and allow sufficient filtering of packet delay variation encountered in the network. Typical rates for most telecom applications connected via a typical network range from 8 to 32 Sync packets per second, when using a local oscillator of acceptable quality at the OC.

The Delay-Request message is sent to the GM by the OC and allows the network path delay to be estimated. The message carries the time t3 at the OC at the moment of transmission. The rate of transmission of Delay-Request messages should be chosen to suit the PDV, and rates similar to that of the Sync message can be expected, although other rates are allowed.

The GM sends one Delay-Response message for each Delay-Request message that it receives. The Delay-Response message carries the time t4 at which the GM received the Delay-Request message.

These message transfers provide the four timestamps, carrying times t1-t4, to the OC, from which it can calculate the time at the GM.

There are other messages in PTP, but they are not involved in the time-transfer. Announce messages, for example, carry information about the reference source used by a clock.

The Sync and Delay-Request messages are classed as event messages in PTP and, when using the UDP-IP-Ethernet mapping, are from UDP Port 319. Other messages are general messages from UDP Port 320.

To transfer ToD or common phase across a network, the PTP packet flow must be two-way; that is, both Sync and Delay-Request PTP messages must be used. It is recommended that unicast transmission be used, supported, where possible, by Quality of Service (QoS) assistance in the nodes in the network through which the PTP messages flow. These measures not only help to provide the best accuracy and stability of the ToD deliverable by an OC, but they also reduce the traffic load on clocks. The alternative use of multicast PTP event messages means that each clock receives Delay-Request messages from every OC in the network, and it also receives Delay-Response messages intended for every OC in the network. As the number of PTP clocks in a network grows, this can overload the ports of the clocks and interfere with the legitimate flow of other services.

## Grandmaster selection (default IEEE 1588 BMCA)

The GM is the clock which distributes the timescale amongst the clocks in the network. Most of the other clocks would take their timing from it, although it is possible to have some clocks which cannot defer to others; these could also distribute their timing or they could go into a passive state. The action they take depends on the clock selection mechanism employed. A basic clock-selection mechanism has been defined in PTP (the BMCA), which is suitable for many applications of PTP. It may not, however, be universally adopted in telecoms applications because it does not mirror the traditional clock hierarchy. Alternative clock-selection mechanisms can be defined in PTP profiles.

According to the PTP BMCA, the GM clock is the one to which all other clocks have deferred. On start-up, each PTP clock listens for Announce messages from a GM; these contain information about the reference source quality and any pre-configured preferences for the order in which clocks should be selected. If no Announce messages are heard after a short period of time, the clock begins to send its own Announce messages.

Each clock compares the information from other clocks with its local values and decides whether it is the best clock in the network; if not, it becomes an OC (if it can) and prepares to accept timing from another clock. The parameters compared, and the order in which they are compared, is as follows:

Priority 1
Clock Quality
Priority 2
Clock ID

Using the Priority 1 value in the first comparison allows the network operator to pre-determine the order in which GMs would be selected. However, this assumes that the quality of the reference source driving the selected GM is constant; the BMCA cannot respond to changes in the quality of the clock if the Priority 1 value alone is enough to make the selection. To bring the clock quality parameters into the selection mechanism, the Priority 1 value has to be set to be the same value in all clocks being considered for the GM role. This then allows the BMCA to identify the clock which advertises the best reference source and can allow that to become the GM. Using the BMCA, therefore, the selection depends heavily on the configured quality of the reference sources used by the clocks.

The reference source is of vital importance in PTP. Not only does it control the quality of the timing being distributed around the network (in the case of the GM), it is also used by the BMCA to identify the GM; in addition to this, it also limits the range of applications that the timing network can support. For example, if an application requires ToD, then the reference supplied to the GM must provide this.

The reference is the source of timing to which a clock is tied. Potential GMs and OCs both have references, where the reference of a potential GM would typically be supplied from an external source (e.g., a GPS receiver if ToD is to be transferred), while that of an OC would typically be the local oscillator that provides a local system clock frequency.

The quality of the reference is represented by three parameters, known as clock accuracy, clock variance and clock class. The clock accuracy parameter indicates how closely the reference represents the ideal source. This is usually an estimate derived from experience with the type of reference employed - for example, a GPS receiver can be expected to be within 100 ns of true GPS time, even though the actual error is unknown for a particular receiver.

The clock accuracy parameter is only of use when ToD applications are to be supported; it is redundant for frequency-delivery applications, for example.

The clock variance represents the stability of the reference, which is related to the noise content and drift of the reference over time; again, this is usually an estimate based on experience with the type of reference. In principle, clock variance could be useful in frequency-delivery applications, but this would need additional standardization beyond the current PTP standard.

The clock class parameter indicates the type of reference and how it can be used in a PTP network -- for example, whether the clock is currently locked to its reference and the reference is valid, or that the clock's reference is currently invalid but is still within the tolerated accuracy error; the clock class can also indicate whether a clock can be used as a GM or whether it can only become an OC. The clock class parameter is the most useful of the clock quality parameters in telecom applications. It is analogous to an SSM value, although any equivalence would need to be standardised (e.g. G.8265.1[33]).

Using these clock quality parameters, the "best master clock" would be the clock which was allowed to be a GM and was tied to a valid reference which had the tightest accuracy, the smallest variance and was suitable for the application.

In accordance with the PTP standard, it is sometimes appropriate to limit a PTP clock to adopting a role which is appropriate to its particular situation, and barring it from adopting other roles; for example, clocks which do not have good enough local oscillators or external references should not be allowed to become GrandMasters, even if they are the best clocks visible in the PTP network (such a clock would be a so-called "Slave-only" clock); similarly, some clocks may not be allowed to become slaves of other clocks. To support this, the ACS9528 can be individually barred from adopting either the GM role or the OC role. An API call is available to control this configuration, but the default setting is to be able to freely adopt either role according to the clock selection algorithm in use.

### BMCA selection based on priority

If the PTP network has a preference for the order in which clocks can become the GM then this can be indicated in the Priority 1 and Priority 2 parameters of the Announce message. Priority 1 is tested first by the BMCA, and the clock with the higher priority is selected; this means that Priority 1 overrides the clock quality parameters. This is useful if it is known that all GM candidates have the same clock quality, and one clock is preferred over others, but it does not allow for changes in the clock quality of a GM to influence the selection. For example, if a GM lost its reference source and went into holdover, this would be indicated by the clock class parameter, but it would not cause the GM to be replaced by one which is still tied to its reference source. For this reason, Priority 1 is probably best used to segregate potential GMs from other clocks (that is, give all potential GMs a high Priority 1 value, and give lesser clocks a lower value). The BMCA would then not be able to select a GM on Priority 1 alone but must look at other parameters as well.

### BMCA selection based on reference quality

If the network requires that the clock with the best reference be selected, then Priority 1 should be set to the same value in all GM candidates. The BMCA then selects the GM based on the Clock Quality parameters, in the order ClockClass, Clock Accuracy, Clock Variance. In the BMCA, Clock Class values greater than 127 are used to indicate clocks which are not required to become PTP GrandMasters. To select between clocks which have the same clock quality, the Priority 2 value is used.

### BMCA in Multicast vs Unicast networks

Once the best master clock has been identified, all other potential GMs should decide whether to cease transmission of PTP event and Announce messages, leaving just the best master clock to control all the ordinary clocks, or continue transmission.

A strict interpretation of the PTP standard shows that the BMCA need only be applied when multicast transmission is used; there is no strict requirement to apply the BMCA if unicast transmission is used. This is just as well if the Acceptable Master Table (AMT) is to be used, because this allows more than one GM to send PTP messages at any time.

### Reference sources for telecom applications

The most important reference source of a PTP system is the one which feeds the GM. The qualities of the reference source can determine which master, out of a set of possible masters, becomes the GM.

To become a PTP GM, the ACS9528 must be supplied with a reference source which meets the needs of the application. Figure 11, Figure 12 and Figure 13 summarize what are expected to be the three main types of applications: ToD, common-phase-transfer and frequency-transfer. The reference source must support the application. For example, a ToD reference must be used if the application requires ToD (see Time of day port).

A ToD reference source would be supplied to the GM as a ToD timing message and a 1PPS signal. Peripheral information, such as the current count of leap seconds, would be supplied via API calls. The ToD timing message would be supplied to the UART receive port. The timing of the message is not critical, provided the message has been received before the rising edge of the 1PPS signal occurs. Supported by the leap-second count, the timing message would be used to derive the PTP timescale inside the ACS9528, and this is carried in the timestamps. The 1PPS signal is fed to the PTP Block and the internal timescale is aligned with it.

For telecom clocks which are known to be stable, such as the outputs of BITS/SSUs, the reference signal can be supplied directly to an input port of the PTP Block. The PTP Block can accept signals at frequencies which meet the requirements in section “PTP input reference port (time selector)”. Whichever type of reference is supplied, the PTP Block must know the quality of the selected clock and it is given this using an API call.

The accuracy and variance are parameters obtained from the manufacturer of the reference source (or interpreted by the user). For ToD applications, these parameters could be important; for example, if each of the potential Masters have different accuracies or stabilities to offer, then the Master with the best performance should be selected as the GM for the application; however, the individual values for these parameters at each Master may not be known absolutely and may have to be estimated from anecdotal information (such as production test records). Alternatively, if there is no way to know the parameters with sufficient accuracy, the parameters could be removed from the selection mechanism by making them identical across all Masters (the default values provide an easy way to do this). Similarly, for many telecom applications, such as the transfer of existing network clocks across a packet network, these parameters are likely to be meaningless, and it would be best to use the default values.

The clock class parameter is a status flag and does not require an accurate measurement of a physical parameter. It is simply assigned by a network manager in accordance with the rules of PTP. The clock class values are used to indicate what state the reference is in (that is, whether it is traceable to a reference point or not) and this information has to be passed to the ACS9528.

*NOTE: To correctly advertise the Masters clock quality the host code must configure the ACS9528 with the appropriate parameters for the associated reference source.*

### ToD applications

If an application requires a ToD signal, the timebase of the GM must be traceable to TAI and OCs (slaves) must be controlled to select only GMs which have TAI-traceable references. The GM reference source determines the traceability to TAI. The selection of GMs with TAI-traceable timebases can be achieved by the OCs using their AMT, which is programmed using host code. Host code must monitor traceability and status information that is passed out in the Announce messages. An API call makes this information available to the host code.

The input reference port consists of IPCLK input clocks and the UART port. With a ToD reference source, an IPCLK port is supplied with a 1 PPS signal and the timing message carrying the current time is applied to the UART port of the ACS9528.

The ToD port can support either TAI-traceable or non-TAI-traceable applications. TAI-traceable applications are those which require the timebase of the ACS9528 to be aligned with a primary time source which is derived from TAI (such as UTC or GPS). Non-TAI-traceable applications are those which require alignment to some other, application-specific, time source.

The UART port accepts timing-related ToD 0183 timing messages (ignoring other messages, such as those which carry position information). The format and timing of this message is described in Time of day message format.

The UART port is used in the same way in both TAI-traceable and non-TAI-traceable applications, but the ACS9528 has to be informed by configuration which type of application it is supporting. In both types of application, the day/hours/minutes/seconds information given by the ToD messages determines the coarse phase of the timebase relative to the source time reference. Failure of the UART port is detected and the messages ignored.

So long as the ACS9528 had previously been receiving good messages, the timebase is correctly aligned to the external timebase and, so long as the 1 PPS signal remains good, the timebase remains aligned during the failure.

When the ACS9528 is informed by configuration that it is tied to a time standard which is traceable to TAI, then, in accordance with IEEE 1588 version 2[13], the internal timebase is aligned to the PTP epoch (which is derived from TAI). Timestamps in PTP event messages are PTP timebase values. PTP announce messages have the following flags and fields set accordingly:

PTP flag is TRUE (indicating that the timebase is traceable to TAI).

L1 and L2 flags are valid.

timeTraceable flag is TRUE.

frequencyTraceable flag is TRUE.

currentUtcOffset field is valid (as set by configuration via an API call).

timeSource field is valid (as set by configuration).

clockClass field is as set by configuration (6, if no special profile is in use).

Figure 11 shows an example of a PTP link delivering ToD to an application, which applies to TAI-traceable and non-TAI-traceable situations.

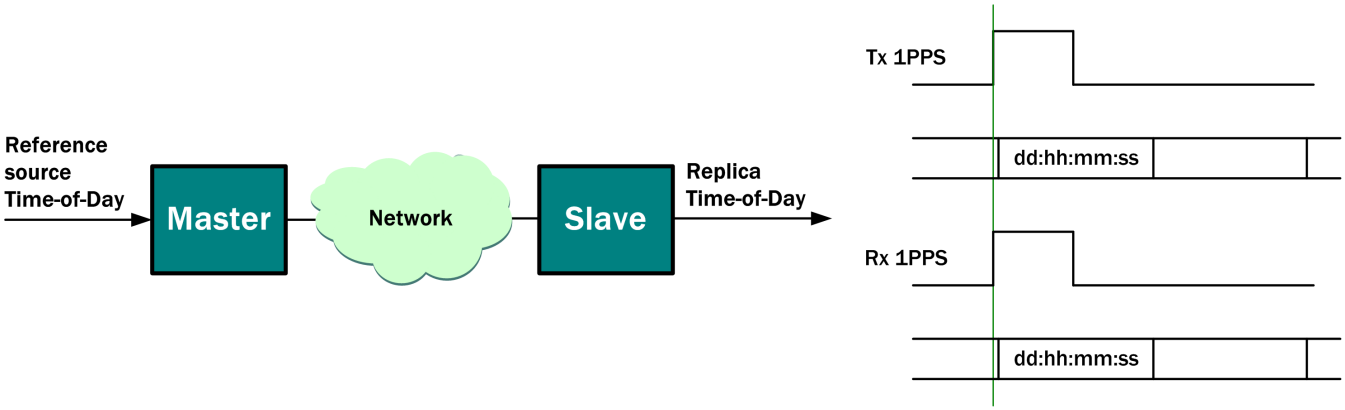



*Figure 11 - Example of ToDPSync transfer between DPSync pair*

In TAI and non-TAI traceable applications, the low-frequency clock input is used to determine the rate and phase of the timebase. The seconds rollover of the internal timebase is steered until it coincides with the rising edge of this input. In this mode, alignment to an external timebase is required, and this input must be driven by a 1 PPS signal (a 1 Hz signal generated so that the rising edge indicates the *top-of-second* point of the external time source: the end of one second and the beginning of the next).

Failures of the 1 PPS signal are detected by an activity monitor integral to the ACS9528 and the signal no longer controls the rate of change of phase of the internal timebase. In this mode, the ACS9528 goes into holdover (if it has been locked for a time sufficient to acquire good holdover data) or free-run. However, there is no automatic reference switching available because the 1PPS signal goes directly to the PTP Block. Instead, the host code has to select an alternative input port if a back-up signal is available.

## Common-phase applications

If the application requires a common phase, then the GM can be served by a ToD source, but it can also be served by a source which has an arbitrary epoch. This source would resemble a time-of-day signal but it would not necessarily be traceable to TAI; the timebase of the GM will then be traceable to the arbitrary reference epoch.

Figure 12 shows an example of the transfer of a common phase using a 1PPS as the reference.

When the ACS9528 is informed by configuration that it is not tied to a time standard which is traceable to TAI, then the internal timebase is aligned to the epoch of the supplied time source (which may not be derived from TAI, and may thus be considered to have an arbitrary phase).

Timestamps in PTP event messages are ARB timebase values, and PTP announce messages have the following flags and fields set accordingly:

PTP flag is FALSE (indicating that the timebase is not traceable to TAI).

L1 and L2 flags are FALSE.

timeTraceable flag is FALSE.

frequencyTraceable flag is TRUE.

currentUtcOffset field is invalid.

timeSource field is valid (as set by configuration).

clockClass field is as set by configuration (13, if no special profile is in use).

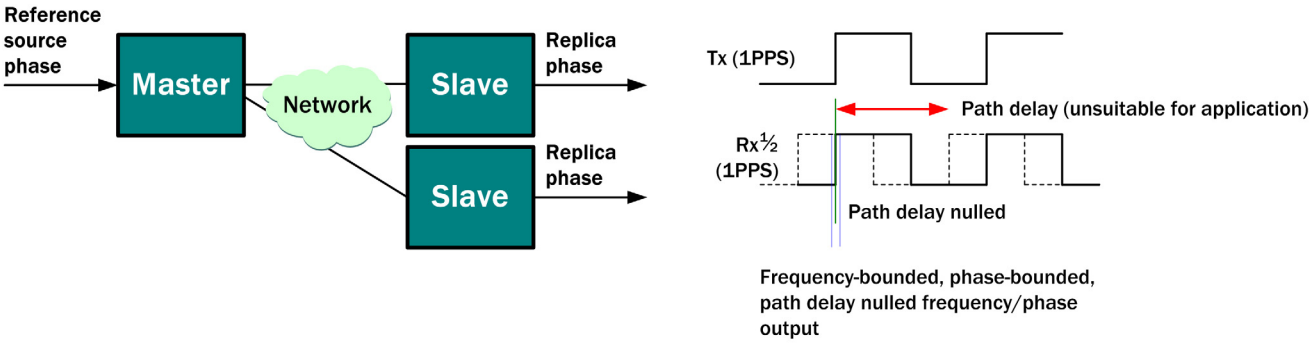



*Figure 12 - Example of common phase transfer using PPS as reference*

## Frequency-transfer applications

If the application requires a frequency only, then the GM can be served by a TAI-traceable ToD signal, an arbitrary-epoch ToD signal or a simple frequency. In the latter case, the timebase of the GM will not be traceable to any external reference epoch but will be generated internally. It will have an arbitrary phase (its own epoch) but will increase at a rate controlled by the reference frequency signal.

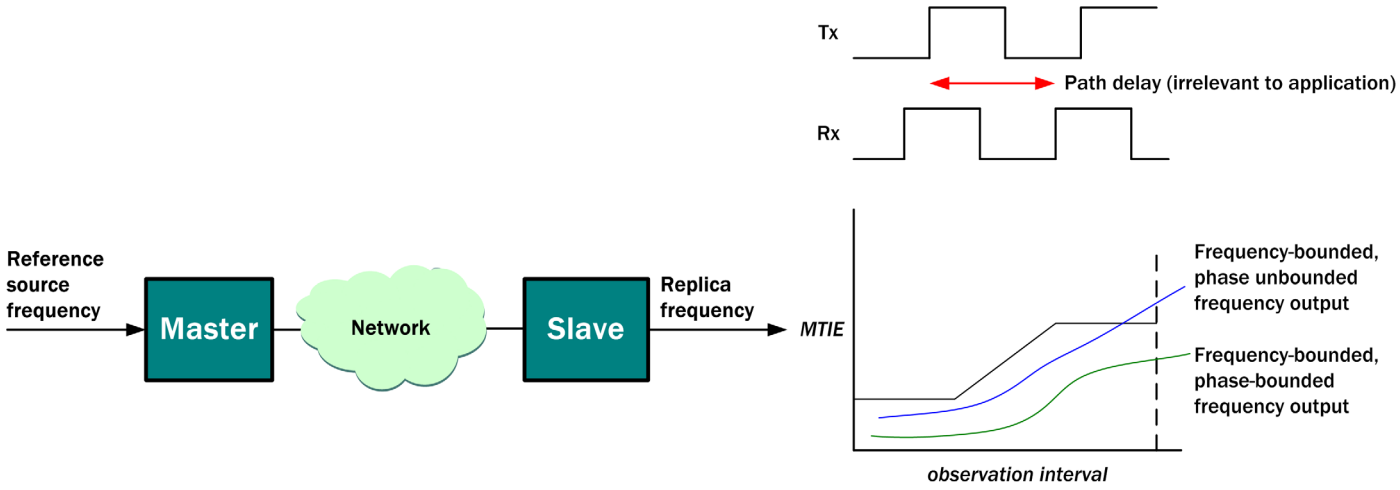



*Figure 13 - Example of internally-generated timebase*

There are two types of frequency delivery, in which the phase deviation is either bounded or unbounded. Both are examples of frequency-transfer, but have different applications. Bounded phase delivery is required by applications which need to protect buffers against overflow; circuit-emulation (e.g. psuedo-wire emulation edge-to-edge, PWE3) is an example of this sort of application. The performance requirement would be defined by MTIE and TDEV masks. Unbounded phase delivery is acceptable for applications where the frequency accuracy is the important parameter. Wireless basestations using frequency division duplex (FDD) technology are an example of where unbounded phase delivery can be used (although these have tended to obtain their timing from synchronized backhaul links, and so actually use bounded phase delivery by default).

Figure 13 shows examples of bounded-phase and unbounded-phase frequency-transfer applications.

If the application requires a bounded-phase delivery of frequency, then all potential GMs that could be selected by an OC must have the same reference source (e.g., traceable to TAI or a telecom PRC). This ensures that they operate at the same rate so that, if a reference switch is necessary, the output phase can still be bounded. If the application requires an unbounded-phase delivery, potential GMs that could be selected by the OCs must all have references that are frequency-aligned within the margins required by the application.

Figure 14 shows an example of a PTP network in which two GMs, GM1 and GM2, are tied to the same reference source (a PRC) and so support a phase-bounded frequency-transfer application; at the same time, another GM, GM3, can support a ToD application.

Although a two-way flow is not obviously necessary for the delivery of a stable frequency, it has the benefit of overcoming the large phase plateaux that occur due to long-term variations in traffic load in wide-area packet networks. These phase plateaux can cause the requirements of, for example, G.8261[20] to be violated. Using a two-way flow therefore helps to meet the G.8261[20] standard.

In frequency-transfer applications, the timebase of the ACS9528 has an arbitrary phase with respect to recognized time scales. To indicate that the ACS9528 is not tied to a TAI-traceable time source, the PTP announce messages carry the following flag and field values:

PTP flag is FALSE (indicating that the timebase is not traceable to TAI).

L1 and L2 flags are FALSE.

timeTraceable flag is FALSE.

frequencyTraceable flag is TRUE.

currentUtcOffset field is invalid.

timeSource field is INTERNAL_OSCILLATOR.

clockClass field is as set by configuration (according to special profile in use).

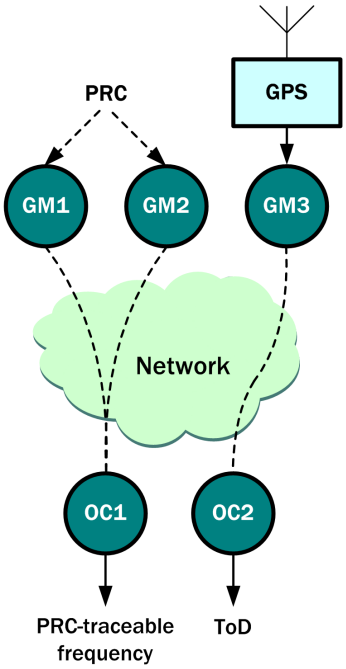



*Figure 14 - Selection of GM must suit application needs*

## Sources of error in PTP networks

PTP is a two-way protocol. It requires timing messages to flow in each direction in order that the path delay can be calculated, and accounted for, when aligning the slave timebase to the GM. Any asymmetry between the path delays of sync and delay-request messages causes an offset in the slave timebase relative to the GM timebase. This offset is an error. Asymmetry can have many causes, including differential routing where the sync messages take a different path to the delay-request messages (static asymmetry) and load-dependent delay where the delay caused by waiting in loaded queues can be different in each direction (dynamic asymmetry). Asymmetries can also be caused by physical attributes of networking equipment such as differential delays in twisted-pair cables, unbalanced delays in optical cables due to dissimilar corrections of chromatic or polarity dispersion, and differential serialization/de-serialization delays in the transceivers.

*NOTE: Static asymmetry can be compensated for within DPSync.*

Measures can be taken to minimize the effects of asymmetries. For example, differential routing can be avoided by engineering the same route in each direction; similarly, load-dependent delay asymmetry can often be minimized by appropriate use of quality-of-service facilities. These are examples of how network engineering can be applied to improve the performance of a PTP link, and they are applied at a *network level*.

Other techniques can be applied to the *physical level* of a link to improve the performance in the face of physical-layer imperfections. Serialization/de-serialization phases are often readable from the transceivers and the asymmetry can thus be calculated.

Similarly, differential delays in the two directions of a link caused by un-balanced twisting in unshielded twisted pair (UTP) cabling can often be estimated with a high degree of accuracy: for example, an estimate of the average differential delay can be obtained by taking measurements on a sample of known length and scaling up the result to suit the length of the transmission cable used. The length of the transmission cable can be estimated from the round-trip time, so that the total differential delay can be estimated automatically. This feature is not included in DPSync but can be easily implemented in the host code.

Differential delays in optical fibres due to chromatic or polarization dispersion comes into play when cables are many kilometers in length. A survey of the cable lengths can be useful in estimating differential delay. PTP v2 includes a correction field where any such information can be sent to the slave clock. DPSync will use this data to reduce the effects of asymmetry.

## Influences on Grandmaster fan-out

PTP distributes the timebase of a GM clock to a population of slave clocks. The number of slaves that can be correctly controlled by an ACS9528 running as a PTP GM depends on several factors. An important consideration is the utilization figure of the port which is receiving the delay-request messages (the incoming port). If the utilization figure is too high, head-of-line blocking may occur. This can result in the accumulation of extra delay in the slave-to-master direction which, in turn, can lead to asymmetric delay and consequent time offset error.

The same characteristic also applies to the outgoing ports of all network switches that carry PTP delay-request messages to the GM. It is important therefore to limit the average utilization of the incoming port by carefully balancing the number of slaves and the message rate.

The utilization of the port transmitting the sync, delay-response and announce messages (the outgoing port), should also be considered as a limiting factor in the number of slaves that can be supported. The outgoing link carries all of the announce, sync and delay-response messages sent by the GM to its community of slaves. Announce and delay-response messages are classed as general messages in PTP. The sync and delay-request messages are classed as event messages. In a PTP system in which a slave performs PDV filtering, best performance is obtained when the rate of delay-request messages is approximately the same as the rate of sync messages.

Each delay-request message must be answered by a corresponding delay-response message, so the rate of delay-response messages is approximately the same as that of sync messages. (In comparison, the rate of announce messages is negligibly small.) If the full capacity of an outgoing fast Ethernet link (100 Mbaud) could be devoted to carrying PTP sync and delay-response messages, the maximum aggregate rate would be approximately 76,000 messages per second. On the incoming port, this would be matched by an equal rate of delay-request messages and would produce an average utilization of some 50%. This could be expected to cause significant head-of-line blocking on the incoming link, with frequent periods of additional queueing delay and a consequent time offset error.

Reducing the utilization of the incoming port to a value nearer 20%, for example, would improve the performance and produce an insignificant time offset error. A utilization value of 20% on an incoming fast Ethernet port would allow the port to handle approximately 30,000 PTP event messages per second which could, in principle, support a population of approximately 1000 slaves at 30 messages per second. A population of this size is useful for many applications using PTP Grandmasters that can support such a population. However, it should be noted that a number of 1000 slaves exceeds that which can be supported by an ACS9528 GM.

To support a larger community of slaves, companion ACS9528 devices can be used at the same time in a network. As dictated by the PTP best master clock algorithm, a GM enters the passive state if it detects another GM on the same sub-domain, and so each of the ACS9528s must operate in its individual sub-domain. The sub-domain can be configured via the API.

## Time Stamping

Although the ACS9528 includes built-in timestamping capability, in some designs, improved performance can be achieved by capturing the sending time of the sync messages and the arrival time of the delay response messages external to the device. This is often true when there is considerable variation in delay between the ACS9528 and the Ethernet phy associated with the system's physical port, or ports, such as occurs when the traffic passes through a software router. To support, this, the ACS9528 allows for external timestamping by providing a 1PPS sync signal and a flexible frequency timestamping clock (up to 62.5 MHz) to the phy or switch which then maintains its own timebase aligned to that of the ACS9528. For outgoing sync messages the phy or switch inserts the actual sending timestamp into the message as it passes through, whereas for incoming delay request messages the arrival timestamp is captured and appended to the message in some form. The ACS9528 provides considerable flexibility in how the arrival timestamp is included in the message.Figure 15 shows the difference between internal and external timestamping.

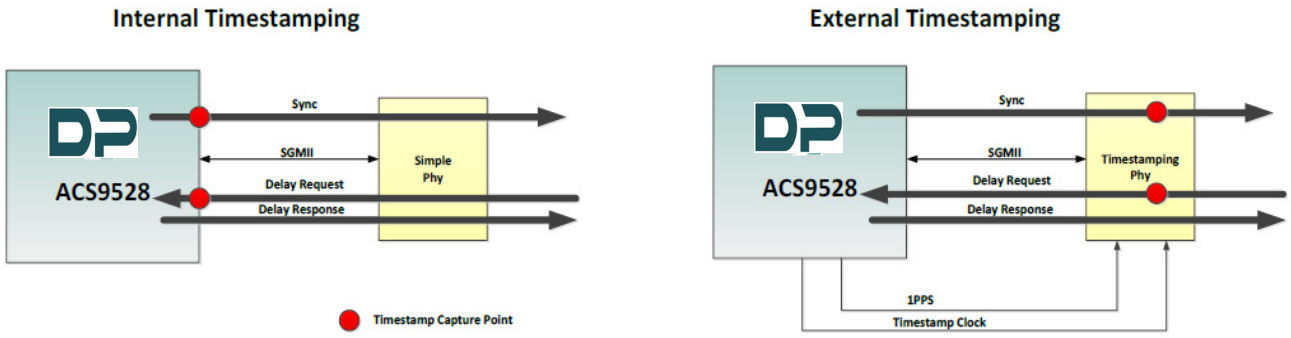



*Figure 15 - Internal and External Timestamping*

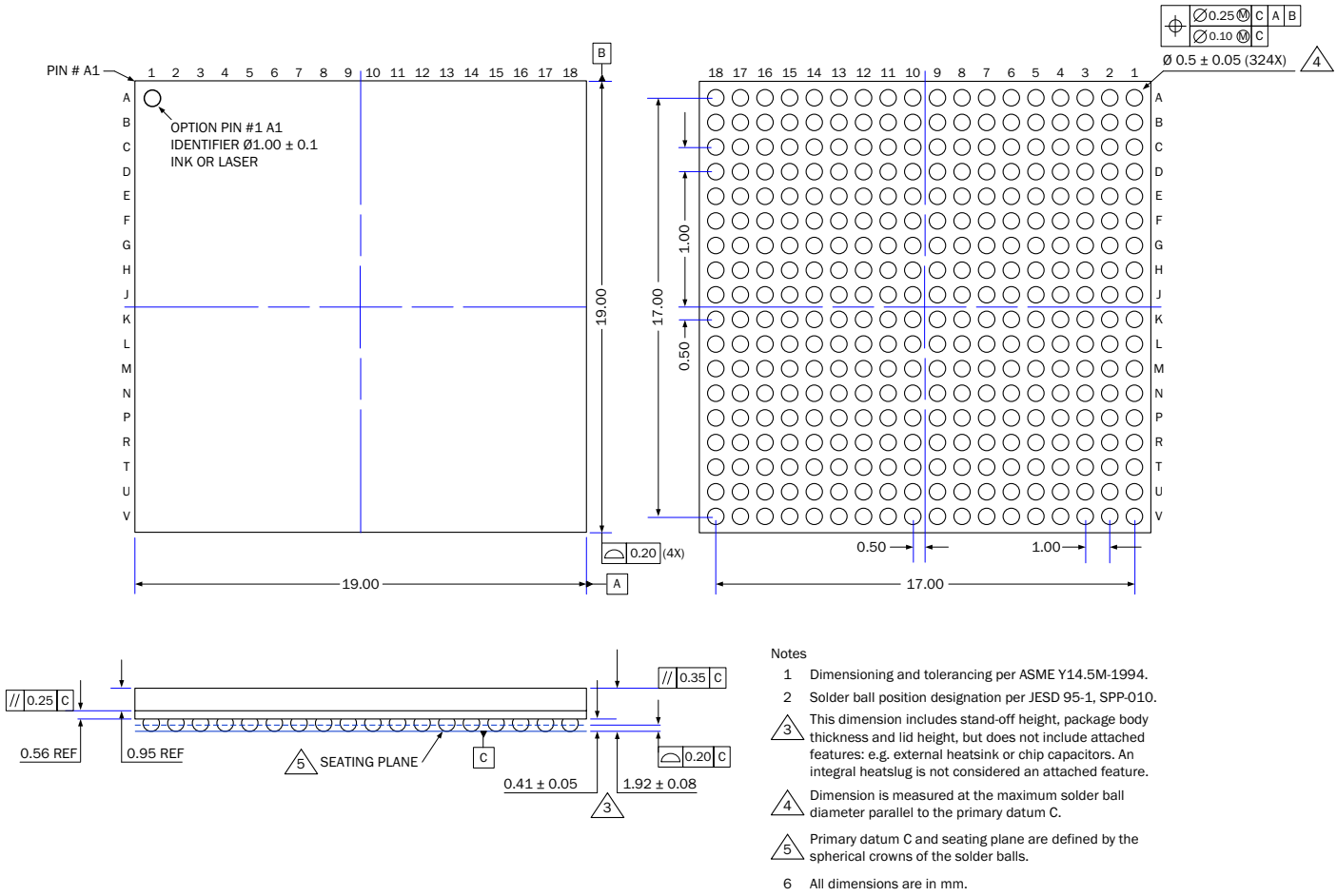
Each of the master blocks can operate using either PTP over Ethernet (layer 2) or PTP over UDP/IPv4 (layer 3) as defined in the IEEE 1588-2008 standard. The two master blocks can be used together to provide simultaneous layer 2 and layer 3 operation. When operating at layer 3, the ACS9528 implements a standard full UDP/IP stack including ARP handling and DHCP client capability.

The ACS9528 includes two separate SGMII Ethernet ports for external connection. Each port can be associated with a single master block, or both master blocks can be attached to the same port, in which case the other port is unused. This latter case is used to provide simultaneous layer 2 and layer 3 operation, or to allow the ACS9528 to be a master in two separate PTP domains at the same time. When the two ports are used independently, each can have its own IP address in separate subnets if required.

In addition to the master blocks, the ACS9528 provides a Synchronous Ethernet frequency controller that connects to an external DAPU ACS1790 device through an $I^2C$ interface. The ACS1790 provides a 25 MHz and either a 125 or 156.25 MHz clock that is phase-locked to the internal timebase and which can be used to implement Synchronous Ethernet clocking. Assuming that the network is architected to support Synchronous Ethernet, slave devices can use this clock as a stable timebase to improve performance by supplementing their local oscillators. Since the clock is derived from the same timebase as drives the PTP master blocks, the slaves can also use the Synchronous Ethernet clock to operate in a full coherent mode which typically provides much superior performance to using PTP alone.

The SPI interface allows an external CPU to both configure the ACS9528 and to extract status information. It is also used to update the embedded firmware, allowing field upgrades of the device's functionality, and to configure non-volatile configurations if desired. The SPI interface provides access to a pseudo-register based architecture consisting of a large number of virtual registers within the ACS9528. A DAPU supplied control driver, which is a thin veneer interface in processor-agnostic C source code, is implemented on the external CPU to provide functions to read and write these registers, as well as update the device firmware.

# PACKAGE DETAILS




Notes
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Solder ball position designation per JESD 95-1, SPP-010.
3. This dimension includes stand-off height, package body thickness and lid height, but does not include attached features: e.g. external heatsink or chip capacitors. An integral heatslug is not considered an attached feature.
4. Dimension is measured at the maximum solder ball diameter parallel to the primary datum C.
5. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
6. All dimensions are in mm.

***Figure 16 - LBGA package, 1.0 mm pitch, 19 mm x 19 mm x 1.92 mm, 324 balls***

MSL level 3 and peak reflow temperature = 260°C.

RoHS level = RoHS-6.

Terminal metallization (BGA balls) = SAC305.

# Thermal conditions

The ACS9528 is rated for the full temperature range of -40°C to +85°C when this package is used with a PCB of eight layers or more.

Copper coverage must exceed 50%.

All balls must be soldered to the PCB.

Maximum operating temperature must be reduced, or an appropriate airflow must be used, when the ACS9528 is used with a PCB that does not meet these minimum requirements.

***Table 32 ACS9528 thermal resistance***

| Parameter | Symbol | Airflow | Value (°C/W) |
|---|---|---|---|
| Theta-$_{JA}$ (thermal resistance - junction to ambient) | $\theta_{JA}$ | at 0 m/sec airflow<br>at 1 m/sec airflow<br>at 2 m/sec airflow | 23.2<br>17.7<br>16.8 |
| Theta-$_{JB}$ (thermal resistance - junction to board) | $\theta_{JB}$ | | 12.3 |
| Theta-$_{JC}$ (thermal resistance - junction to case) | $\theta_{JC}$ | | 5.1 |

# GENERAL INFORMATION

## Acronyms and abbreviations

| | |
|---|---|
| API | Application Programming Interface |
| APLL | Analogue Phase Locked Loop |
| ARB | Arbitrary Time Base (see IEEE 1588, v2) |
| ASSP | Application Specific Standard Product |
| BGA | Ball Grid Array |
| BITS | Building Integrated Timing Supply |
| BMC | Best Master Clock |
| BSDL | Boundary Scan Description Language |
| CMU | Clock Multiplier Unit |
| DDS | Direct Digital Synthesis |
| DFS | Digital Frequency Synthesis |
| DPLL | Digital Phase Locked Loop |
| DTO | Discrete Time Oscillator |
| EEC | Ethernet Equipment Clock |
| ESD | Electrostatic Discharge |
| GM | Grandmaster |
| GPS | Global Positioning System |
| HBD | Human Body Model |
| IEEE | Institute of Electrical & Electronics Engineers |
| I/O | Input - Output |
| ITU | International Telecommunications Union |
| LQFP | Low profile Quad Flat Pack |
| LVDS | Low Voltage Differential Signal |
| LVPECL | Low Voltage Positive Emitter Coupled Logic |
| LVTTL | Low Voltage Transistor - Transistor Logic |
| MAC | Media Access Controller |
| MII | Media Independent Interface |
| MTIE | Maximum Time Interval Error |
| NE | Network Element |
| OC | Ordinary Clock |
| OCXO | Oven Controlled Crystal Oscillator |
| PBO | Phase Build-out |
| PDV | Packet Delay Variation |
| PHY | Physical Layer Device |
| PLL | Phase Locked Loop |
| POR | Power-On Reset |
| ppb | parts per billion |
| ppm | parts per million |
| PPS | Pulse Per Second |
| PRC | Primary Reference Clock |
| PTP | Precision Time Protocol (synonymous with 1588™) |
| RoHS | Restrictive Use of Certain Hazardous Substances (directive) |
| SDH | Synchronous Digital Hierarchy |
| SEC | SDH/SONET Equipment Clock |
| SETS | Synchronous Equipment Timing Source |
| SGMII | Serial Gigabit Media Independent Interface |
| SONET | Synchronous Optical Network |
| SPI | Serial Peripheral Interface |

| | |
|---|---|
| SSM | Synchronous Status Messages |
| SSU | Synchronization Supply Unit |
| STM | Synchronous Transport Module |
| TAI | Temps Atomic International (International Atomic Time) |
| TBA | To be advised |
| TCXO | Temperature Compensated Crystal Oscillator |
| TDEV | Time Deviation |
| ToD | Time of Day |
| UART | Universal Asynchronous Receiver Transmitter |
| UDP | User Datagram Protocol |
| UI | Unit Interval |
| UTC | Universal Time, Coordinated |
| UTP | Unshielded Twisted Pair |
| W-CDMA | Wide Code Division Multiple Access, one of several 3G radio interface standards |
| WEEE | Waste Electrical and Electronic Equipment (directive) |
| 3G | 3rd Generation - an ITU specification for increased bandwidth cellular communications |
| 3GPP | 3rd Generation Partnership Project |

# References and related standards

[1] DPSync Resource Center.

[2] ANSI T1.101-1999 (1999)
Synchronization Interface Standard.

[3] AT & T 62411 (12/1990)
ACCUNET® T1.5 Service description and Interface Specification.

[4] ETSI ETS 300 462-3, (01/1997)
Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 3: The control of jitter and wander within synchronization networks.

[5] ETSI ETS 300 462-5 (09/1996)
Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 5: Timing characteristics of slave clocks suitable for operation in Synchronous Digital Hierarchy (SDH) equipment.

[6] IEEE 1149.1 (1990)
Standard Test Access Port and Boundary-Scan Architecture.

[7] IEEE 802.3 xxx.

[8] ITU-T G.703 (10/1998)
Physical/electrical characteristics of hierarchical digital interfaces.

[9] ITU-T G.736 (03/1993)
Characteristics of a synchronous digital multiplex equipment operating at 2048 kbit/s.

[10] ITU-T G.742 (1988)
Second order digital multiplex equipment operating at 8448 kbit/s, and using positive justification.

[11] ITU-T G.783 (10/2000)
Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks.

[12] IEEE Std 802.3 (2005)
Revision of IEEE Std 802.3-2002 including all approved amendments.

[13] IEEE Std. 1588 (2008)
1588™ IEEE Standard for a precision clock synchronization protocol for networked measurement and control systems.

[14] ITU-T G.812 (06/1998)
Timing requirements of slave clocks suitable for use as node clocks in synchronization networks.

[15] ITU-T G.813 (08/1996)
Timing characteristics of SDH equipment slave clocks (SEC).

[16] ITU-T G.822 (11/1988)
Controlled slip rate objectives on an international digital connection.

[17] ITU-T G.823 (03/2000)
The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy.

[18] ITU-T G.824 (03/2000)
The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy.

[19] ITU-T G.825 (03/2000)
The control of jitter and wander within digital networks which are based on the Synchronous Digital Hierarchy (SDH).

[20] ITU-T G.8261 (former G.pactiming) - This version of the Recommendation was approved during the SG15/13 meeting, held in Geneva, 6th -17th February 2006.

[21] ITU-T K.41 (05/1998)
Resistibility of internal interfaces of telecommunication centres to surge over-voltages.

[22] Telcordia GR-253-CORE, Issue 3 (09/ 2000)
Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria.

[23] Telcordia GR-499-CORE, Issue 2 (12/1998)
Transport Systems Generic Requirements (TSGR) Common requirements.

[24] Telcordia GR-1244-CORE, Issue 2 (12/2000)
Clocks for the Synchronized Network: Common Generic Criteria.

[25] DAPU application note AN-SETS-2.

[26] RoHS Directive 2002/95/EC: Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

[27] Waste electrical and electronic equipment (WEEE) directive (2002/96/EC): directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

[28] ITU-T G.781 (06/99): Synchronization layer functions.

[29] ITU-T Recommendation G.8262 (FOR CONSENT): Timing characteristics of Synchronous Ethernet Equipment (EEC) slave clock.

[30] Cisco Systems Serial-GMII Specification. ENG-46158.

[31] Philips-NXP I²C-bus specification and user manual. UM1024, Rev.03-19 June 2007.

[32] ACS9525 Application Note.

[33] ITU-T G.8265.1 Precision time protocol telecom profile for frequency synchronization.

# Trademark acknowledgements



# Product status/datasheet revision history

## Product status

The relationship between the status of the ACS9528 within the product design cycle and this datasheet is shown in the right of the header bar at the top of the datasheet.

DRAFT DATASHEET signifies that the design is being realized but is not yet physically available. The datasheet gives advance notification of the intention of the design.

PRELIMINARY DATASHEET signifies that initial prototype devices are physically available. The content of the datasheet more accurately represents the realization of the product design.

FINAL DATASHEET signifies that the device is fully characterized. The datasheet contains measured parameter values instead of simulated values.

## Datasheet revision

This datasheet is Revision 1.0, as shown in the left footer at the bottom of each page. The changes made to this document and a summary of previous revisions are listed in Table 33. For specific changes between earlier revisions of the datasheet, please refer to the earlier revisions (where available). Always use the latest revision of the datasheet.

*Table 33 Revision history*

| Revision | Reference | Description of changes |
|---|---|---|
| 1.0 | All pages | First release of PRELIMINARY Datasheet for ACS9528. |
| 2.0 | All pages | First release of FINAL Datasheet for ACS9528. |
| 3.0 | Page 22<br>Page 26 | Table 22 updated<br>Fig 7 updated to add PORB. |

# Ordering information

***Table 34 Parts list***

| Order code | Description |
|---|---|
| ACS9528IFALBGT | DPSync Timing-over-packet synchronization technology dual channel master 1588 device.<br>Lead (Pb)-free packaged version.<br>RoHS and WEEE compliant. |

## Disclaimers

Life support - this product is not designed or intended for use in life support equipment, devices or systems, or other critical applications, and is not authorized or warranted for such use.

Right to change - changes may be made to this product without notice. Customers are advised to obtain the latest version of the relevant information before placing orders.

Compliance to relevant standards - operation of this device is subject to the user's implementation and design practices. It is the responsibility of users to ensure that equipment using this device is compliant to all relevant standards.

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