Customer Code : _____

DATASHEET

DAPU P/N: **CM54T-S128-10.00MHz**

Customer P/N: _____

DAPU			Customer Approval
Drew	Audited	Approved	
Amway.wei	Carry.Wang	James.Liu	
Date: 2017.04.10			Stamp, please! Thanks!

Guangdong Dapu Telecom Technology Co.,Ltd

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Table of amendment

Version	Revision contents	Prepared by	Revised date
1.0	The first issued	Amway	2017.04.10

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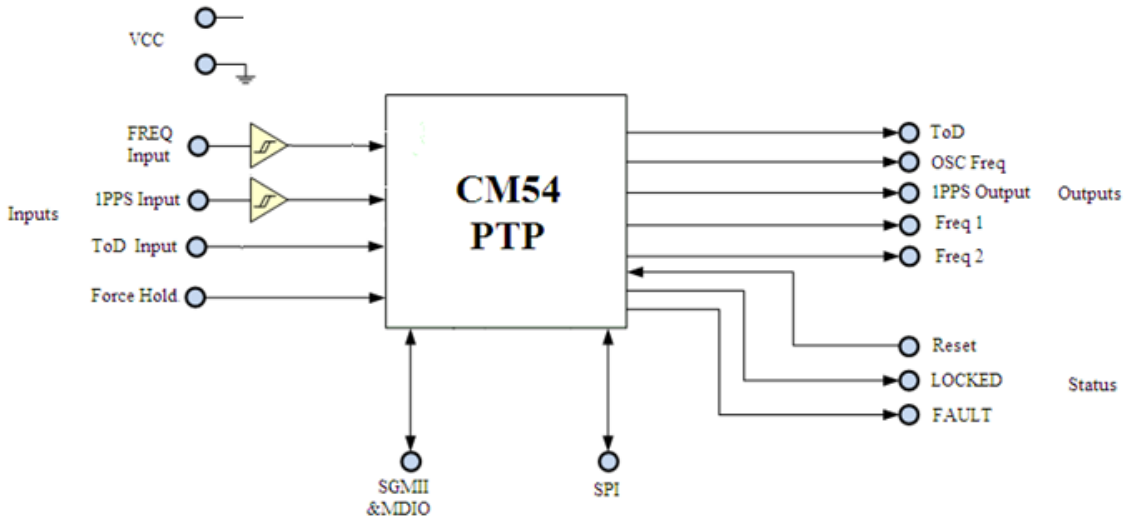
1. CM54 PTP



ABOUT THE CM54

The CM54 PTP supports:

Timebase derived from:

PTP slave, SONET/SDH recovered clock, BITS/SSU input, SyncE recovered clock, GPS, 1PPS, precision holdover. Physical layer clock sources are jitter and wander attenuated according to G.812, G.813, G.8261, G.8262, GR-1244-CORE, GR253 etc.

PTP Grandmaster:

PTP Grandmaster function supports multiple PTP slaves using multicast or unicast messaging. Timebase may be PTP or ARB.

PTP Slave:

Acting as a PTP Ordinary Clock in Slave mode, the CM54 can lock to BCs or TCs, or it can use sophisticated packet delay filters and adaptation algorithms to lock to a remote PTP Grandmaster over a multi-hop legacy network which has no PTP support.

Self test- the device self-checks for consistency and makes rudimentary checks of the external Ethernet PHYs.

Time-aligned output pair:

1 PPS and 125 MHz divided by n (n = 4 to 125000).

Frequency-aligned outputs:

1 Hz and programmable frequency 1 kHz to 180 MHz.

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2. Electrical Parameters

2.1 Input/Output reference clocks

There are 7 clock reference inputs, 6 clock outputs, using these variety of I/O technologies:

- LVDS
- TTL

2.1.1 LVDS input and output ports

Table 1 DC characteristics of the LVDS input and output ports

Across all operating conditions , unless otherwise stated.

Parameter	Symbol	Min	Typ	Max	Unit
LVDS input voltage range. Differential input voltage = 100 mV.	V_{VRLVDS}	0		2.4	V
LVDS differential input threshold.	V_{DITH}	-100		100	mV
LVDS input differential voltage.	$V_{IDLVTSDS}$	0.1		1.4	V
LVDS input termination resistance.	R_{TERM}	95	100	105	Ω
LVDS output high voltage.	V_{OHLVDS}			1.585	V
LVDS output low voltage.	V_{OLLVDS}	0.885			V
LVDS differential output voltage.	V_{ODLVDS}	250		450	mV
LVDS change in magnitude of differential output voltage for complementary states.	$V_{DOSLVDS}$			25	mV
LVDS output offset voltage. Temperature = 25℃	V_{OSLVD}	1.125		1.375	V

Note that Table 1is only applicable to IPCLK8P/N, IPCLK11P/N, OPCLK4P/N and OPCLK5P/N when configured in LVDS mode.

2.1.2 TTL ports

Table 2 DC characteristics of the TTL ports

Parameter	Symbol	Min	Typ	Max	Unit
TTL input port					
V_{IN} High.	V_{IH}	2			V
V_{IN} Low.	V_{IL}			0.8	V
Input current.	I_{IN}			10	μ A
TTL input port with internal pull-up					
V_{IN} High.	V_{IH}	2			V
V_{IN} Low.	V_{IL}			0.8	V
Pull-up resistor.	P_U	20		200	kΩ
Input current.	I_{IN}			100	μ A
TTL input port with internal pull-down					
V_{IN} High.	V_{IH}	2			V
V_{IN} Low.	V_{IL}			0.8	V
Pull-down resistor.	P_D	20		200	kΩ

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Input current.	I_{IN}			100	μ A
TTL output port (OPCLKx, 1PPSOUTx)					
V_{OUT} Low (l_{OL} = 8 mA).	V_{OL}	0		0.4	V
V_{OUT} High (l_{OH}= 8 mA).	V_{OH}	2.4			V
Drive current.	I_D	-8		8	mA
TTL output port (other pins)					
V_{OUT} Low (l_{OL} = 4 mA).	V_{OL}	0		0.4	V
V_{OUT} High (l_{OH}= 4 mA).	V_{OH}	2.4			V
Drive current.	I_D			4	mA

2.2 SGMII interface

The CM54 has two serial SGMII interfaces running with a 100 Mbps data rate and a 1.25 Gbps line rate. The interfaces are IEEE 802.3[7]compliant for communication via a suitable packet PHY.

Table 3 SGMII output data AC characteristics

Symbol	Parameter	Min	Typ	Max	Unit
DR	Serial data rate		1.25		Gbits/sec
t_{FALL}	Vod fall time (80% to 20%)	100		200	picosec
t_{RISE}	Vod rise time (20% to 80%)	100		200	picosec
t_{SKEW}	Skew between two members of a differential pair:[tp_{HLP}- tp_{LHN}] or [tp_{LHP}- tp_{HLN}]			±20	picosec

Table 4 SGMII output data DC characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}	Output voltage high state			1525	mV
V_{OL}	Output voltage low state	875			mV
V_{OD}	Output differential voltage	150		400	mV

Table 5 SGMII input data AC characteristics

Symbol	Parameter	Min	Typ	Max	Unit
D_{RT}	Serial input data rate tolerance	-300		+300	ppm

Table 6 SGMII input data DC characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_I	nput voltage range	675		1725	mV
V_{IDTH}	Input differential threshold	50		400	mV
V_{OD}	Input differential voltage	150		400	mV
R_{IN}	Differential input impedance	80		120	Ω

2.3 Serial peripheral interface

The serial peripheral interface (SPI) is a slave port for communication with a serial microprocessor bus, allowing the CM54 to be controlled by an external processor. The serial interface header must be connected to the host processor, which acts as the master. The CM54 requires data to be transmitted LSB first, MSB first is not supported.

Figure 1 and Table 7 show the read access timing for the serial interface. The data is sampled on the rising edge and driven on the falling edge.

Figure 2 and Table 8 show the write access timing for the serial interface. The data is sampled on the rising edge and driven on the falling edge.

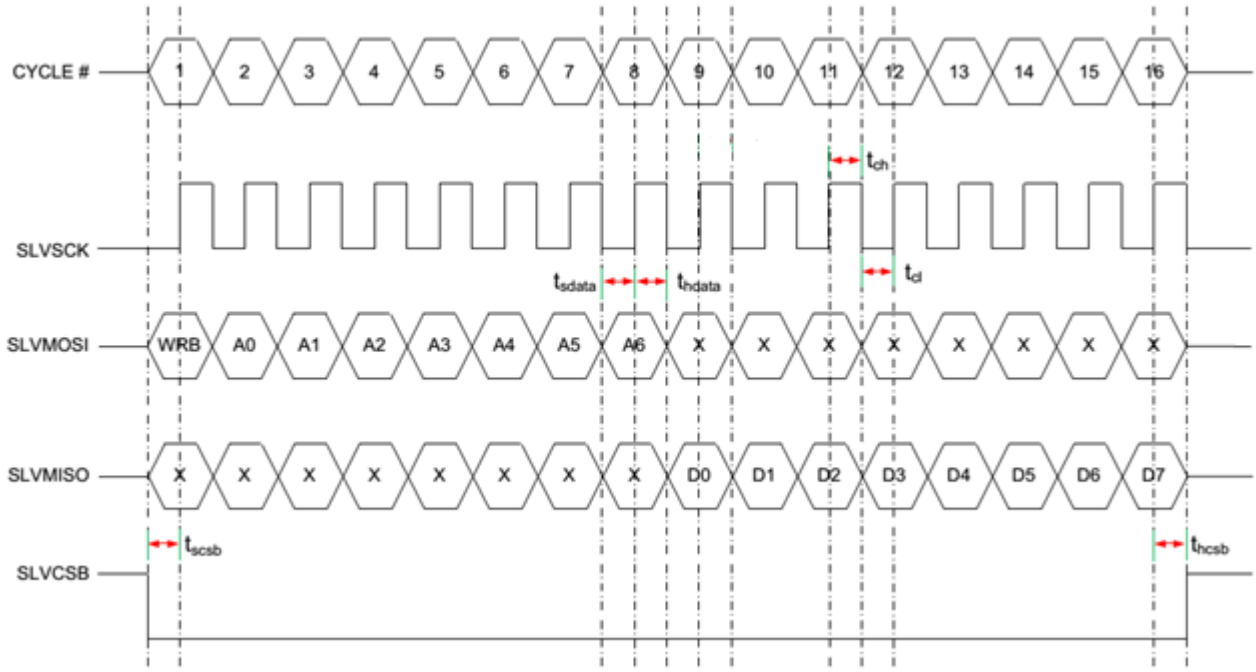

Figure 1-Read access timing of the serial interface

Table 7 Serial interface read access timing data

Symbol	Parameter	Min	Typ	Max	Unit
F_{sck}	SPI clock frequency			10	MHz
t_{sdata}	Setup MOSI valid to $SCK_{rising\ edge}$	4			ns
t_{scsb}	Setup $CSB_{falling\ edge}$ to $SCK_{rising\ edge}$	14			ns
t_{d1}	Delay $SCK_{falling\ edge}$ to MISO valid			45	ns
t_{d2}	Delay $CSB_{rising\ edge}$ MISO high-Z		45		ns
t_{cl}	SCK Low time	45			ns
t_{ch}	SCK High time	45			ns
t_{hdata}	Hold MOSI valid after $SCK_{rising\ edge}$	6			ns
t_{hcsb}	Hold CSB low after $SCK_{rising\ edge}$	6			ns
t_p	Time between accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	45			ns

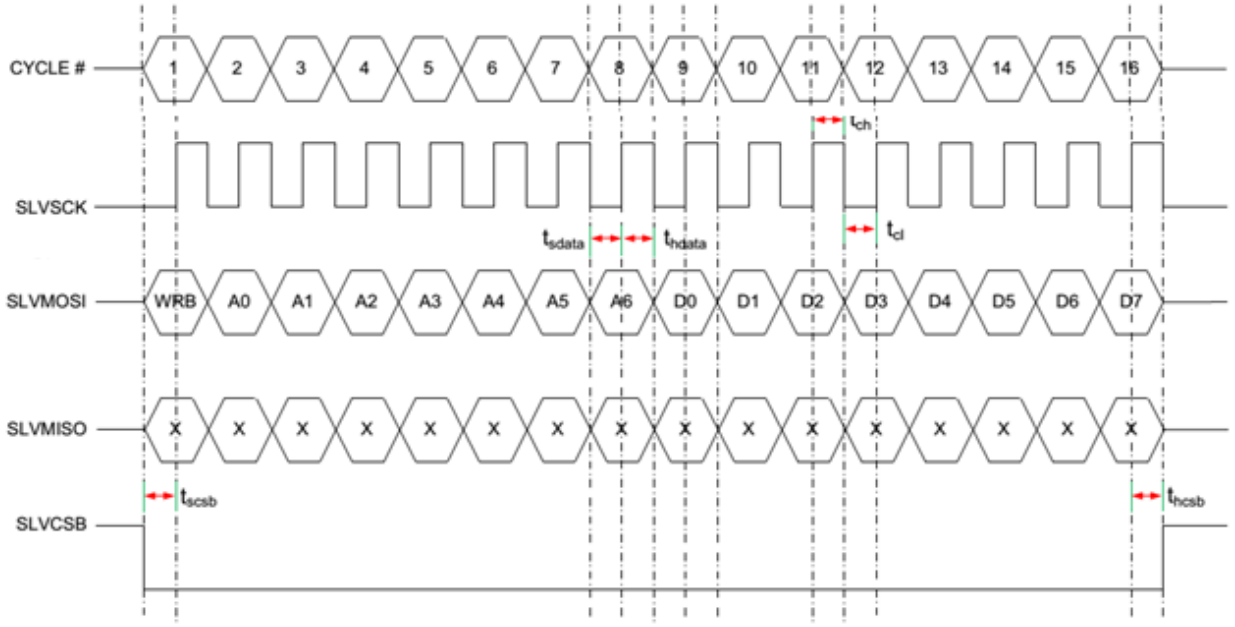

Figure 2 -Write access timing of the serial interface

Table 8 Serial interface write access timing data

Symbol	Parameter	Min	Typ	Max	Unit
F_{sck}	SPI clock frequency			10	MHz
t_{sdata}	Setup MOSI valid to $SCK_{rising\ edge}$	4			ns
t_{scsb}	Setup $CSB_{falling\ edge}$ to $SCK_{rising\ edge}$	14			ns
t_{d1}	Delay $SCK_{falling\ edge}$ to MISO valid			45	ns
t_{d2}	Delay $CSB_{rising\ edge}$ MISO high-Z		45		ns
t_{cl}	SCK Low time	45			ns
t_{ch}	SCK High time	45			ns
t_{hdata}	Hold MOSI valid after $SCK_{rising\ edge}$	6			ns
t_{hcsb}	Hold CSB low after $SCK_{rising\ edge}$	6			ns
t_p	Time between accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	45			ns

2.4 Time of day message format

The ToD message format can be a GPRMC message or one of a group of other GPS messages or proprietary messages to suit specific causes.

2.4.1 GPRMC message format

A GPRMC message has the format $GPRMC,122356,A,0000.0000,N,00000.0000,W,0.0.0.0,120508,,,A*F6 in which the commas are separators. The architecture of the message is shown in Table 18. The message is 62

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characters in length (i.e. 62 bytes). No parity bit is used, but each byte has a stop bit.

Table 9 Architecture of GPRMC message

Elements	Description
$GPRMC	Message header.
122356	UTC value.
A	Status (A = active, V = void).
0000.0000,N	Latitude, north (fixed to zero).
00000.0000,W	Longitude, west (fixed to zero).
0.0	Speed over ground (fixed to zero).
0.0	Track angle (fixed to zero).
120508	Date (ddmmyy).
A	A = autonomous, D = differential, E = estimated, S = simulation, N = not valid.
*F6	Checksum.

2.5 Jitter tolerance of the 1PPS input

The CM54 will reject a 1PPS signal if the jitter is greater than 4 μs peak-to-peak. However, it is strongly recommended that jitter on this signal is avoided as much as possible because the distribution of jitter on this signal is not known and so cannot be correctly attenuated by filtering. Any filtering applied to this signal will introduce a phase offset error. This treatment differs from that of more traditional reference sources because the phase of a 1PPS signal, relative to a recognised source of time such as UTC, is the parameter of most significance. For other references, the rate (frequency) is the more significant parameter.

2.6 Time of day port

A ToD port is used in PTP Timing modes only. In PTP GM mode, the port is an input comprising UARTRX and a 1 PPS signal. In PTP Slave mode, the port is an output comprising UARTTX and a PPnS signal, which gives a pulse every n seconds (t_W configurable for a minimum of 100 ns to a maximum of 400 ms). The UART has an integrated baud rate generator using 1 stop bit and no parity. The maximum baud rate of the UART port is 19200 baud.

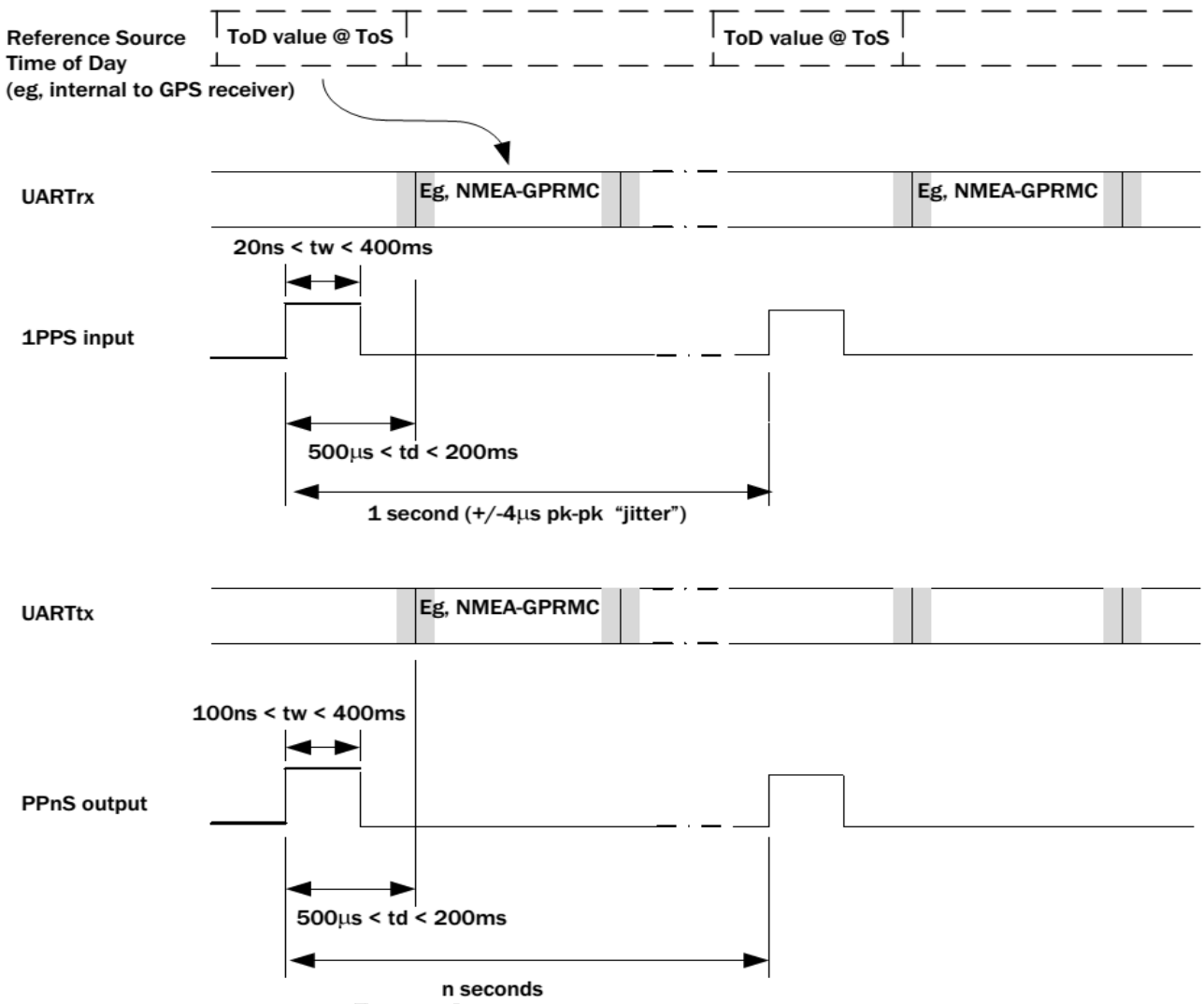

Figure 3 - ToD port timing

2.7 Reset

Active low. Must be active low for a minimum of 100 ns. If Reset is forced low, all internal states are reset to default values.

2.8 Locked status

Indicates (active high) that the device has achieved lock to the selected reference. The degree of lock indicated is software defined. The LOCKED pin is used in PTP and self test modes only.

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3. Performances of CM54

Recovery Capability	Recovery time	Min	Typ	Max	Unit	Test Condition
	24 Hours	-200		200	ns	ΔT=±5℃， Test after Power on 30 min
Holdover Capability	Holdover Time	Min.	Typ.	Max.	Unit.	Test Condition
	24 Hours	-44		+44	μs	ΔT=±5℃, 24 hours holdover after turn on and lock2days
Supply Voltage	Parameters	Min.	Typ.	Max.	Unit.	Test Condition
	Supply Voltage	4.75	5.0	5.25	V	
	Current Consumption			2000	mA	During Warm-up
				1000	mA	During steady state operation @25℃
	AC Ripple			50	mVpk-pk	10Hz to 1MHz

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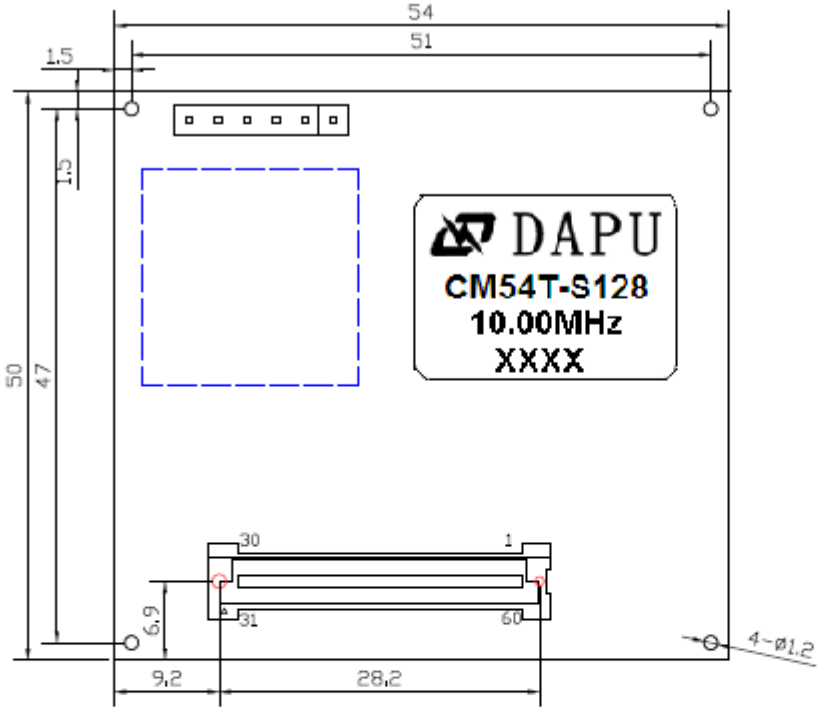
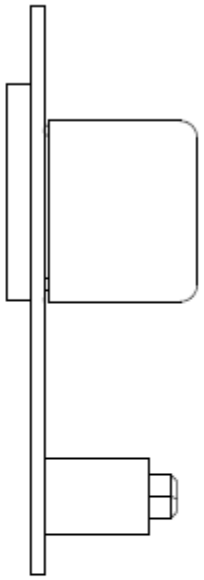
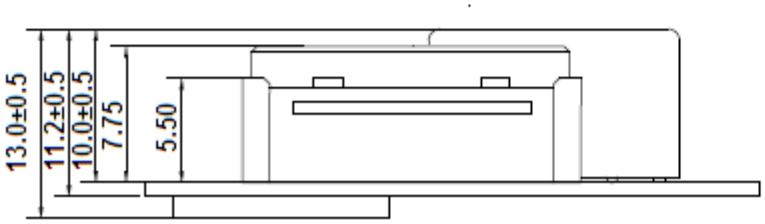
4. Mechanical Structure(mm)



Top view



Right view



Front view

Note1: Tolerance ± 0.2mm without mark
The height of connector is optional.

Note2: The first two xx representative: week
After two xx representative: year

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60 Pins Connections			
PIN	NAME	I/O	DESCRIPTION
1	VCC		Power supply input, 4.75V to 5.25V
2	IPCLK1	I	Clock reference input. Acceptable frequencies into the PTP module from: 1 PPS/1 Hz to 161MHz (input reference for PTP Master).
3	IPCLK0	I	
4	RESET	I	Reset the PTP module
5			Suspended, reserved
6	GND	I	
7		I	Suspended, reserved
8	GND		
9	IPCLK11NEG	I	Clock reference input 11. TDM module only. Differential input. Programmable input frequencies to a maximum of 155.52 MHz. Default 19.44 MHz. Default signal type LVPECL.
10	IPCLK11POS	I	
11	GND		
12	IPCLK12	I	Clock reference input.TDM module only. Acceptable frequencies directly into the TDM module: n × 8 kHz 1.544 MHz (SONET)/2.048 MHz (SDH) 6.48 MHz 19.44 MHz 25.92 MHz 38.88 MHz 51.84 MHz 77.76 MHz (Pull low if not used)
13	GND		
14	SGMIITXP1	O	PTP port 1,SGMII interface
15	SGMIITXN1	O	
16	SGMIIRXP1	I	
17	SGMIIRXN1	I	
18	GND		
19	IPCLK13	I	Clock reference input 13. TDM module only. Acceptable input frequencies as IPCLK12. (Pull low if not used).
20	OPCLK8	O	Clock reference output 8. TDM module only. Same clock frequency configuration options as

			OPCLK0. For operation in TDM Timing mode.
21	GND		
22	SGMIIRXN0	I	PTP port 0,SGMII interface
23	SGMIIRXP0	I	
24	SGMIITXN0	O	
25	SGMIITXP0	O	
26	GND		
27	1PPS_OUT1	O	The clock module 1PPS output port1.
28	UARTRX0	I	Time of day interface, NMEA 0183 or UBX protocol, The UART has an integrated baud rate generator using 1 stop bit and no parity. The maximum baud rate of the UART port is 19200 baud.
29	UARTTX0	O	
30	VCC		Power supply input, 4.75V to 5.25V
31	VCC		Power supply input, 4.75V to 5.25V
32	LOCKED	O	State output. Output high level when the CM is locked and stable, others low level.
33	FAULT	O	Fault alarm.
34	GND		
35	UARTRX1	I	Time of day interface, NMEA 0183 or UBX protocol, The UART has an integrated baud rate generator using 1 stop bit and no parity. The maximum baud rate of the UART port is 19200 baud.
36	UARTTX1	O	
37	GND		
38	MDIO	I/O	MII data input/output
39	MDC	O	MII CLK
40	GND		
41	OPCLK7	O	Clock reference output 7. TDM module only. Same clock frequency configuration options as OPCLK0. For operation in TDM Timing mode.
42	GND		
43	OPCLK4POS	O	Clock reference output 4. Default frequency 77.76 MHz. Default signal type LVDS.
44	OPCLK4NEG	O	
45	GND		
46	OPCLK0	O	Time-aligned output pair: 125 MHz divided by n (n = 4 to 125000) maximum of 25MHz MHz (divide by 4) minimum of 100 Hz (divide by 1249999) Frequency-aligned outputs: programmable frequency 1 kHz to 62.5MHz

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47	GND		
48	1PPS_OUT0	O	The clock module 1PPS output port0
49	OPCLK1	O	Clock reference output 1. Same clock frequency configuration options as OPCLK0.
50	GND		
51	IPCLK2	I	Clock reference input 2. PTP or TDM module. Acceptable input frequencies as IPCLK0. (Pull low if not used).
52	GND		
53	SLVSCLK	I	SPI interface, The serial peripheral interface (SPI) is a slave port for communication with a serial microprocessor bus, allowing the module to be controlled by an external processor.
54	SLVMOSI	I	
55	SLVINT	O	
56	SLVCSB	I	
57	SLVMISO	O	
58	GND		
59			Suspended, reserved
60	VCC		Power supply input, 4.75V to 5.25V

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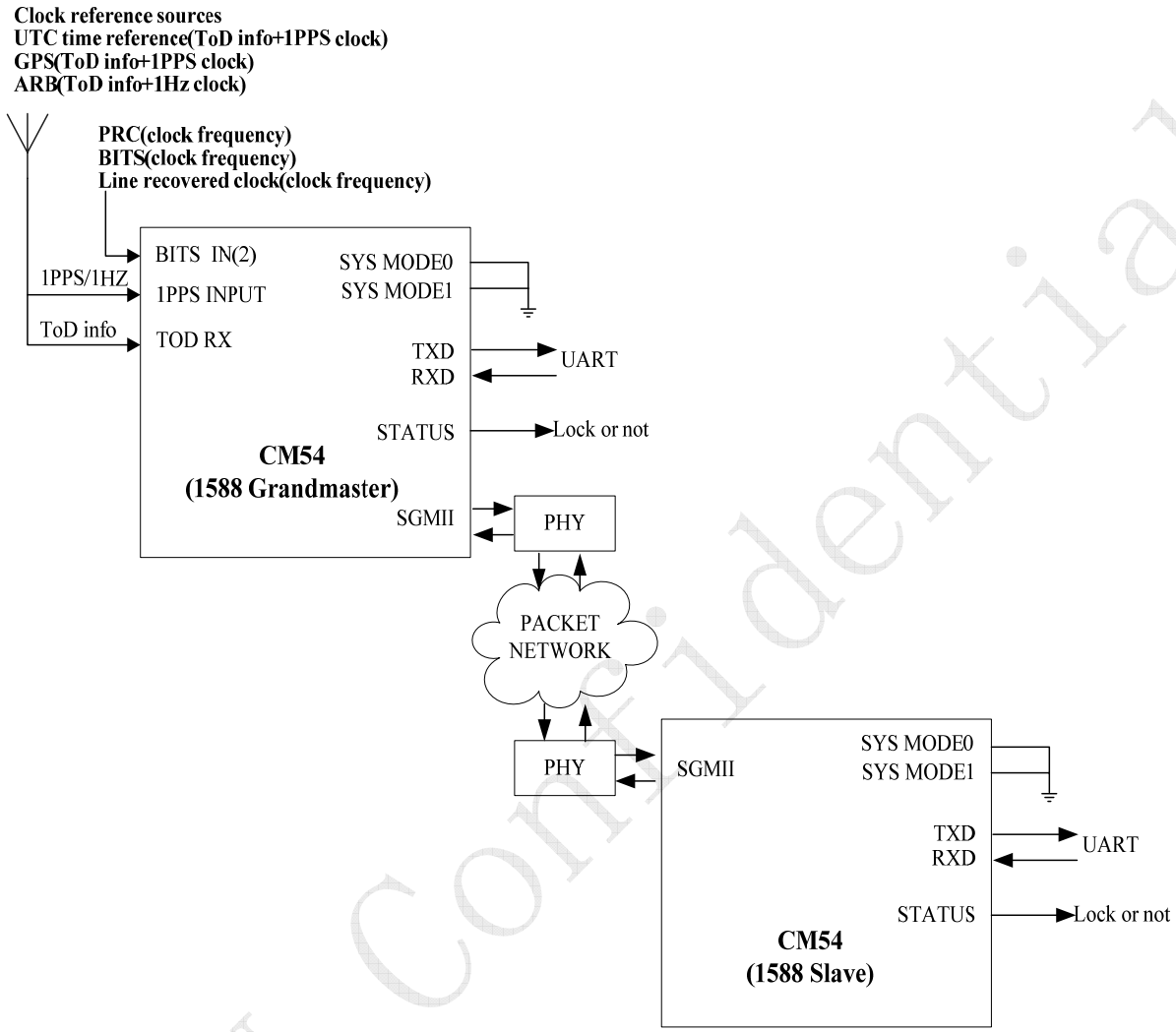
5.Application Information

Typical application 1



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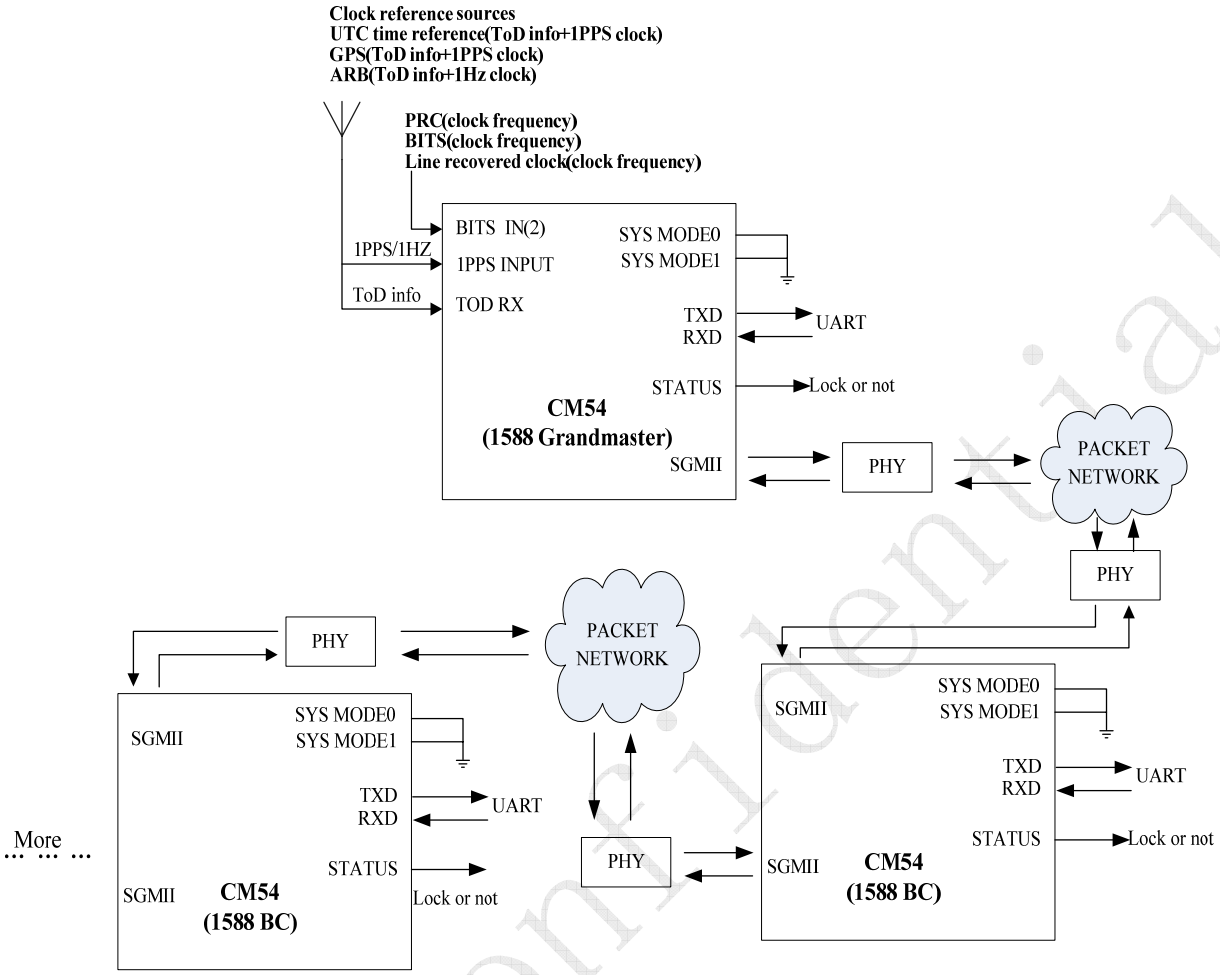
Typical application 2



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6.Coding Rules

CM XX X - X X X X - XX.XX MHz

Clock Module

Output Frequency

Size		Height		Holdover Capability				Supply Voltage		Output Waveform		Operating temperature	
65	65×65(mm)	A	Without GPS Receiver,single Freq.19mm	A	±1.5μs	ΔT=±30℃	24hours	1	5.0V	1	Sine Wave	8	-40℃~85℃
55	50×50(mm)	B	Without GPS Receiver,single Freq.15mm	W	±1.5μs	ΔT=±15℃	24hours	3	3.3V	2	HCMOS	9	-20℃~75℃
22	20×20(mm)	F	Without GPS Receiver,single Freq.13mm	D	±1.5μs	ΔT=±5℃	24hours						
				E	±3.0μs	ΔT=±5℃	24hours						
66	60×60(mm)	G	Build-in GPS Receiver,single Freq.13mm	F	±8.0μs	ΔT=±5℃	24hours						
		H	Build-in GPS Receiver,dual-Freq.13mm	J	±80μs	ΔT=±5℃	24hours	*1					
		K	Build-in GPS/BeiDou Receiver,single Freq.13mm	S	±44μs	ΔT=±5℃	24hours	*2					
		L	Build-in GPS/BeiDou Receiver,dual-Freq.13mm										
77	75×75(mm)	P	13mm,PTP Function,SMT										
33	35×35(mm)	T	19mm, PTP Function,DIP										
54	54×50(mm)												

NOTE:*1 Power on and lock to the GPS 1PPS 2 hours
*2 Power on and lock to the PTP 48 hours
Default power on 7 days and lock to the reference source 3 days

7.Package（mm）