Travelling Merchant:_____

DATASHEET

Standard: **CM33B-A118-25.60MHz**

P/N: _____

Plot			The Label
Drew	Audited	Approved	
Amway.wei	Steven.Sun	James.Liu	
Date: 2014.07.15			Stamp, please! Thanks!

Guangdong Dapu Telecom Technology Co.,Ltd

Bldg13-16,.N.Ind.Zone,SSL Industry Park, GuangDong City, Guangdong Province, China

TEL：0086-0769-88010888 FAX：0086-0769-81800098

Bldg13-16,.N.Ind.Zone,SSL Industry Park, Dongguan City, Guangdong Province, PRC China
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FAX:0086-0769-81800098

Table of amendment

Version	Revision contents	Prepared by	Revised date
1.0	The first issued	Amway	2014.07.15

Bldg13-16,.N.Ind.Zone,SSL Industry Park, Dongguan City, Guangdong Province, PRC China
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1. Electrical Parameters

1 PPS Reference Input	Parameters	Min.	Typ.	Max.	Unit.	Test Condition
	Waveform	HCMOS				
	High-Level Output Voltage (V_{IH})	2.7		3.4	V	50Ω
	Low-Level Output Voltage (V_{IL})			0.4	V	
	Pulse Width	10			μs	
	Connector	Pin 4				
State Input	Parameters	Min.	Typ.	Max.	Unit.	Test Condition
	1PPS IN	2.7		3.4	V	<5mA Load
	DAC IN			0.4	V	<5mA Load
	Connector	Pin 1				
RF Output	Parameters	Min.	Typ.	Max.	Unit.	Test Condition
	Nominal Frequency	25.60			MHz	Synchronization with input 1PPS
	Waveform	Sine wave				
	Level	6		10	dBm	
	Load	50			Ω	
	Harmonics/ Sub-harmonics Suppression			-30	dBc	
	Spurious Suppression			-60	dBc	
	Accuracy	−0. 05		+0.05	$\times10^{-9}$	24 hours average when locked to 1PPS after power on 2days.
	Short-term Stability	−0. 05		+0.05	$\times10^{-9}$	Temperature stability, no EMI\EMC or other interference, test after power for 1 hour ref. to 25℃; 1s, using PN9000 equipment.
	Warm-Up	-0.1		+0.1	$\times10^{-6}$	T_A=25℃, V_{cc}=5.0V constant measurement referenced to 25.6MHz, after power on 3min.
	Aging Tolerance Per Day	-3		+3	$\times10^{-9}$	Constant measurement referenced to frequency observed with T_A=25℃, V_{cc}=5.0V, after 24 hours of operation.
	Aging Tolerance Per Day	-1		+1	$\times10^{-9}$	Constant measurement referenced to frequency observed with T_A=25℃, V_{cc}=5.0V, after 30 days of operation.
	Aging Tolerance 1 Year	-0.1		+0.1	$\times10^{-6}$	

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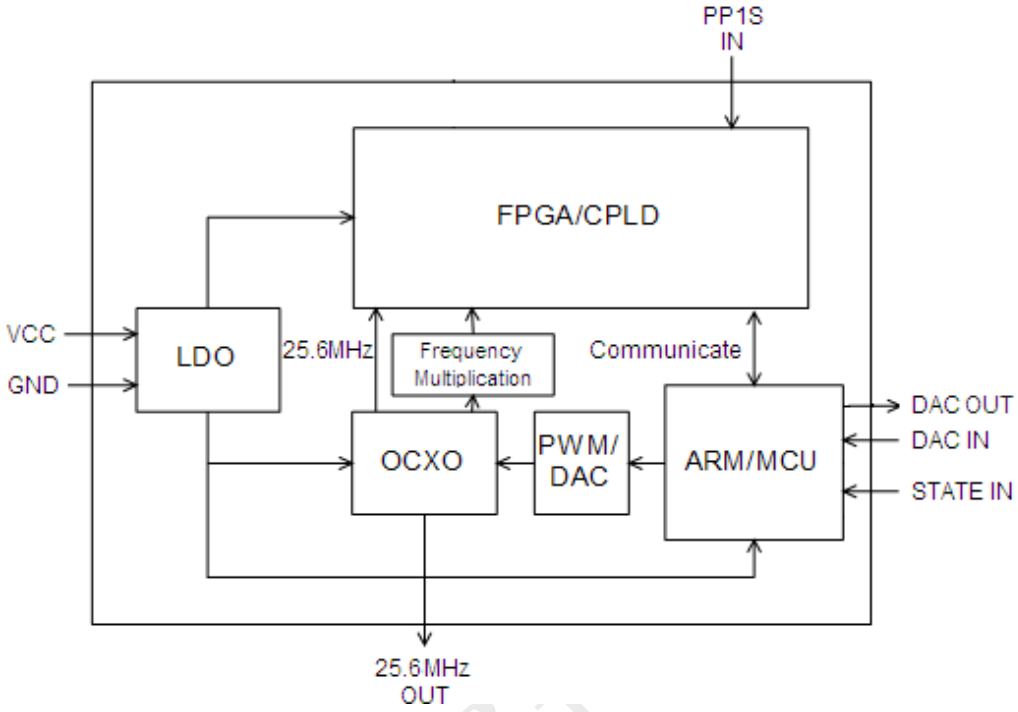
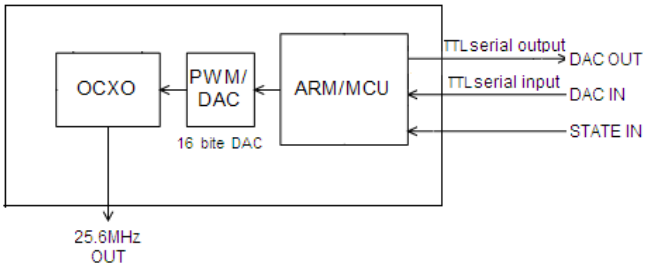
	Phase Noise (All conditions)		-100	-90	dBc/Hz	10Hz
			-125	-115		100Hz
			-143	-138		1KHz
			-150	-145		10KHz
			-150	-145		100KHz
			-150	-150		1MHz
	Connector	Pin8				
Holdover Capability	Holdover Time	Min.	Typ.	Max.	Unit.	Test Condition
	24 Hours	-5		+5	$\times10^{-9}$	(Fmax-Fmin) @ΔT=±15℃, 24 hours holdover after lock 1PPS and power on 1day. Temperature variable speed less than 2℃per minute
Supply Voltage	Parameters	Min.	Typ.	Max.	Unit.	Test Condition
	Supply Voltage	4.75	5.0	5.25	V	
	Current Consumption			600	mA	During Warm-up
				300	mA	Steady state operation @25℃
	AC Ripple			50	mVpk-pk	10Hz to 1MHz
	Connector	Pin 2				
DAC Input/ DAC Output Characteristics	Parameters	Min.	Typ.	Max.	Unit.	Test Condition
	high-level Input Voltage (VH)	2.7		3.6	V	
	low-level Input Voltage (VL)			0.4	V	
	Serial Protocol	9600-N-8-1				
	Connector	Pin5 / Pin6				
Environmental Conditions	Parameter	Conditions				
	Operating Temperature	-40℃ to 85℃				
	Storage Temperature	-55℃ to 105℃				
	Storage Humidity	30%~80%				
	ESD Level	Human Body Model,class2: 2000V to 4000V; ANSI/ESDA/JEDEC JS-001-2010.				
		Machine Model, class B: 200V to 400V; ANSI/ESDA/JEDEC JS-001-2010.				
	Moisture Sensitivity Level	Not humidity sensitive.				
	Vibration	Test Condition: 0.75mm ;acceleration:10g;10Hz～500Hz, one cycle per 30 min, test 2 hours. (3 times for each 3 directions X ,Y , Z)， IEC 68-2-06 Test Fc.				
	Shock	50g；11ms；half sine wave (3 times for each 3 directions X ,Y, Z),IEC 68-2-27 Test Ea/Severity 50A.				

2. Functional Block Diagram



3. The External DAC Control Flow



When the State In was set low or the Satellite lost, the module can adjust the OCXO 25.6MHz output frequency to track the DAC Signal of 25.6MHz with DAC Signal.

DAC communication protocol:

1. Write DAC

START	ADDRESS	R/W	RESERVED	MSB	LSB	CK	STOP

START: 0x24

ADDRESS: 0x50

R/W: Read: 0x00

Write: 0x01

RESERVED: 0x02

CK: CHECKOUT. CK=START xor ADDRESS xor R/W xor RESERVED xor STOP

MSB: the 16 bite DAC big eight

LSB: the 16 bite DAC low eight

STOP: 0x01

Eg.

When the DAC IN sent “24 50 01 02 00 01 76 01”, that means write DAC “0x0001”

DAC Output sent “24 50 02 02 00 01 75 01”

2. Read DAC

START	ADDRESS	R/W	RESERVED	MSB	LSB	CK	STOP

START: 0x24

ADDRESS: 0x50

R/W: Read: 0x00

Write: 0x01

RESERVED: 0x02

CK: CHECKOUT. CK=START xor ADDRESS xor RESERVED xor RESERVED xor STOP

MSB: the 16 bite DAC big eight

LSB: the 16 bite DAC low eight

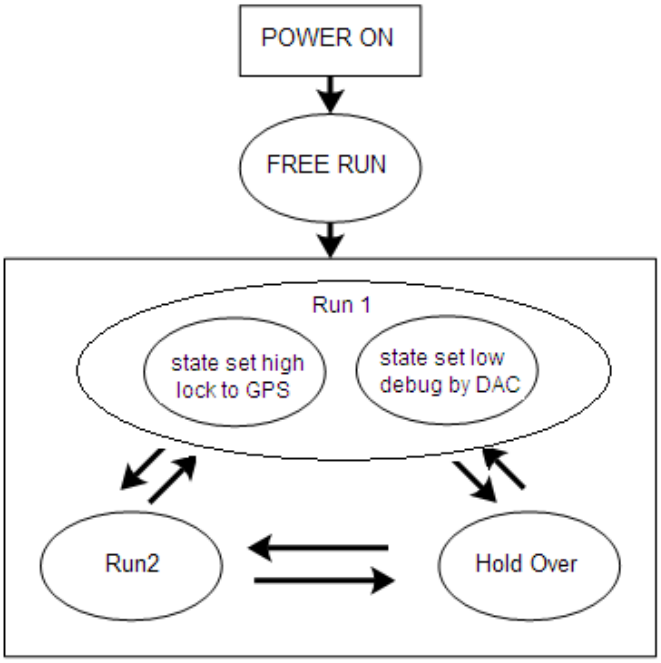
STOP: 0x01

Eg.

IF the DAC was set “0x8000”

When the DAC IN sent “24 50 00 02 XX XX 77 01”, DAC Output sent “24 50 00 02 80 00 75 01”.

4. Workflow Diagram



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Run1: Fast track.

State High : adjust the OCXO 25.6MHz output frequency quickly to track the PP1S of 25.6MHz with PP1S reference.

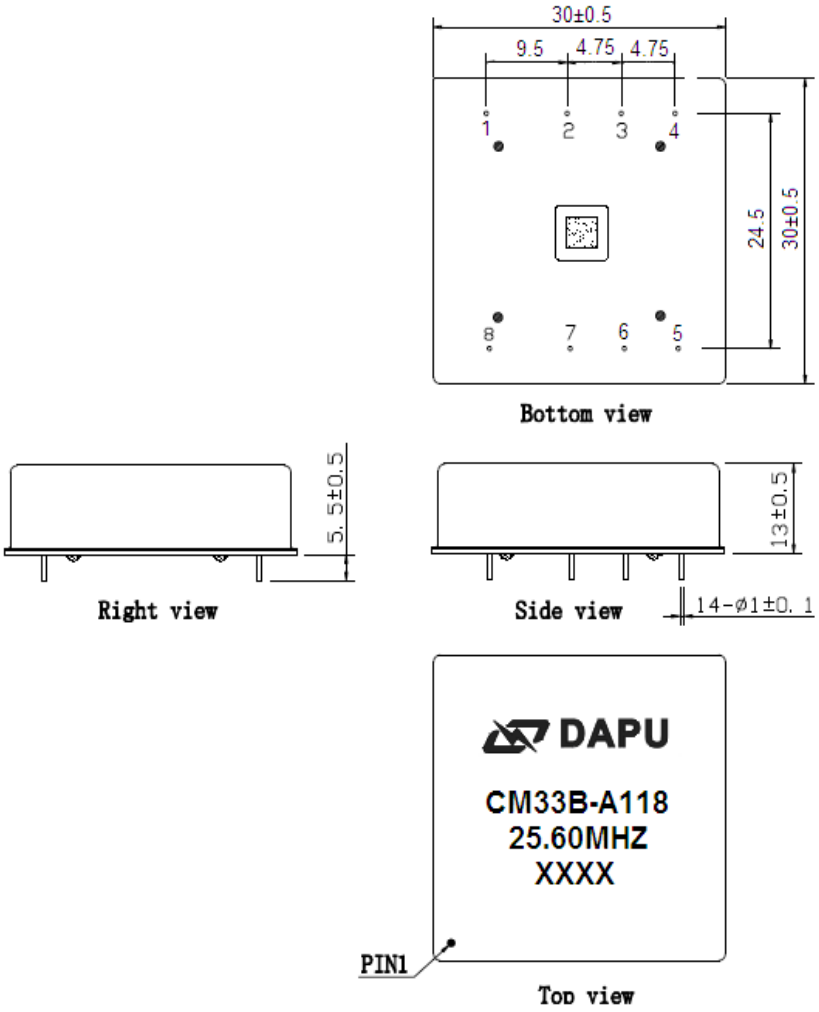
State Low : adjust the OCXO 25.6MHz output frequency quickly to track the DAC Signal of 25.6MHz with DAC Signal.

Run2: Slow track. Adjust the OCXO 25.6MHz output frequency slowly in order to synchronization with the PP1S reference when the phase error is in the define range.

Hold Over: PP1S reference and DAC Signal fixed, an algorithm has been developed which enables adaptive modeling of the frequency stability of OCXO with reference to GPS PP1S signal.

Free Run: Clock module power on without PP1S reference or DAC fixed before Fast track.

5. Mechanical Structure(mm)



Note1: Tolerance ±0.2mm without mark

Note2: The first two xx representative: week

After two xx representative: year

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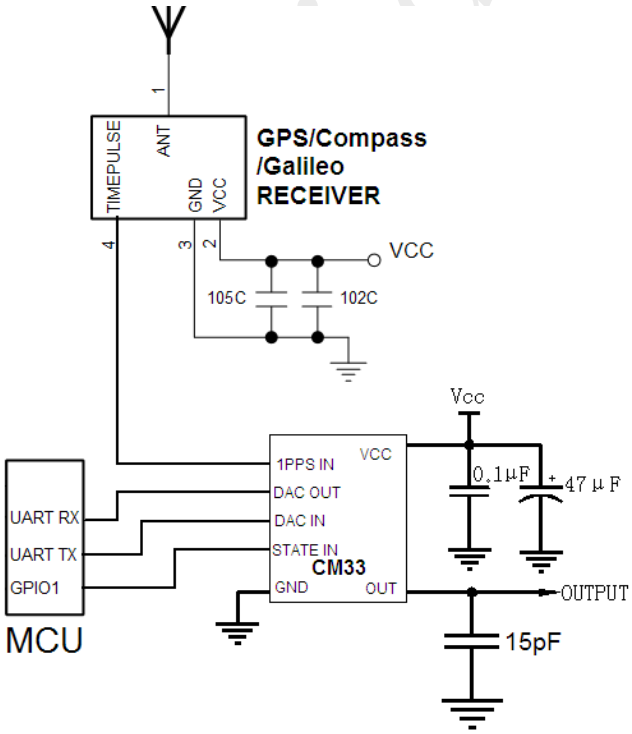
PIN DEFINITION			
PIN	**NAME**		**DESCRIPTION**
1	State Input	H: Lock	The clock module lock to PP1S reference when the state pin set high
		L: DAC	The clock module debug the output frequency by DAC when the state pin set low
2	VCC		Power supply: 4.75V to 5.25V
3	GND		GND
4	PP1S Input		PP1S reference input
5	DAC IN		The external DAC signal input
6	DAC OUT		Output the DAC signal when read DAC
7	NC		NC
8	25.6MHz OUTPUT		25.6MHz OCXO frequency output, synchronization with PP1S reference.

6. Typical Application



Satellite receiver offer 1PPS signal to the clock module CM33B.
The MCU offer DAC signal to the clock module CM33B.
The MCU monitor the work state of CM33B.
The CM33B power of 5V.

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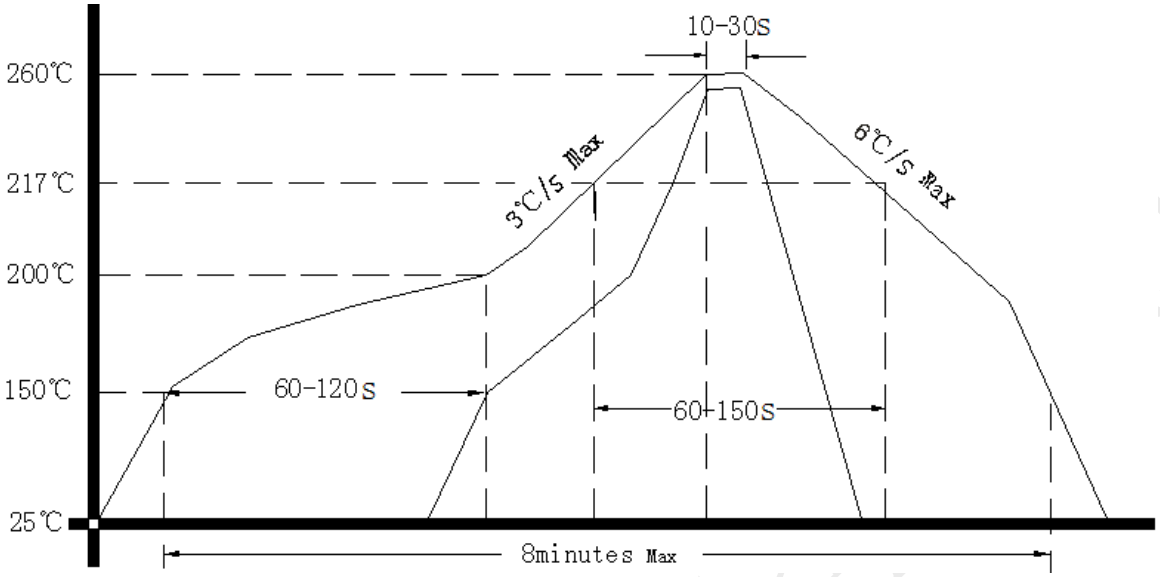
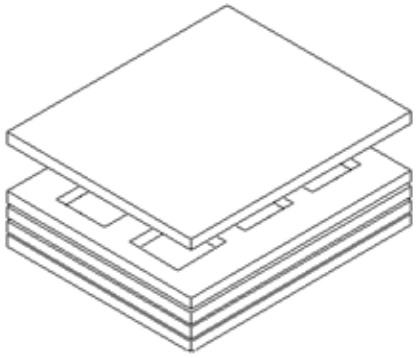
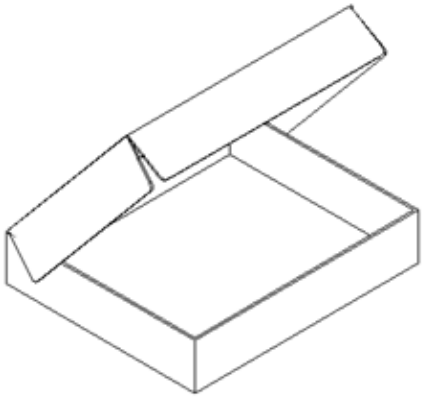
7. Reflow Soldering Curve (RoHS)



8. Package（mm）



Buffer material



Cardboard
Max 6pcs. circulator