

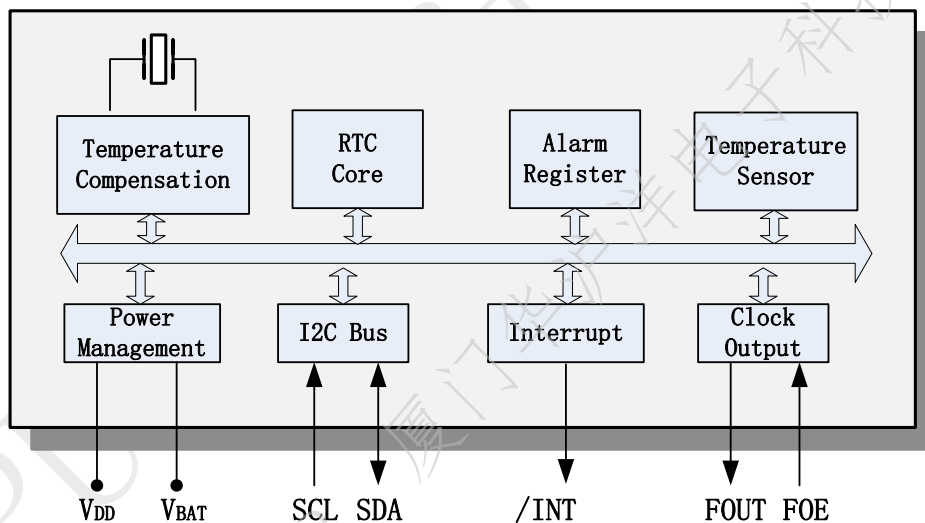


INS5830A —Low Power Consumption I²C RTC

Key Features

- Low current consumption: 0.5uA (Typ.)
- High stability:
< 5±23ppm @ +25°C
- Build-in TCXO: 32.768KHz
- Build-in temperature sensor
- Communication Interface: I²C bus
- Power Supply Voltage: 1.6V~5.0V
- Operation Temperature Range: -40°C ~ +85°C
- Leap years autocorrection
- Backup battery switchover function
- Timer output function with adjustable period
- Package: 3.2mm × 2.5mm × 1.0mm

Block Diagram



Overview

INS5830A is an I²C bus interface real-time clock with low power consumption. It embeds a 32.768KHz TCXO. The high precise temperature sensor and temperature compensated circuit ensure the high clock accuracy. It supports calendar (year, month, day, hour, minute, second), clock and timer functions etc. The SMD3225 package with only 1.0mm thickness makes it very suitable to be used in portable and small size electronic devices.



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1 Overview

INS5830A is an I²C bus interface real-time clock with low power consumption. It embeds a 32.768KHz TCXO. The high precise temperature sensor and temperature compensated circuit ensure the high clock accuracy. It supports calendar (year, month, day, hour, minute, second), clock and timer functions etc. The SMD3225 package with only 1.0mm thickness makes it very suitable to be used in portable and small size electronic devices.

2 Block Diagram

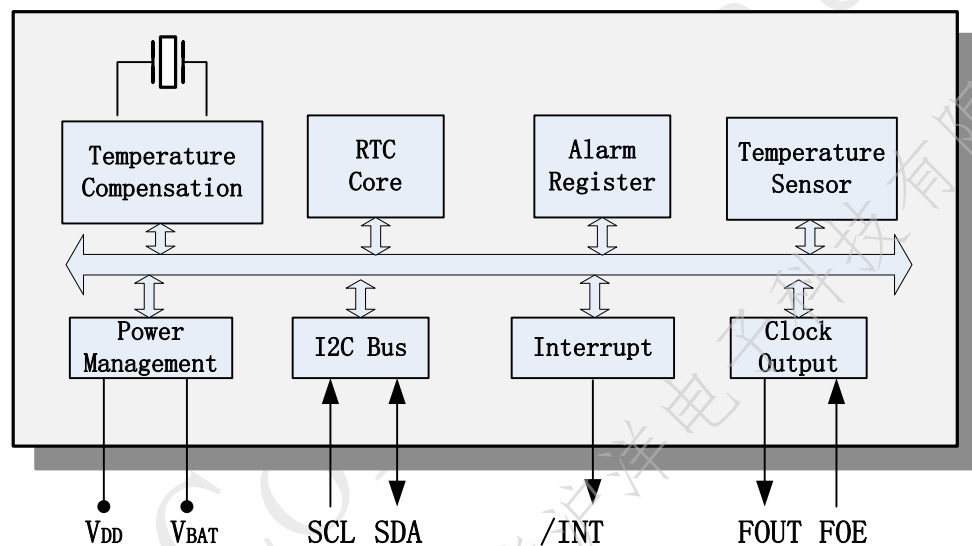


Figure 1. Block Diagram

3 Features

- Low current consumption: 0.5uA (Typ.)
- High stability:
< 5±23ppm @ +25°C
- Communication Interface: I2C bus
- Build-in TCXO: 32.768KHz
- Build-in temperature sensor
- Power Supply Voltage: 1.6V ~ 5.0V



- Operation Temperature Range: -40°C ~ +85°C
- Leap years autocorrection
- Backup battery switchover function
- Timer output function with adjustable period
- Package: 3.2mm × 2.5mm × 1.0mm

4 Pin definition

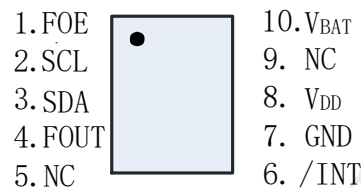


Table1. Pin Definition

| Pin Number | Pin Name | I/O | Description |
|------------|------------------|--------|--|
| 1 | FOE | In | FOUT output control pin. "1" - enable FOUT, "0"- FOUT Hi-Z |
| 2 | SCL | In | I ² C clock signal |
| 3 | SDA | In/Out | I ² C data signal |
| 4 | FOUT | Out | Frequency output. Controlled by FOE. Frequency can be set by FSEL bits. |
| 5 | NC | - | Floating |
| 6 | /INT | - | Interrupts Output, Open-Drain. |
| 7 | GND | - | Ground |
| 8 | V _{DD} | - | Power supply |
| 9 | NC | - | Floating |
| 10 | V _{BAT} | - | Backup battery pin. Connect to large-capacity capacitors or a backup battery. Connect to V _{DD} when switchover function is not necessary |



5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table2. Absolute Maximum Ratings

| Parameter | Symbol | Value | | | Unit | Notes |
|------------------------|-------------------|---------|------|----------------------|------|---------------------|
| | | Min. | Typ. | Max. | | |
| Power Supply Voltage | V _{DD} | -0.3 | | 5.5 | V | |
| Backup Battery Voltage | V _{BAT} | -0.3 | | 5.5 | V | |
| Input Voltage | V _{IN} | GND-0.3 | | 5.5 | V | FOE, SCL, SDA input |
| Clock Output Voltage | V _{OUT1} | GND-0.3 | | V _{DD} +0.3 | V | FOUT output |
| Output Voltage | V _{OUT2} | GND-0.3 | | 5.5 | V | SDA, /INT output |
| Storage temperature | T _{STG} | -55 | | 125 | °C | |

5.2 Recommended Operating Conditions

Table3. Recommended Operating Conditions

| Parameter | Symbol | Value | | | Unit | Notes |
|--|------------------|-------|------|------|------|----------------------|
| | | Min. | Typ. | Max. | | |
| Power Supply Voltage (normal mode) | V _{DD} | 2.5 | 3.0 | 5.0 | V | |
| Power Supply Voltage In case of single supply (V _{DD} = V _{BAT}) (Note 1) | V _{DD} | 1.6 | 3.0 | 5.0 | V | |
| Backup Battery | V _{BAT} | 1.6 | 3.0 | 5.0 | V | |
| Current consumption | I _{DD} | | 0.5 | | uA | Using Battery supply |
| Operation temperature | T _{OPR} | -40 | 25 | 85 | °C | |

Note 1: To apply Min. value of V_{DD} and V_{BAT}, V_{DD} and V_{BAT} need to be supplied with more than 2.5V at least for the oscillation to stabilize (oscillation start time t_{STA}).

5.3 Frequency Characteristics

Table4. Frequency Characteristics

| Parameter | Symbol | Value | | | Unit | Notes |
|------------------------|------------------|-------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Frequency stability | $\Delta f_1/f$ | 5±23 | | | ppm | V _{DD} =3.0V; @+25°C |
| Frequency stability | $\Delta f_2/f$ | -120 | | +10 | ppm | V _{DD} =3.0V; -20°C ~ +70°C; Reference frequency @ +25°C |
| Oscillation start time | t _{STA} | | | 1 | s | @+25°C |
| Year Aging | f _a | | | ±3 | ppm | |



| Parameter | Symbol | Value | | | Unit | Notes |
|-----------------------------|------------------|-------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Temperature Sensor Accuracy | Temp | | | ±5 | °C | V _{DD} =3.0V |
| FOUT duty cycle | t _{w/t} | 40 | | 60 | % | |

5.4 DC Characteristics

Table5. DC Characteristics

| Parameter | Symbol | Value | | | Unit | Notes | |
|------------------------------|------------------|---------------------|------|---------------------|------|---|--|
| | | Min. | Typ. | Max. | | | |
| Average Current consumption1 | I _{DD1} | 0.91 | | 5.1 | uA | V _{DD} =5.0V | f _{SCL} =0Hz, FOE=GND, /INT = V _{DD} ; V _{DD} =V _{BAT} ; FOUT off (High-Z); |
| Average Current consumption2 | I _{DD2} | 0.88 | | 4.9 | | V _{DD} =3.0V | Compensation interval 2s; V _{DD} voltage detection time 2ms |
| Average Current consumption3 | I _{DD3} | | | 20 | uA | V _{DD} =5.0V | f _{SCL} =0Hz, FOE=V _{DD} , /INT = V _{DD} ; V _{DD} =V _{BAT} ; FOUT:32.768kHz, |
| Average Current consumption4 | I _{DD4} | | | 19 | | V _{DD} =3.0V | CL=0pF; Compensation interval 2s; V _{DD} voltage detection time 2ms |
| High-level input voltage | V _{IH} | 0.8*V _{DD} | | 5.0 | V | SCL, SDA, FOE pin | |
| Low-level input voltage | V _{IL} | GND-0.3 | | 0.2*V _{DD} | V | | |
| High-level output voltage | V _{OH1} | 4.0 | | 5.0 | V | V _{DD} =5.0V, I _{OH} = -1mA | FOUT pin |
| | V _{OH2} | 2.2 | | 3.0 | | V _{DD} =3.0V, I _{OH} = -1mA | |
| | V _{OH3} | 2.9 | | 3.0 | | V _{DD} =3.0V, I _{OH} = -100uA | |
| Low-level output voltage | V _{OL1} | GND | | GND+0.5 | V | V _{DD} =5.0V, I _{OL} = 1mA | FOUT pin |
| | V _{OL2} | GND | | GND+0.8 | | V _{DD} =3.0V, I _{OL} = 1mA | |
| | V _{OL3} | GND | | GND+0.1 | | V _{DD} =3.0V, I _{OL} = 100uA | |
| | V _{OL4} | GND | | GND+0.25 | V | V _{DD} =5.0V, I _{OL} = 1mA | /INT pin |
| | V _{OL5} | GND | | GND+0.4 | | V _{DD} =3.0V, I _{OL} = 1mA | |
| | V _{OL6} | GND | | GND+0.4 | | V _{DD} ≥3.0V, I _{OL} = 3mA | |
| Input leakage current | I _{LK} | -0.5 | | 0.5 | uA | FOE, SDA, SCL pin, V _{IN} = V _{DD} or GND | |
| Output leakage current | I _{OZ} | -0.5 | | 0.5 | uA | FOUT, SDA, /INT pin, V _{IN} = V _{DD} or GND | |



5.5 AC Characteristics

Table6. AC Characteristics

V_{DD}=2.5V ~ 4.5V; Ta=-40°C ~ +85°C

| Parameter | Symbol | Value | | | Unit |
|--|---------------------|-------|------|------|------|
| | | Min. | Typ. | Max. | |
| SCL clock frequency | f _{SCL} | | | 400 | kHz |
| SCL low level time | t _{LOW} | 1.3 | | | us |
| SCL high level time | t _{HIGH} | 0.6 | | | us |
| Start condition setup time | t _{HD;STA} | 0.6 | | | us |
| Start condition hold time | t _{SU;STA} | 0.6 | | | us |
| Stop condition setup time | t _{SU;STO} | 0.6 | | | us |
| Bus idle time between start condition and stop condition | t _{RCV} | 1.3 | | | us |
| Data setup time | t _{SU;DAT} | 100 | | | ns |
| Data hold time | t _{HD;DAT} | 0 | | | ns |
| SCL, SDA rising time | t _r | | | 0.4 | us |
| SCL, SDA falling time | t _f | | | 0.4 | us |

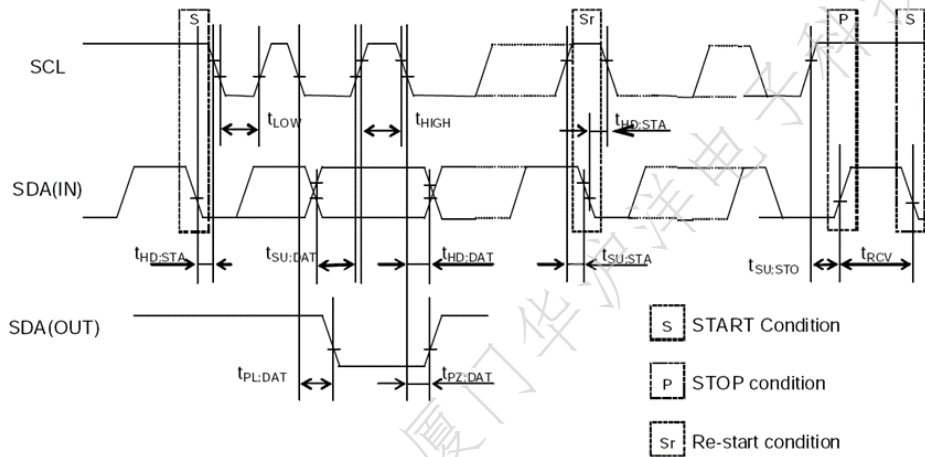


Figure 2. I²C bus Timing Chart



6 Registers

6.1 Register Lists

Address 0x00~0x0F: Basic Time and Calendar Registers

Address 0x10~0x1F: Extended Register Group 1

Address 0x20~30: Extended Register Group 2

Note: 0x10~16 and 0x00~06 with the same function, 0x1B~1F and 0x0B~0F with the same function

Table7. Basic Time and Calendar Registers

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | R/W |
|---------|--------------------|--------------------------------|----------------------------------|--------------------------------|---------------------------------|----------------------------------|----------|----------|----------|-----|
| 0x00 | SEC | ○ | BCD code, Second tens place, 0-5 | | | BCD code, Second ones place, 0-9 | | | | R/W |
| 0x01 | MIN | ○ | BCD code, Minute tens place, 0-5 | | | BCD code, Minute ones place, 0-9 | | | | R/W |
| 0x02 | HOUR | ○ | ○ | BCD code, Hour tens place, 0-2 | | BCD code, Hour ones place, 0-9 | | | | R/W |
| 0x03 | WEEK | ○ | 6 | 5 | 4 | 3 | 2 | 1 | 0 | R/W |
| 0x04 | DAY | ○ | ○ | BCD code, Day tens place, 0-3 | | BCD code, Day ones place, 0-9 | | | | R/W |
| 0x05 | MONTH | ○ | ○ | ○ | BCD code, Month tens place, 0-1 | BCD code, Month ones place, 0-9 | | | | R/W |
| 0x06 | YEAR | BCD code, Year tens place, 0-9 | | | | BCD code, Year ones place, 0-9 | | | | R/W |
| 0x07 | RAM | ● | ● | ● | ● | ● | ● | ● | ● | R/W |
| 0x08 | MIN Alarm | AE | BCD code, Minute tens place, 0-5 | | | BCD code, Minute ones place, 0-9 | | | | R/W |
| 0x09 | HOUR Alarm | AE | ● | BCD code, Hour tens place, 0-2 | | BCD code, Hour ones place, 0-9 | | | | R/W |
| 0x0A | WEEK Alarm | AE | 6 | 5 | 4 | 3 | 2 | 1 | 0 | R/W |
| | DAY Alarm | | ● | BCD code, Day tens place, 0-3 | | BCD code, Day ones place, 0-9 | | | | R/W |
| 0x0B | Timer Counter 0 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | R/W |
| 0x0C | Timer Counter 1 | ● | ● | ● | ● | 2048 | 1024 | 512 | 256 | R/W |
| 0x0D | Extension Register | TEST | WADA | USEL | TE | FSEL [1] | FSEL [0] | TSEL [1] | TSEL [0] | R/W |
| 0x0E | Flag Register | ○ | ○ | UF | TF | AF | ○ | VLF | VDET | R/W |
| 0x0F | Control Register | CSEL [1] | CSEL [0] | UIE | TIE | AIE | ○ | ○ | RESET | R/W |

Table8. Extended Register Group 1

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | R/W |
|---------|----------|------|----------------------------------|------|------|----------------------------------|------|------|------|-----|
| 0x10 | SEC | ○ | BCD code, Second tens place, 0-5 | | | BCD code, Second ones place, 0-9 | | | | R/W |



| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | R/W |
|---------|--------------------|--------------------------------|----------------------------------|--------------------------------|---------------------------------|----------------------------------|----------|-----------|-----------|-----|
| 0x11 | MIN | ○ | BCD code, Minute tens place, 0-5 | | | BCD code, Minute ones place, 0-9 | | | | R/W |
| 0x12 | HOUR | ○ | ○ | BCD code, Hour tens place, 0-2 | | BCD code, Hour ones place, 0-9 | | | | R/W |
| 0x13 | WEEK | ○ | 6 | 5 | 4 | 3 | 2 | 1 | 0 | R/W |
| 0x14 | DAY | ○ | ○ | BCD code, Day tens place, 0-3 | | BCD code, Day ones place, 0-9 | | | | R/W |
| 0x15 | MONTH | ○ | ○ | ○ | BCD code, Month tens place, 0-1 | BCD code, Month ones place, 0-9 | | | | R/W |
| 0x16 | YEAR | BCD code, Year tens place, 0-9 | | | | BCD code, Year ones place, 0-9 | | | | R/W |
| 0x17 | TEMP | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | R |
| 0x18 | Backup Function | ○ | ○ | ○ | ○ | VDET OFF | SWOFF | BKSMP [1] | BKSMP [0] | R/W |
| 0x19 | Not use | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | R |
| 0x1A | Not use | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | R |
| 0x1B | Timer Counter 0 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | R/W |
| 0x1C | Timer Counter 1 | ● | ● | ● | ● | 2048 | 1024 | 512 | 256 | R/W |
| 0x1D | Extension Register | TEST | WADA | USEL | TE | FSEL [1] | FSEL [0] | TSEL [1] | TSEL [0] | R/W |
| 0x1E | Flag Register | ○ | ○ | UF | TF | AF | ○ | VLF | VDET | R/W |
| 0x1F | Control Register | CSEL [1] | CSEL [0] | UIE | TIE | AIE | ○ | ○ | RESET | R/W |

Table9. Extended Register Group2

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | R/W |
|---------|--------------------|-----------------------------|------|------|------|-------------|------|------|--------|-----|
| 0x20 | Device ID | Vendor ID[3:0] | | | | Ver[3:0] | | | | R |
| 0x21 | Control Register 1 | Reserved: Ensure to be 0x8 | | | | ○ | ○ | ○ | VBATSW | R/W |
| 0x22-26 | RSV | Reserved: Ensure to be 0x00 | | | | | | | | R |
| 0x27 | SubSEC | Reserved | | | | SubSEC[3:0] | | | | R |
| 0x28-30 | RSV | Reserved: Ensure to be 0x00 | | | | | | | | R/W |

Note:

1, After power-up reset or in case VLF bit returns "1", make sure to initialize all registers to default state before using the RTC. Ensure all inputs are in the required range and the defined values are set for the reserved bits in case the clock cannot work normally.

- ✓ During the initial power-up, below bits will be in the state as below:

Initial 0: TEST, WADA, USEL, TE, FSEL[1:0], TSEL[0], UF, TF, AF, CSEL[1], UIE, TIE, RESET, VDETOFF, SWOFF, BKSMP[1:0], VBATSW.

Initial 1: VLF, VDET, CSEL[0].

- ✓ All other register values are undefined, so make sure to reset the module before using it.



- ✓ The bits marked with “○” can be read out “0” only after initializing.
- ✓ The bits marked with “●” are RAM bits which can be used to write or read any data.
- ✓ Only 0 can be written to UF, TF, AF, VLF, VDET bits.
- ✓ Make sure “0” to be written for TEST bits which are used for testing only.
- ✓ Reserved bits must be set to the defined values accordingly.

6.2 Details of Registers

6.2.1 Clock counter registers

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|----------------------------------|--------------------------------|------|----------------------------------|------|------|------|---------|
| 0x00/10 | SEC | ○ | BCD code, Second tens place, 0-5 | | | BCD code, Second ones place, 0-9 | | | | 0x25 |
| 0x01/11 | MIN | ○ | BCD code, Minute tens place, 0-5 | | | BCD code, Minute ones place, 0-9 | | | | 0x36 |
| 0x02/12 | HOUR | ○ | ○ | BCD code, Hour tens place, 0-2 | | BCD code, Hour ones place, 0-9 | | | | 0x01 |

SEC: BCD format, Value: 0~59

MIN: BCD format, Value: 0~59

HOUR: BCD format, Value: 0~23

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|------|------|------|------|------|------|---------|
| 0x03/13 | WEEK | ○ | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x40 |

WEEK: Value 01h, 02h, 04h, 08h, 10h, 20h, 40h. Only one bit can be set to 1 each time, all others must be set to 0.

Table10. WEEK Register

| WEEK | Data | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|-----------|------|------|------|------|------|------|------|------|------|
| Sunday | 01h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Monday | 02h | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Tuesday | 04h | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Wednesday | 08h | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| Thursday | 10h | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Friday | 20h | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| Saturday | 40h | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|-------------------------------|------|-------------------------------|------|------|------|---------|
| 0x04/14 | DAY | ○ | ○ | BCD code, Day tens place, 0-3 | | BCD code, Day ones place, 0-9 | | | | 0x01 |

DAY: BCD format, the value range will be adjusted automatically according to the month setting and if a leap year or not .

**Table11. DAY Register Value**

| Month | Day Value Range |
|-------------------------|-----------------|
| 1, 3, 5, 7, 8, 10, 12 | 1~31 |
| 4, 6, 9, 11 | 1~30 |
| February in normal year | 1~28 |
| February in leap year | 1~29 |

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|--------------------------------|------|------|------------------------------------|---------------------------------|------|------|------|---------|
| 0x05/15 | MONTH | ○ | ○ | ○ | BCD code, Month tens place, 0-1 | BCD code, Month ones place, 0-9 | | | | 0x01 |
| 0x06/16 | YEAR | BCD code, Year tens place, 0-9 | | | | BCD code, Year ones place, 0-9 | | | | 0x00 |

MONTH: BCD format, Value1~12

YEAR: BCD format, Value0~99(2000~2099)

Example: 2020/01/01 Wednesday 21:18:36

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------|----------|------|------|------|------|------|------|------|------|
| 0x00/10 | SEC | ○ | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0x01/11 | MIN | ○ | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0x02/12 | HOUR | ○ | ○ | 1 | 0 | 0 | 0 | 0 | 1 |
| 0x03/13 | WEEK | ○ | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0x04/14 | DAY | ○ | ○ | 0 | 0 | 0 | 0 | 0 | 1 |
| 0x05/15 | MONTH | ○ | ○ | ○ | 0 | 0 | 0 | 0 | 1 |
| 0x06/16 | YEAR | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

6.2.2 Alarm registers

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|------------|------|----------------------------------|-----------------------------------|------|----------------------------------|------|------|------|---------|
| 0x08 | MIN Alarm | AE | BCD code, Minute tens place, 0-5 | | | BCD code, Minute ones place, 0-9 | | | | 0x00 |
| 0x09 | HOUR Alarm | AE | ● | BCD code, Hour tens place, 0-2 | | BCD code, Minute ones place, 0-9 | | | | 0x00 |
| 0x0A | WEEK Alarm | AE | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x00 |
| | DAY Alarm | | ● | BCD code, Day tens place, 0-3 | | BCD code, Day ones place, 0-9 | | | | |

According to AIE, AF, WADA bits setting, the alarm interrupt will be generated once the current time match the settings in the above registers, the /INT pin goes to low level and AF bit is set to '1' to record an alarm interrupt event has occurred.

WEEK Alarm/DAY Alarm: Controlled by WADA bit in 0x0D register

AE: Alarm Enable bit, 0-enable; 1-disenable

AF: Defined in 0x0E register bit3

AIE: Defined in 0x0F register bit3



6.2.3 Timer control registers

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|--------------------|------|------|------|------|------|------|------|------|---------|
| 0x0B/1B | Timer Counter 0 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 0x00 |
| 0x0C/1C | Timer Counter 1 | ● | ● | ● | ● | 2048 | 1024 | 512 | 256 | 0x00 |

According to TE, TF, TIE, TSEL[1:0] bits setting, a timer interrupt will be generated once the value counts down to 0 from the one set in the above registers.

TE: Defined in 0x0D register bit4

TF: Defined in 0x0E register bit4

TIE: Defined in 0x0F register bit4

TSEL[1:0]: Defined in 0x0D register bit1 and bit0

6.2.4 Extension registers

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|-----------------------|------|------|------|------|---------|---------|---------|---------|---------|
| 0x0D/1D | Extension Register | TEST | WADA | USEL | TE | FSEL[1] | FSEL[0] | TSEL[1] | TSEL[0] | 0x02 |

TEST: Test bit, must be set to "0"

WADA: Week Alarm/Day Alarm control bit, decide 0x0A register as DAY Alarm or WEEK Alarm. 0-WEEK alarm, 1-DAY alarm

USEL: Update Interrupt Select bit, 0-output interrupt once a second, 1-output interrupt once a minute

TE: Timer Enable bit, 0-disable, 1-enable

FSEL[1], FSEL[0]: FOUT frequency setting:

| FSEL[1] | FSEL[0] | FOUT Frequency |
|---------|---------|---------------------|
| 0 | 0 | 32.768KHz (Default) |
| 0 | 1 | 1024Hz |
| 1 | 0 | 1Hz |
| 1 | 1 | 32.768KHz |

TSEL[1], TSEL[0]: Timer countdown period(source clock) setting:

| TSEL[1] | TSEL[0] | Source clock |
|---------|---------|--------------|
| 0 | 0 | 4096Hz |
| 0 | 1 | 64Hz |
| 1 | 0 | 1Hz |
| 1 | 1 | 1/60Hz |

6.2.5 Flag registers

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|---------------|------|------|------|------|------|------|------|------|---------|
| 0x0E/1E | Flag Register | ○ | ○ | UF | TF | AF | ○ | VLF | VDET | 0x23 |



UF: Update flag bit. When time update interrupt event occurs, it will be set to “1” and keeps “1” until a “0” is written to it.

TF: Timer Flag bit. When a fixed-cycle timer interrupt event occurs, it will be set to “1” and keeps “1” until a “0” is written to it.

AF: Alarm Flag bit. When an alarm interrupt event occurs, it will be set to “1” and keeps “1” until a “0” is written to it.

VLF: Voltage Low Flag bit. When supply voltage is lower than 1.6V, it will be set to “1” and keeps “1” until a “0” is written to it.

VDET: Voltage Detection Flag bit. When supply voltage is lower than 1.95V, it will be set to “1” and keeps “1” until a “0” is written to it.

6.2.6 Control registers

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|------------------|----------|----------|------|------|------|------|------|-------|---------|
| 0x0F/1F | Control Register | CSEL [1] | CSEL [0] | UIE | TIE | AIE | ○ | ○ | RESET | 0x40 |

CSEL[1], CSEL[0]: Compensation interval Select 1, 0 bits, used to set temperature compensation interval.

| CSEL[1] | CSEL[0] | Compensation interval |
|---------|---------|-----------------------|
| 0 | 0 | 0.5s |
| 0 | 1 | 2s(default) |
| 1 | 0 | 10s |
| 1 | 1 | 30s |

UIE: Update Interrupt Enable bit. When UF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).

TIE: Timer Interrupt Enable bit: When TF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).

AIE: Alarm Interrupt Enable bit: When AF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).

RESET: Reset IC, prepared for the synchronized starting of time or timer.

6.2.7 Temperature register

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|------|------|------|------|------|------|---------|
| 0x17 | TEMP | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 0xa9 |

Read digital temperature data, Temp [°C] = (TEMP[7:0] * 2 - 187.19) / 3.218.

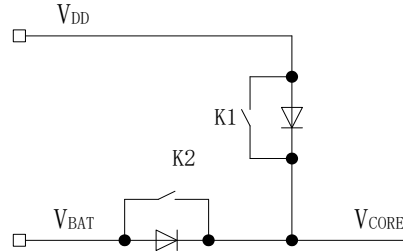
6.2.8 Battery Backup switchover register

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|-----------------|------|------|------|------|----------|-------|-----------|-----------|---------|
| 0x18 | Backup Function | ○ | ○ | ○ | ○ | VDET OFF | SWOFF | BKSMP [1] | BKSMP [0] | 0x00 |



This register controls the power switchover function. Once abnormal VDD is detected, it will be switched to use battery as the power supply.

The power circuit diagram is shown below:



VDETOFF (Voltage Detector OFF): Main power supply VDD voltage detection control bit. 0-enable detection function (Default), VDD voltage will be detected once a second; 1-disenable detection function.

SWOFF (Switch OFF): Switch K1 control bit. 0- close (Default); 1- open

BKSMP[1], BKSMP[0](Backup mode Sampling time): Control the voltage detection sampling time. Default: 00.

Table12. VDD Voltage Sampling Time

| VDD Detect Function | VDETOFF | SWOFF | BKSMP [1] | BKSMP [0] | VDD Voltage Sampling Time | Switch K1 ON/OFF | Notes |
|---------------------|---------|-------|-----------|-----------|---------------------------|------------------|----------|
| ON | 0 | X | 0 | 0 | 2ms | 2ms OFF | Default |
| | | | 0 | 1 | 16ms | 16ms OFF | |
| | | | 1 | 0 | 128ms | 128ms OFF | |
| | | | 1 | 1 | 256ms | 256ms OFF | |
| OFF | 1 | 0 | x | x | OFF | ON | K1 Close |
| | | 1 | x | x | OFF | OFF | K1 Open |

6.2.9 Device ID register

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|-----------|---------------|------|------|------|----------|------|------|------|---------|
| 0x20 | Device ID | VendorID[3:0] | | | | Ver[3:0] | | | | 0xd2 |

VendorID[3:0]: The fixed value is defined as VendorID[3:0]=1101b=Dh to represent DAPU.

Ver[3:0]: version of the IC

6.2.10 Control Register 1

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|--------------------|-----------------------|------|------|------|------|------|------|--------|---------|
| 0x21 | Control Register 1 | Reserved: must be 0x8 | | | | ○ | ○ | ○ | VBATSW | 0x80 |

VBATSW: Battery supply switch K2 control bit. Default 0, 0- Open, 1-Close.



6.2.11 Sub-second timer register

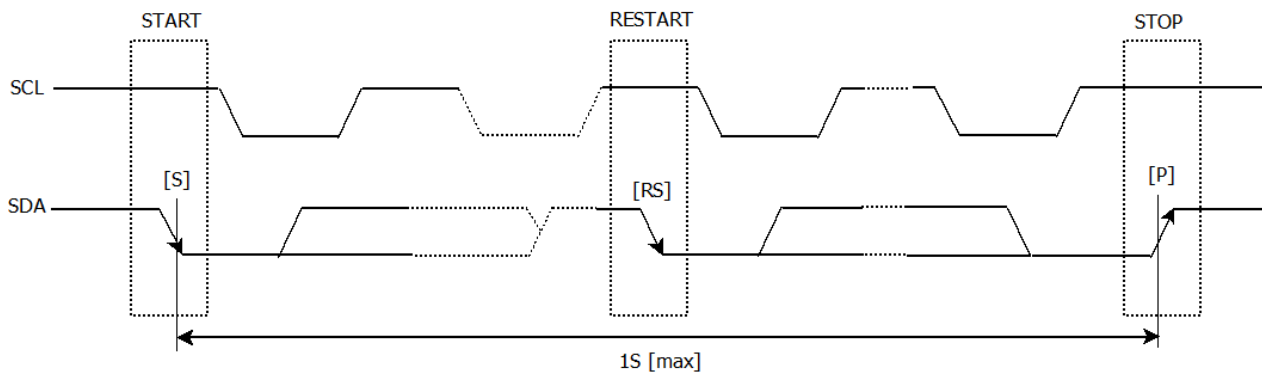
| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|----------|------|------|------|-------------|------|------|------|---------|
| 0x27 | SubSEC | Reserved | | | | SubSEC[3:0] | | | | 0x00 |

SubSEC[3:0]: sub second bit, and unit is 1/16s.

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7 I²C Bus Interface



I²C bus supports bi-directional communications through a serial clock line SCL and a serial data line SDA. I²C bus device can be defined as “Master” and “Slave”. INS5830A can only be used as Slave.

7.1 Cautions

I²C bus includes START, RESTART, STOP conditions, the duration between START and STOP must be less than 1 second just in case the bus to be set to standby mode automatically. A new START condition must be transferred before restarting of any communications.

INS5830A I²C bus interface supports single byte read/write operations as well as multiple bytes incremental access. After 0x7F address, the next one will be 0x00.

7.2 Slave Address

Table13. I²C Bus Slave Address

| Transfer data | Slave address | | | | | | | R/W |
|---------------|---------------|------|------|------|------|------|------|-----------|
| | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| 65h (Read) | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 (Read) |
| 64h (Write) | | | | | | | | 0 (Write) |

INS5830A I²C bus Slave Address is [0110 010*].

7.3 I²C bus protocol

It is assumed CPU is master and INS5830A is slave in this section.

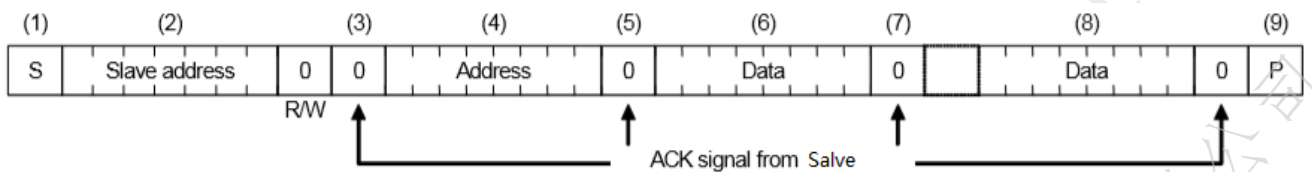
7.3.1 Write process

I²C bus includes an address auto-increment function, once the initial address has been specified, the



INS5830A increments (+1) the address automatically after each data is sent, then to write next data.

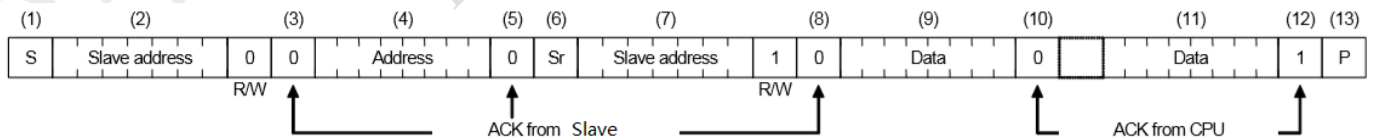
- (1) CPU sends start condition[S]
- (2) CPU sends INS5830A's slave address with R/W bit to set to write mode
- (3) CPU verifies ACK signal from INS5830A
- (4) CPU sends write address to INS5830A
- (5) CPU verifies ACK signal from INS5830A
- (6) CPU sends write data to the address specified at step (4)
- (7) CPU verifies ACK signal from INS5830A
- (8) Repeat (6) (7) if multiple bytes need to be written, address will be incremented automatically
- (9) CPU ends stop condition[P]



7.3.2 Read process

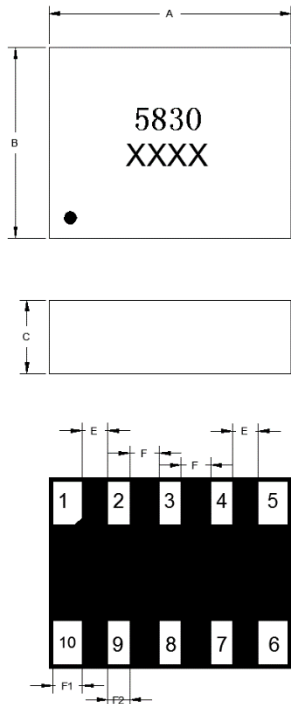
Writing the address to be read with write mode firstly, then reading the data with read mode.

- (1) CPU sends start condition[S]
- (2) CPU sends INS5830A's slave address with R/W bit to set to write mode
- (3) CPU verifies ACK signal from INS5830A
- (4) CPU sends address for reading from INS5830A
- (5) CPU verifies ACK signal from INS5830A
- (6) CPU sends RESTART condition [Sr]
- (7) CPU sends INS5830A's slave address with R/W bit to set to read mode
- (8) CPU verifies ACK signal from INS5830A
- (9) CPU reads data from the specified address in step (4)
- (10) CPU verifies ACK signal from INS5830A
- (11) Repeat (9) (10) if multiple bytes need to be read, address will be incremented automatically
- (12) CPU sends ACK signal for "1"
- (13) CPU sends stop condition[P]





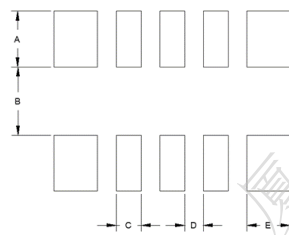
8 Dimensions



| Dimension | Min. | Typ. | Max. |
|-----------|------|------|------|
| A | 3.0 | 3.2 | 3.4 |
| B | 2.3 | 2.5 | 2.7 |
| C | -- | 1.0 | -- |
| E | -- | 0.30 | -- |
| F | -- | 0.4 | -- |
| G | -- | 0.6 | -- |
| H | -- | 1.3 | -- |
| F1 | -- | 0.45 | -- |
| F2 | -- | 0.30 | -- |

(Unit: mm)

Figure 3. Dimension



| Dimension | Max. |
|-----------|------|
| A | 0.9 |
| B | 1.1 |
| C | 0.4 |
| D | 0.3 |
| E | 0.7 |

(Unit: mm)

Figure 4. Recommended Soldering Pattern



9 Package

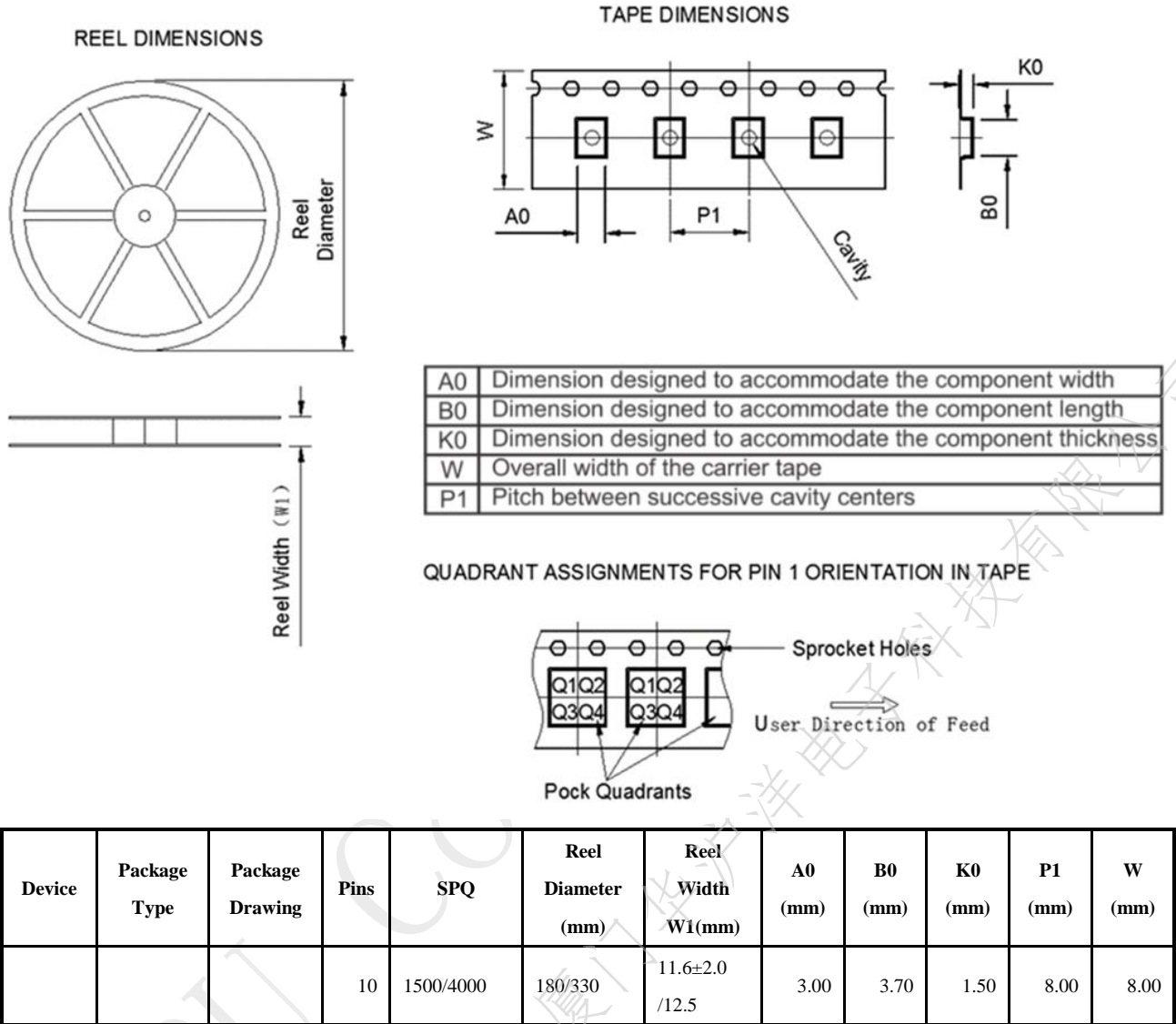


Figure 5. Package