DSO3001 —High Performance All-silicon Oscillator

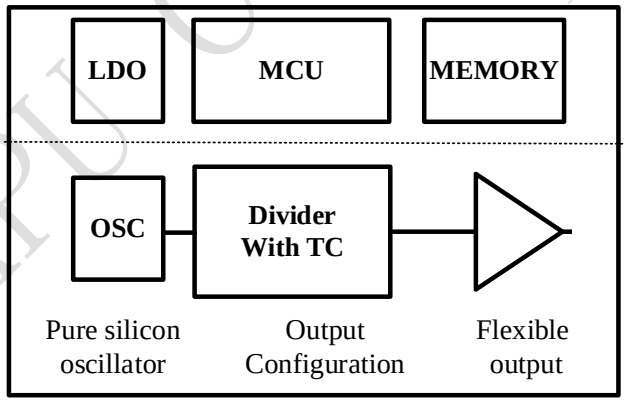
Key Features

- All-silicon without quartz and MEMS
- Total frequency stability ： ±50 ppm
- Single ended output： 10 kHz ~ 212.5MHz
- Differential output： 10 kHz ~ 350 MHz
- Operating temperature ： -40℃~85℃
- Power supply： 1.8V/2.5V/3.3V
- Output： LVDS, LVPECL, HCSL, CML, LVCMOS or dual LVCMOS
- Package： 3225 and 5032
- Low jitter: 350 fs Typ RMS (12 kHz – 20 MHz bandwidth)
- Built-in LDO and power filter circuit
- RoHS Compliant

Application

- Automotive electronics
- Intelligent terminal
- Ethernet
- Consumer electronics
- Communication equipment

Block Diagram



Overview

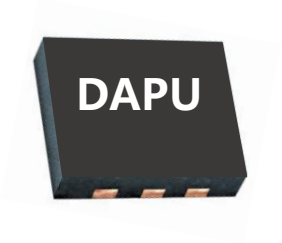
Dapu all silicon oscillator adopts unique frequency synthesis and sensor technology, which can output any clock from 10 kHz to 350 MHz without quartz and MEMS devices. The product can keep low jitter and frequency stability in the whole working range, and has high reliability in harsh environment and strong vibration.

Revision History

Version	Change Contents	Prepared by	Revised Date
V1.0.0	First Issued	*David*	2021.05.8

Index

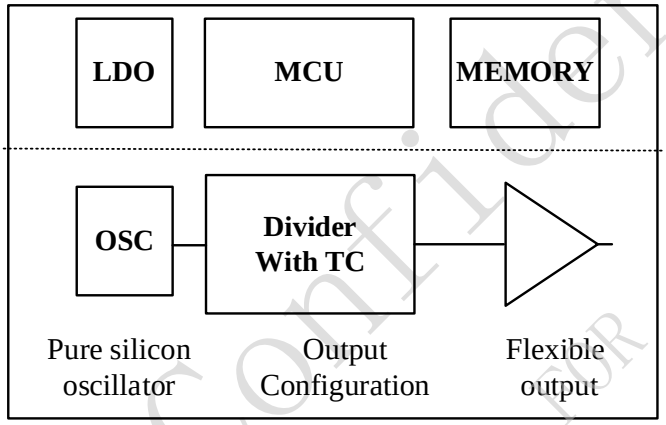
1 Overview



DSO3001 series all silicon oscillator is a clock free oscillator without quartz and MEMS devices. It is a high reliable clock oscillator which can still work normally under harsh environment and strong vibration. The chips can be manufactured to achieve multi-frequency and multi-format output from 10KHz to 350MHz, and maintain low jitter and frequency stability throughout the operation range.

Thanks to the built-in temperature and stress sensors, the DSO3001 all silicon oscillator can adapt to the harsh working environment. The built-in LDO and filter circuit greatly enhance the power supply noise suppression ability of the chip. Flexible clock frequency configuration and output format configuration provide maximum convenience for customer product design.

2 Block Diagram



3 Features

- All-silicon without quartz and MEMS
- Total frequency stability: ±50 ppm
- Single ended output: 10 kHz ~ 212.5MHz
- Differential output: 10 kHz ~ 350 MHz
- Operating temperature: -40℃~85℃
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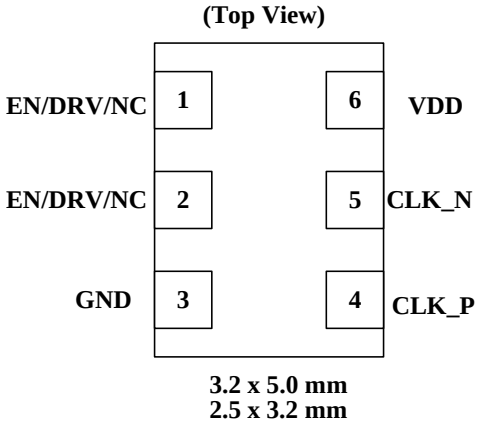
- Low jitter: 350 fs Typ RMS (12 kHz – 20 MHz bandwidth)
- Built-in LDO and power filter circuit
- RoHS Compliant

4 Pin Definition



PIN	Description
1	Optional function EN = Output Enable, active high DRV = Output Driver Enable, active high NC = Not Connect
2	Optional function (refer to PIN1)
3	GND
4	CLK_P
5	CLK_N
6	VDD

5 Electrical Specifications

Table 5.1 Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Unit
Operating Temperature	TA	-40 to 85	°C
Storage Temperature	T_S	-55 to 105	°C
Supply Voltage	V_{DD}	-0.5 to 3.8	V
Input Voltage	V_{IN}	-0.5 to V_{DD} + 0.3	V
ESD HBM (JESD22-A114)	HBM	4.0	kV
Solder Temperature[2]	T_{PEAK}	260	°C
Solder Time at T_{PEAK}[2]	T_P	20 - 40	sec

Notes:

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

2. The device is compliant with JEDEC J-STD-020.

Table 5.2 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition/Comment
Supply Voltage	V_{DD}	1.71	1.8	1.89	V	V_{DD} = 1.8 V
		2.375	2.5	2.625	V	V_{DD} = 2.5V
		3.135	3.3	3.47	V	V_{DD} = 3.3 V
Supply Current (F_{CLK} = 50 MHz)	I_{DD}		40	50	mA	Tristate Hi-Z (EN = 0, output disabled)
			1	2	mA	Ready State

						(DRV = 0, standby mode)
			70	80	mA	LVPECL (DC-Coupled)
			60	70	mA	LVPECL (AC-Coupled)
			45	55	mA	LVDS
			60	70	mA	HCSL
			60	70	mA	CML
			40	55	mA	CMOS
			50	60	mA	Dual CMOS
Operating Temperature	TA	-40		85	℃	

Table5.3 Input Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition/Comment
Output Enable (EN)[1]	V_{IH}	0.7×V_{DD}			V	
	V_{IL}			0.3×V_{DD}	V	
	T_D			3	µs	Output Disable Time, F_{CLK} >10 MHz
	T_E			20	µs	Output Enable Time, F_{CLK} >10 MHz
Output Enable (DRV)[1]	$V_{IH'}$	0.7×V_{DD}			V	
	$V_{IL'}$			0.3×V_{DD}	V	
	$T_{D'}$			3	µs	Output Disable Time. Within 40us, the current drops to less than 1.5mA F_{CLK} >10 MHz
	$T_{E'}$			400	µs	Output Enable Time, F_{CLK} >10 MHz

Notes:

1.EN/DRV includes a 50 kΩ pull-up to V_{DD} for EN active high. Includes a 50 kΩ pull-down to GND for EN/DRV active low. NC (No Connect) pins include a 50 kΩ pull-down to GND.

Table 5.4 Output Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition/Comment
Frequency Range	F_{CLK}	0.01		350	MHz	LVDS, LVPECL, CML, HCSL
		0.01		212.5	MHz	CMOS, Dual CMOS
Total Stability[1]	F_{STAB}	-50		50	ppm	Frequency stability
Rise/Fall Time (20% to 80% V_{PP})	T_R/T_F			350	ps	LVPECL/LVDS/CML
			0.5	1.5	ns	CMOS / Dual CMOS (C_L = 5 pF)
				550	ps	HCSL, F_{CLK} >50 MHz
Powerup Time	t_{OSC}			4	ms	Time from 0.9 × V_{DD} until output frequency (F_{CLK}) within spec
Duty Cycle	DC	45		55	%	
LVPECL Output Option[2] (DC-Coupled)	V_{OC}	V_{DD}–1.55		V_{DD}–1.25	V	Mid-level
	V_O	1.4		1.85	V_{PP}	Swing (diff [6])
LVPECL Output Option[2]	V_O	1.4		1.85	V_{PP}	Swing (diff [6])

(AC-Coupled)						
LVDS Output Option[3] (DC-Coupled)	V_{OC}	1.125	1.20	1.275	V	Mid-level (2.5 V, 3.3 V V_{DD})
		0.795	0.85	0.905	V	Mid-level (1.8 V V_{DD})
	V_O	0.5	0.82	0.96	V_{PP}	Swing (diff [6])
	V_{OL}	0	5	10	mV	Output voltage low
HCSL Output Option[4] (R_{term} = 50 Ω; DC-Coupled)	V_{OH}	695	815	935	mV	Output voltage high
HCSL Output Option[5] (R_{term} = 42.5 Ω; DC-Coupled)	V_{OH}	695	820	945	mV	Output voltage high
	V_{OL}	0	5	10	mV	Output voltage low
CML Output Option (AC-Coupled)	V_O	0.725	0.8	0.89	V_{PP}	Swing (diff [6])
CMOS Output Option	V_{OH}	0.83×V_{DD}			V	I_{OH} = 8/6/4 mA for 3.3/2.5/1.8V V_{DD}
	V_{OL}			0.17×V_{DD}	V	I_{OL} = 8/6/4 mA for 3.3/2.5/1.8V V_{DD}

Notes:

1.Total Stability, includes temperature stability, initial accuracy, load pulling, V_{DD} variation, and aging for 10 years at 40℃.

2. R_{term} = 50 Ω to V_{DD} – 2.0 V (Refer to Appendix figure3).

3. R_{term} = 100 Ω (differential) (Refer to Appendix figure4)

4. R_{term} = 50 Ω to GND (Refer to Appendix figure5).

5. R_{term} = 42.5 Ω to GND (Refer to Appendix figure5).

6. “diff” means differential signal

Table 5.5 Clock Output Phase Jitter and PSRR

Parameter	Symbol	Min	Typ	Max	Test Condition/Comment
Phase Jitter (RMS, 12 kHz - 20 MHz)[1,2] F_{CLK} ≥ 10 MHz	ϕ_J		350	750	Differential Formats
			350		CMOS, Dual CMOS
Phase Jitter (RMS, 50 kHz - 20 MHz) F_{CLK} ≥ 156.25 MHz	ϕ_J		150	250	Differential Formats
			100		CMOS, Dual CMOS
Spurs Induced by External Power Supply Noise, 50 mV_{pp} Ripple. LVDS 156.25 MHz Output V_{DD} = 1.8 V	PSRR		-76		100 kHz sine wave
			-75		200 kHz sine wave
			-75		500 kHz sine wave
			-75		1 MHz sine wave
Spurs Induced by External Power Supply Noise, 50 mV_{pp} Ripple. LVDS 156.25 MHz Output V_{DD} = 2.5 or 3.3 V	PSRR		-83		100 kHz sine wave
			-83		200 kHz sine wave
			-83		500 kHz sine wave
			-82		1 MHz sine wave

Notes:

1. Applies to output frequency: 50, 100, 156.25, 212.5, 350 MHz.

2. Guaranteed by characterization. Jitter inclusive of any spurs.

6 Environmental Conditions

Table 6.1. Environmental Conditions

Package	Symbol	Parameter	Test Condition	Value	Unit
	MSL	Moisture Sensitivity Level	1		
5032 6-pin DFN	Θ_{JA}	Thermal Resistance Junction to Ambient	Still Air	105	°C/W
	Θ_{JB}	Thermal Resistance Junction to Board	Still Air	81	°C/W
	T_J	Max Junction Temperature	Still Air	125	°C
3225 6-pin DFN	Θ_{JA}	Thermal Resistance Junction to Ambient	Still Air	108	°C/W
	Θ_{JB}	Thermal Resistance Junction to Board	Still Air	84	°C/W
	T_J	Max Junction Temperature	Still Air	125	°C

7 Dimension and Package

7.1 Dimension (5032)

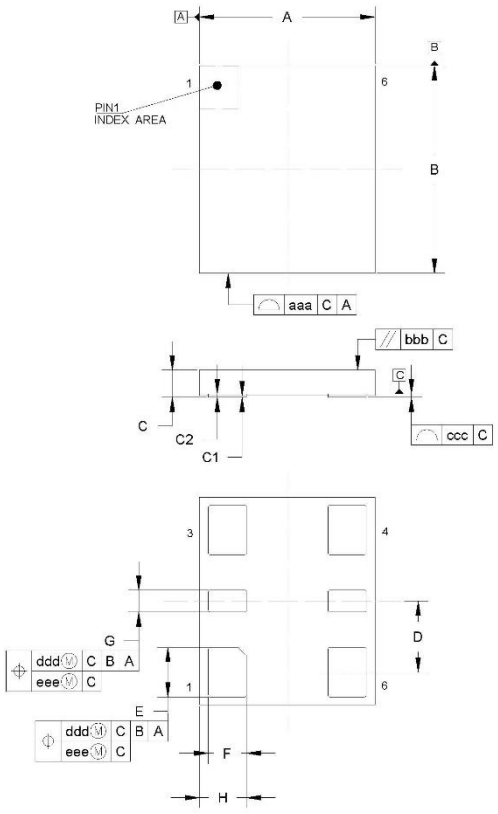


Figure 7.1. DSO3001 (5032) Outline Diagram

Table 7.1. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A		3.2 BSC	
B		4 BSC	
C	0.8	0.85	0.9
C1	0	0.035	0.05
C2		0.203 REF	
D		1.27 BSC	
E	0.59	0.64	0.69
F	0.7	0.75	0.8
G	0.59	0.64	0.69
H		0.85 REF	
aaa		0.1	
bbb		0.1	
ccc		0.08	
ddd		0.1	
eee		0.1	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

7.2 Dimension (3225)

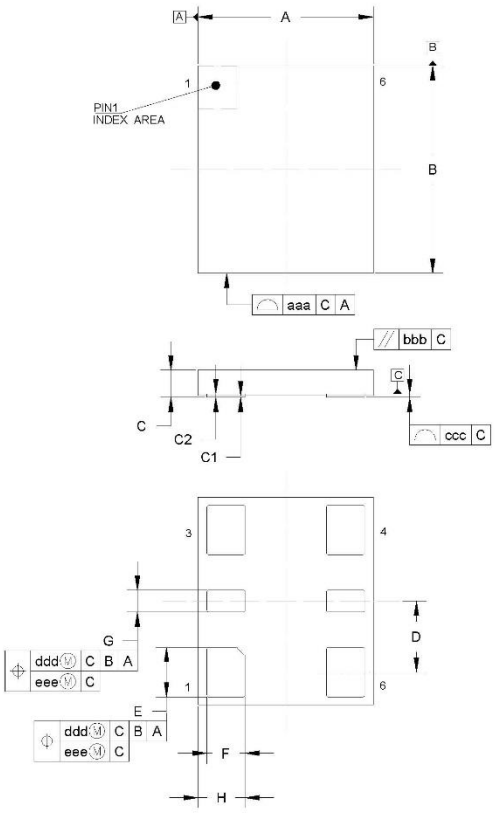


Figure 7.2. DSO3001 (5032) Outline Diagram

Table 7.2. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A		2.5 BSC	
B		3.2 BSC	
C	0.8	0.85	0.9
C1	0	0.035	0.05
C2		0.203 REF	
D		1.175 BSC	
E	0.6	0.65	0.7
F	0.65	0.7	0.75
G	0.45	0.5	0.55
H		0.8 REF	
aaa		0.1	
bbb		0.1	
ccc		0.08	
ddd		0.07	
eee		0.05	

Notes:

1. The dimensions in parentheses are reference.
2. All dimensions in millimeters (mm).
3. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

7.3 PCB

The figure below illustrates the PCB land pattern for the DSO3001. The table below lists the values for the dimensions shown in the illustration.

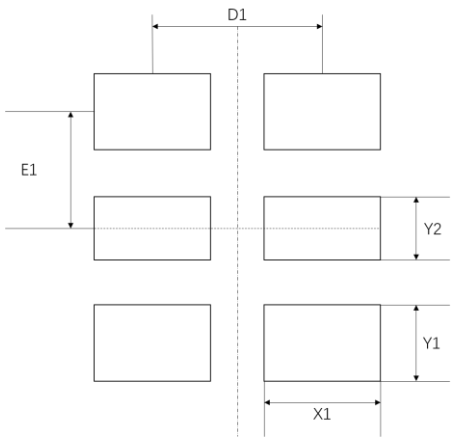


Figure 7.3. DSO3001 (5032 and 3225) PCB Land Pattern

Table 7.3. PCB Land Pattern Dimensions (mm)

Dimension	5032(mm)	3225(mm)
X1	0.75	0.7
Y1	0.64	0.65
Y2	0.64	0.5
D1	2.25	1.6
E1	1.27	1.05

7.4 Marking

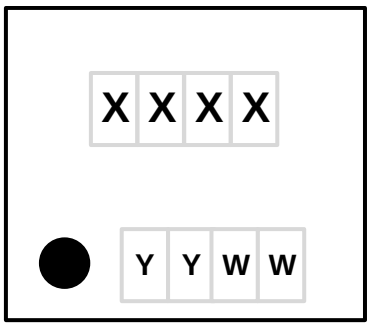


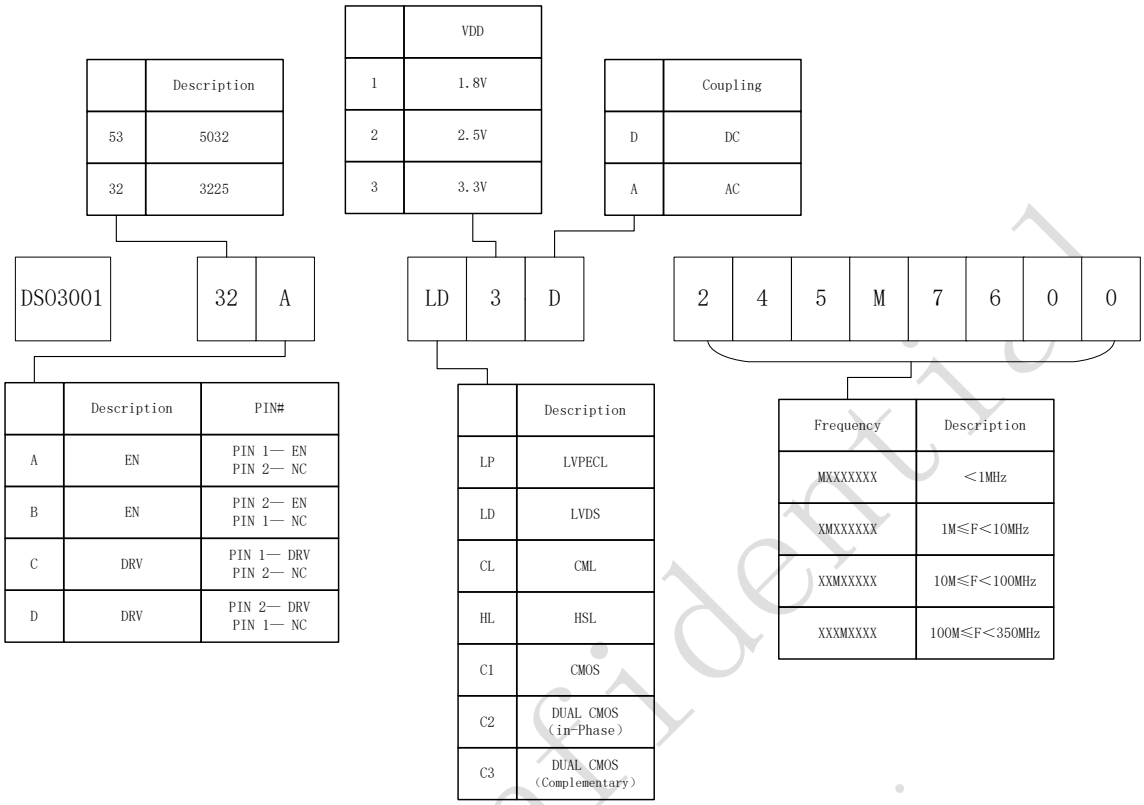
Figure 7.4 DSO3001 Top Mark

Table 7.4 Top Mark Description

Line	Print	Description
1	XXXX	LOGO
2	YYWW	DATE

8 Ordering Guide

The naming rules and definitions of DSO3001 are as follows:



Notes:

1. DSO3001-32A-LD3D-245M7600 means a silicon crystal with 3225 package, 1 pin defined as EN, input voltage 3.3V, output 245.76M DC-coupled LVDS signal.

2. Recommended Signal Formats and Voltage Combinations

Signal Format	VDD	Coupling
LVPECL	2.5V/3.3V	DC/AC
LVDS	1.8V/2.5V/3.3V	DC
CML	1.8V/2.5V/3.3V	AC
HCSL(50Ω termination)	1.8V/2.5V/3.3V	DC
HCSL(42.5Ω termination)	1.8V/2.5V/3.3V	DC
CMOS/Dual CMOS	1.8V/2.5V/3.3V	DC

Appendix

Recommended Output Terminations

CMOS

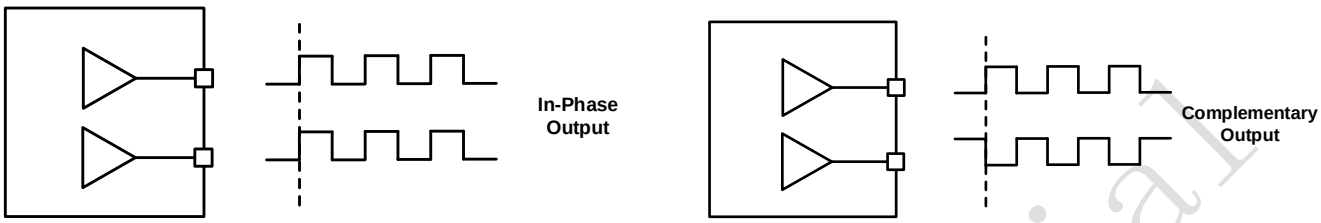
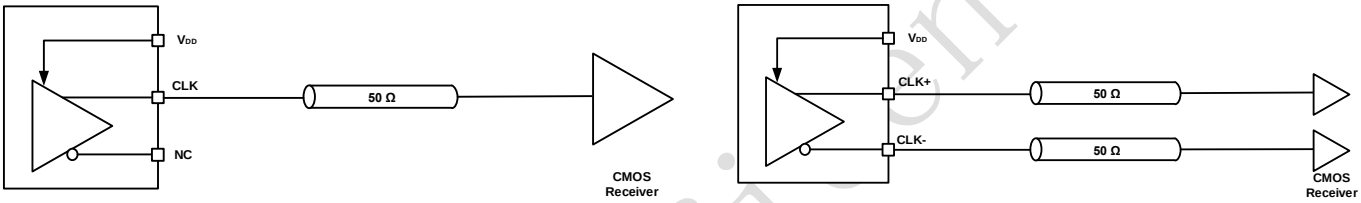


Figure 1 Dual CMOS Output

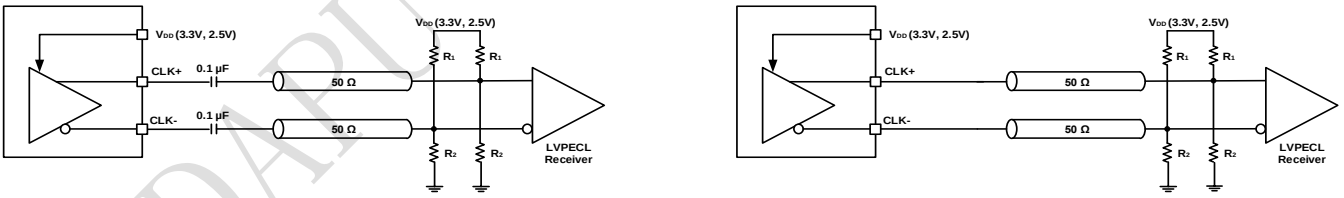


Single CMOS Termination **Dual CMOS Termination**

Figure 2. CMOS Output Termination

LVPECL

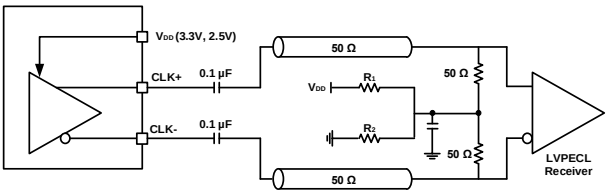
The output drivers support AC-coupled or DC-coupled terminations as shown in figures below.



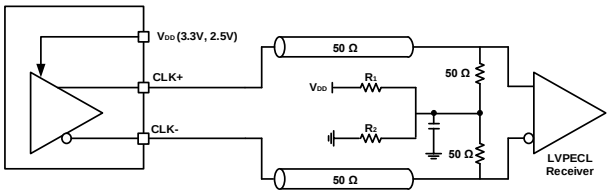
AC-Coupled LVPECL – Thevenin Termination **DC-Coupled LVPECL – Thevenin Termination**

Table 1. Termination Resistor Values

V_{DD}	R_1	R_2
3.3 V	127 Ω	82.5 Ω
2.5 V	250 Ω	62.5 Ω



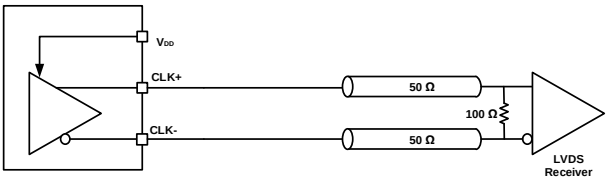
AC-Coupled LVPECL – 50 Ω w/ VTT Bias



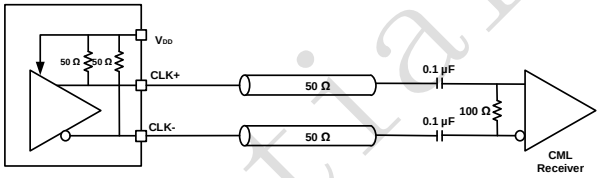
DC-Coupled LVPECL – 50 Ω w/ VTT Bias

Figure 3. LVPECL Output Terminations

LVDS/CML



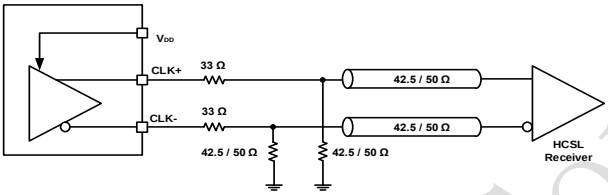
DC-Coupled LVDS



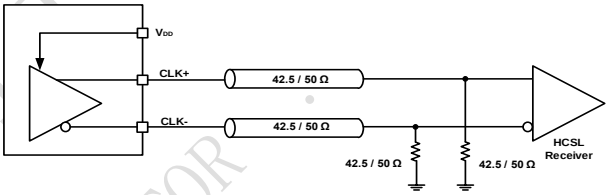
AC-Coupled CML

Figure 4. LVDS / CML Output Terminations

HCSL



Source Terminated HCSL



Destination Terminated HCSL

Figure 5. HCSL Output Terminations