

INS6310A —1:10 Ultra-Low Additive Jitter Differential Clock Buffer

FEATURES

- Two banks with 5 differential outputs each
 - LVPECL、LVDS、HCSL or Hi-Z (selectable per bank)
 - LVPECL additive jitter with clock source at 122.88MHz
 - 40 fs RMS (10KHz to 1MHz)
 - 80 fs RMS (12KHz to 20MHz)
- 3:1 Input Multiplexer
 - Two universal inputs operate up to 2.5GHz and accept LVPECL, LVDS, CML, SSTL, HSTL, HCSL or single-ended clocks
 - One crystal input accepts 10 to 40MHz crystal or single-ended clock
- High PSRR: -65/-76dBc (LVPECL/LVDS) at 156.25MHz
- LVC MOS output with synchronous enable input
- Pin-Controlled configuration
- V_{DD} core supply: $3.3V \pm 5\%$
- 3 independent V_{DDO} output supplies: $3.3V/2.5V \pm 5\%$
- Industrial temperature range: $-40^{\circ}C$ to $+85^{\circ}C$
- Package: QFN48(7.0mm*7.0mm*0.75mm)
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APPLICATIONS

- High speed Clock distribution and level translation
- Wireless BBU, RRU and Wired Communication
- Servers, Computing, PCI Express (PCIe)
- Switches, Routers, Line Cards, Timing Cards

GENERAL DESCRIPTIONS

The INS6310A is a high performance, versatility 10-output differential fanout buffer intended for high-frequency, low-jitter clock/data distribution and level translation. The input clock can be selected from two universal inputs or one crystal input. The selected input clock is distributed to two banks of 5 differential outputs and one LVC MOS output. Both differential output banks can be independently configured as LVPECL, LVDS, or HCSL drivers, or disabled. The LVC MOS output has a synchronous enable input for runt-pulse-free operation when enabled or disabled. The INS6310A operates from a 3.3V core supply and 3 independent 3.3V/2.5V output supplies.

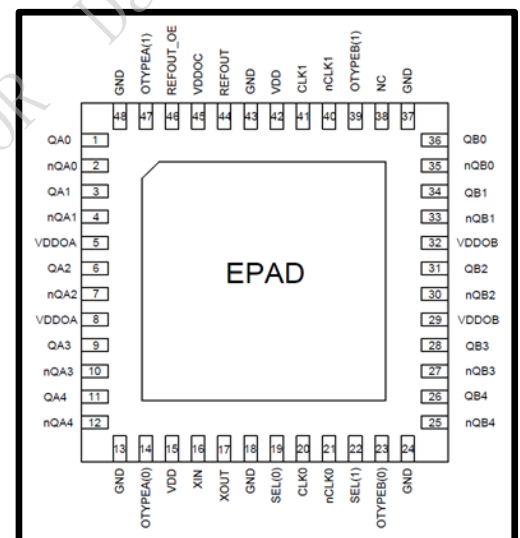


Table of Amendment

| Version | Revised Content | Draft | Revised Date |
|---------|---|-------|--------------|
| V1.0 | Chinese Version | | 2021.11.29 |
| V1.1 | English Version. Change V_{DDOX} maximum Voltage from 3.465V to 3.45V. | | 2022.02.08 |
| V1.2 | Error Correction: nQB* QB* pin swap in Pinouts diagram on Page 1 and Page 5 | | 2022.06.23 |
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Table of Contents

| | | |
|---|----------------------------------|----|
| 1 | GENERAL DESCRIPTION | 4 |
| 2 | FUNCTIONAL BLOCK DIAGRAM | 4 |
| 3 | PINOUTS | 5 |
| 4 | ELECTRICAL CHARACTERISTICS | 6 |
| 5 | FUNCTION DESCRIPTION | 14 |
| 6 | ENVIRONMENT | 21 |
| 7 | PACKAGE OUTLINE | 21 |

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1 GENERAL DESCRIPTION

The INS6310A is a 2.5-GHz, 10-output differential fanout buffer intended for high-frequency, low-jitter clock/data distribution and level translation. The input clock can be selected from two universal inputs or one crystal input. The selected input clock is distributed to two banks of 5 differential outputs and one LVCMOS output. Both differential output banks can be independently configured as LVPECL, LVDS, or HCSL drivers, or disabled. The LVCMOS output has a synchronous enable input for runt-pulse-free operation when enabled or disabled. The INS6310A operates from a 3.3V core supply and 3 independent 3.3V/2.5V output supplies.

The INS6310A provides high performance, versatility, and power efficiency, making it ideal for replacing fixed-output buffer devices while increasing timing margin in the system.

The INS6310A does not have power supply sequencing requirements between the core and output supply domains.

2 FUNCTIONAL BLOCK DIAGRAM



Figure 1. Block Diagram

3 PINOUTS

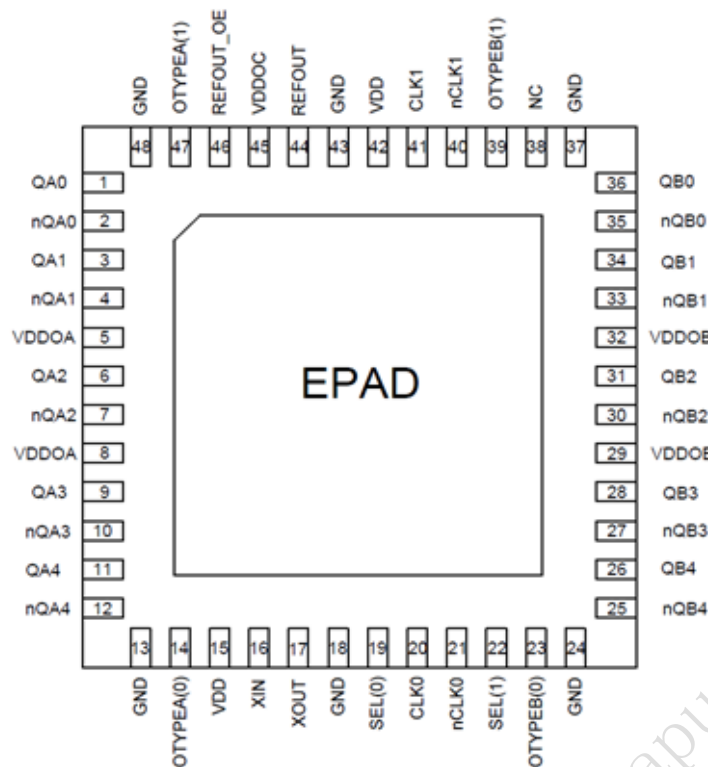


Figure 2. Pinouts Diagram

Table 1. Pin Definition

| PIN No. | PIN Name | TYPE | DESCRIPTIONS |
|------------------------|------------------------|------|---|
| 1,2 | QA0,nQA0 | OUT | Bank A Differential clock output 0 |
| 3,4 | QA1,nQA1 | OUT | Bank A Differential clock output 1 |
| 5,8 | V _{DDOA} | PWR | Power supply for Bank A output buffers. V _{DDOA} can operate from 3.3V or 2.5V. The V _{DDOA} pins are internally tied together. Bypass with a 0.1uF low-ESR capacitor placed very close to each V _{DDO} pin. |
| 6,7 | QA2,nQA2 | OUT | Bank A Differential clock output 2 |
| 9,10 | QA3,nQA3 | OUT | Bank A Differential clock output 3 |
| 11,12 | QA4,nQA4 | OUT | Bank A Differential clock output 4 |
| 13, 18, 24, 37, 43, 48 | GND | GND | Ground |
| 14,47 | OTYPEA[0] OTYPEA[1] | IN | Bank A Outputs selection pins. Pull down internally. |
| 15,42 | V _{DD} | PWR | Power supply for core and input buffer blocks. The V _{DD} supply operates from 3.3V. Bypass with a 0.1uF low-ESR capacitor placed very close to each V _{DD} pin. |

| PIN No. | PIN Name | TYPE | DESCRIPTIONS |
|---------|------------------------|------|---|
| 16 | X _{IN} | IN | Input for crystal. Can also be driven by a XO, TCXO, or other external single-ended clock. |
| 17 | X _{OUT} | OUT | Output for crystal. Leave X _{OUT} floating if X _{IN} is driven by a single-ended clock. |
| 19,22 | SEL[0] SEL[1] | IN | Clock input selection pins. Pull down internally. |
| 20,21 | CLK0,nCLK0 | IN | Universal clock input 0 (differential/single-ended). |
| 23,39 | OTYPEB[0] OTYPEB[1] | IN | Bank A Outputs selection pins. Pull down internally. |
| 25,26 | nQB4,QB4 | OUT | Bank B Differential clock output 4 |
| 27,28 | nQB3,QB3 | OUT | Bank B Differential clock output 3 |
| 29,32 | V _{DDOB} | PWR | Power supply for Bank A output buffers. V _{DDOA} can operate from 3.3V or 2.5V. The V _{DDOA} pins are internally tied together. Bypass with a 0.1uF low-ESR capacitor placed very close to each V _{DDO} pin. |
| 30,31 | nQB2,QB2 | OUT | Bank B Differential clock output 2 |
| 33,34 | nQB1,QB1 | OUT | Bank B Differential clock output 1 |
| 35,36 | nQB0,QB0 | OUT | Bank B Differential clock output 0 |
| 38 | NC | - | Not connected internally. Pin may be floated or grounded. |
| 40,41 | nCLK1,CLK1 | IN | Universal clock input 1 (differential/single-ended). |
| 44 | REFOUT | OUT | LVC MOS reference output. Enable output by pulling REFOUT_OE pin high. |
| 45 | V _{DDOC} | PWR | Power supply for Bank A output buffers. V _{DDOA} can operate from 3.3V or 2.5V. The V _{DDOA} pins are internally tied together. Bypass with a 0.1uF low-ESR capacitor placed very close to each V _{DDO} pin. |
| 46 | REFOUT_OE | IN | REFOUT enable input. Enable signal is internally synchronized to select clock input. Pull down internally. |
| | EPAD | | Connect to the PCB ground plane for heat dissipation. |

4 ELECTRICAL CHARACTERISTICS

Table 2. Absolute Maximum Ratings

Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters | Symbol | Value | Unit |
|------------|--------|-------|------|
|------------|--------|-------|------|

| | | | |
|---|--|--------------------|------|
| Power Supply Voltage | V_{DD} V_{DDOA} V_{DDOB} V_{DDOC} | -0.3~3.6 | V |
| Input Voltage | V_{IN} | -0.3~ $V_{DD}+0.3$ | V |
| Storage Temperature Range | T_{STG} | -65~150 | °C |
| Junction Temperature | T_J | 150 | °C |
| Thermal resistance from Junction to Ambient | θ_{JA} | 28.5 | °C/W |

Table 3. Recommended Parameters

| Parameters | Symbol | Value | | | Unit | Notes |
|-----------------------|--------------------|-------|------|-------|------|---|
| | | Min. | Typ. | Max. | | |
| Core Supply Voltage | V_{DD} | 3.15 | 3.3 | 3.45 | V | |
| Output Supply Voltage | $V_{DDOX}^{(1)}$ | 3.135 | 3.3 | 3.45 | V | |
| | | 2.375 | 2.5 | 2.625 | | |
| Core Supply Current | I_{VDD_CORE} | | 24 | 31 | mA | All Outputs Disabled. Clock input 0 or 1 Selected. |
| | | | 23 | 30 | mA | All Outputs Disabled. Xin Selected. |
| | I_{VDD_LVDS} | | 50 | 75 | mA | Additive Core Supply Current, Per LVDS Bank Enabled |
| | I_{VDD_LVPECL} | | 20 | 26 | mA | Additive Core Supply Current, Per LVPECL Bank Enabled |
| | I_{VDD_HCSL} | | 32 | 42 | mA | Additive Core Supply Current, Per HCSL Bank Enabled |
| | I_{VDD_LVCMOS} | | 4 | 5.2 | mA | Additive Core Supply Current, Per LVCMOS Bank Enabled |
| Output Supply Current | I_{VDDO_LVDS} | | 24 | 31 | mA | Additive Out Supply Current, Per LVDS Bank Enabled |
| | I_{VDDO_LVPECL} | | 230 | 299 | mA | Additive Out Supply Current, Per LVPECL Bank Enabled |
| | I_{VDDO_HCSL} | | 72 | 94 | mA | Additive Out Supply Current, Per HCSL Bank Enabled |
| | I_{VDDO_LVCMOS} | | 9 | 12 | mA | Additive Out Supply Current, Per LVCMOS Bank Enabled |
| Ambient Temperature | T_A | -40 | | 85 | °C | |

* (1) DDOX will represent DDOA/DDOB/DDOC in general when no distinction is needed

Table 4. Control Signals input Characteristics

Test Condition: $-40^{\circ}C \leq T_A \leq 85^{\circ}C, 3.15V \leq V_{DD} \leq 3.45V, 2.375V \leq V_{DDOX} \leq 2.625$ or $3.135V \leq V_{DDOX} \leq 3.45$

| Parameters | Symbol | Value | | | Unit | Notes |
|--|----------|-------|------|------|------|-------|
| | | Min. | Typ. | Max. | | |
| Control Signals (OTYPEA[0:1],OTYPEB[0:1],SEL[0:1],REFOUT_OE) | | | | | | |
| High Level Input | I_{IH} | | | 50 | uA | |

| | | | | | | |
|-------------------------|----------|-----|-----|----------|----|--|
| Current | | | | | | |
| Low Level Input Current | I_{IL} | -5 | 0.1 | 5 | uA | |
| Input High Voltage | V_{IH} | 1.6 | | V_{DD} | V | |
| Input Low Voltage | V_{IL} | 0 | | 0.4 | V | |

Table 5. CLKx/nCLKx⁽²⁾

Test Condition: $-40^{\circ}C \leq T_A \leq 85^{\circ}C, 3.15V \leq V_{DD} \leq 3.45V, 2.375V \leq V_{DDOX} \leq 2.625$ or $3.135V \leq V_{DDOX} \leq 3.45$, CLK driven differentially, input slew rate $\geq 3V/ns$

| Parameters | Symbol | Value | | | Unit | Notes |
|--|-----------------|-------|------|--------------|------|---|
| | | Min. | Typ. | Max. | | |
| CLKx Single-Ended Input Clock Specifications | | | | | | |
| Single-Ended Input High Voltage | V_{IH} | | | V_{DD} | V | CLKx driven single-ended (AC or DC coupled), nCLKx AC coupled to GND or externally biased within V_{CM} range |
| Single-Ended Input Low Voltage | V_{IL} | 0 | | | V | |
| Single-Ended Input Voltage Swing(P2P) | $V_{LSE}^{(3)}$ | 0.3 | | 2 | V | |
| Single-Ended Input Common-Mode Voltage | $V_{CM}^{(4)}$ | 0.25 | | $V_{DD}-1.2$ | V | |
| Differential Input Clock Specifications (CLKx/nCLKx) | | | | | | |
| Differential Input Voltage Swing | V_{ID} | 0.15 | | 1.3 | V | |
| Differential Input Common-Mode Voltage | $V_{CMD}^{(5)}$ | 0.25 | | $V_{DD}-0.9$ | V | $V_{ID}=800mV$ |
| | | 0.25 | | $V_{DD}-1.1$ | V | $V_{ID}=350mV$ |
| | | 0.25 | | $V_{DD}-1.2$ | V | $V_{ID}=150mV$ |
| Differential Input High Voltage | V_{IHD} | | | V_{DD} | V | |
| Differential Input Low Voltage | V_{ILD} | 0 | | | V | |
| Mux Isolation, CLKin0 to CLKin | ISO_{IN} | | -65 | | dBc | $F_{IN}=1000MHz$ |
| | | | -71 | | dBc | $F_{IN}=500MHz$ |
| | | | -82 | | dBc | $F_{IN}=200MHz$ |
| | | | -84 | | dBc | $F_{IN}=100MHz$ |
| Input Frequency (CLK/nCLK) | | | | | | |
| Input Frequency Range | F_{IN} | 0 | | 2500 | MHz | Functional up to 2.5GHz, Output frequency range and timing specified per output type (refer to LVPECL, LVDS, HCSL, LVCMOS output) |

| Parameters | Symbol | Value | | | Unit | Notes |
|-----------------|--------|-------|------|------|------|-------|
| | | Min. | Typ. | Max. | | |
| specifications) | | | | | | |

* (2) CLKx/nCLKx represent CLK0/nCLK0 和 CLK1/nCLK1

(3) For clock input frequency $\geq 100\text{MHz}$, CLKx can be driven with single-ended (LVCMOS) input swing up to 3.3VPP.

For clock input frequency $< 100\text{MHz}$, the single-ended input swing should be limited to 2VPP max to prevent input saturation (refer to Driving the Clock Inputs for interfacing 2.5V/3.3V LVCMOS clock input $< 100\text{MHz}$ to CLKx).

(4) CLKx driven single-ended (AC or DC coupled), nCLKx AC coupled to GND or externally biased within VCM range

(5) AC coupled must be applied when VCM of input signals exceed VCMD Max..

Table 6. XIN/XOUT Characteristics

Test Condition: $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $3.15\text{V} \leq V_{DD} \leq 3.45\text{V}$, $2.375\text{V} \leq V_{DDOX} \leq 2.625$ or $3.135\text{V} \leq V_{DDOX} \leq 3.45$

| Parameters | Symbol | Value | | | Unit | Notes |
|--------------------------------|-----------|-------|-------------|------|----------|-----------------------------------|
| | | Min. | Typ. | Max. | | |
| Crystal Input | | | | | | |
| Crystal Mode | | | Fundamental | | | |
| Crystal Frequency Input Range | fXIN/XOUT | 10 | | 40 | MHz | |
| Effective Series Resistance | ESR | | | 200 | Ω | 10MHz < fXIN \leq 30 MHz |
| | | 125 | | | Ω | 30MHz < fXIN < 40 MHz |
| Input Capacitance | CXO | | 4 | | pF | |
| Single-ended input | | | | | | |
| External Clock Input Frequency | fXIN | DC | | 250 | MHz | Single-Ended Input, Xout floating |

Table 7. LVDS Outputs Characteristics

Test Condition: $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $3.15\text{V} \leq V_{DD} \leq 3.45\text{V}$, $2.375\text{V} \leq V_{DDOX} \leq 2.625$ or $3.135\text{V} \leq V_{DDOX} \leq 3.45$,

CLK driven differentially, input slew rate $\geq 3\text{V/ns}$

| Parameters | Symbol | Value | | | Unit | Notes |
|----------------------------|-----------------|-------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| QAn/nQAn, QBn/nQBn | | | | | | |
| Maximum Output Frequency | FOUT-MAX | 1000 | 1600 | | MHz | Full VOD Swing, VOD > 250mV, RL = 100 Ω differential |
| | | 1500 | 2100 | | MHz | Reduced VOD Swing, VOD > 200mV, RL = 100 Ω differential |
| Output Voltage Swing | VOD | 250 | 400 | 450 | mV | TA = 25°C, DC Measurement, RL = 100 Ω differential |
| Change in Magnitude of VOD | ΔV_{OD} | -50 | | 50 | mV | |

| Parameters | Symbol | Value | | | Unit | Notes |
|--|--------------------------------------|-------|--------|-------|--------|---|
| | | Min. | Typ. | Max. | | |
| for Complementary Output States | | | | | | |
| Output Offset Voltage | V _{OFFSET} | 1.125 | 1.25 | 1.375 | V | |
| Change in Magnitude of V _{OFFSET} for Complementary Output States | ΔV _{OFFSET} | -35 | | 35 | mV | |
| Output Duty Cycle | Duty Cycle | 45 | 50 | 55 | % | |
| Output Rise/Fall Time, 20% to 80% | t _{Rise} /t _{Fall} | | 175 | 300 | ps | uniform transmission line up to 10 inches with 50Ω characteristic impedance, RL = 100Ω differential, C _L ≤ 5p |
| Propagation Delay | t _{Delay} | 200 | 400 | 600 | ps | RL = 100Ω differential, C _L ≤ 5pF |
| Output Skew | t _{Skew} | | 30 | 50 | ps | Skew specified between any two CLKouts with the same buffer type. Load conditions per output type are the same as propagation delay specifications. |
| Part-to-part Output Skew | t _{PDP} | | 80 | 120 | ps | |
| Additive RMS Jitter | t _J | | 132 | | fs | F _{IN} =100MHz Slew Rate≥3V/ns 1MHz to 20MHz |
| | | | 103 | | fs | F _{IN} =156.25MHz Slew Rate≥3V/ns 1MHz to 20MHz |
| | | | 33 | | fs | F _{IN} =625MHz Slew Rate≥3V/ns 1MHz to 20MHz |
| | | | 138 | | fs | F _{IN} =100MHz Slew Rate≥3V/ns 10kHz to 20MHz |
| | | | 99 | | fs | F _{IN} =156.25MHz Slew Rate≥3V/ns 10kHz to 20MHz |
| Noise Floor f _{OFFSET} ≥10MHz | NF | | -159.5 | | dBc/Hz | F _{IN} =100MHz Slew Rate≥3V/ns |
| | | | -157 | | dBc/Hz | F _{IN} =156.25MHz Slew Rate≥3V/ns |
| | | | -152.5 | | dBc/Hz | F _{IN} =625MHz Slew Rate≥3V/ns |

Table 8. LVPECL Outputs Characteristics

Test Condition: -40°C ≤ T_A ≤ 85°C, 3.15V ≤ V_{DD} ≤ 3.45V, 2.375V ≤ V_{DDOx} ≤ 2.625 or 3.135V ≤ V_{DDOx} ≤ 3.45, CLK driven differentially, input slew rate ≥ 3V/ns.

| Parameters | Symbol | Value | | | Unit | Notes |
|------------|--------|-------|------|------|------|-------|
| | | Min. | Typ. | Max. | | |
| | | | | | | |

| Parameters | Symbol | Value | | | Unit | Notes |
|------------------------------|----------------------|------------------------|-------------------------|------------------------|------|---|
| QAn/nQAn,QBn/nQBn | | | | | | |
| Maximum Output Frequency | F _{OUT-MAX} | 1000 | 1200 | | MHz | Full V _{OD} Swing , V _{OD} ≥ 600mV, R _L = 100Ω differential, V _{DDOX} =3.3V, R _T = 160Ω to GND |
| | | 750 | 1000 | | MHz | Full V _{OD} Swing , V _{OD} ≥ 600mV, R _L = 100Ω differential, V _{DDOX} =2.5V, R _T = 91Ω to GND |
| | | 1500 | 2200 | | MHz | Reduced V _{OD} Swing , V _{OD} ≥ 400mV, R _L = 100Ω differential, V _{DDOX} =3.3V, R _T = 160Ω to GND |
| | | 1500 | 2200 | | MHz | Reduced V _{OD} Swing , V _{OD} ≥ 400mV, R _L = 100Ω differential, V _{DDOX} =2.5V, R _T = 91Ω to GND |
| Output Voltage Swing | V _{OD} | 600 | 830 | 1000 | mV | T _A = 25°C, DC Measurement, R _T = 50Ω to V _{DDO} - 2V |
| Output High Voltage | V _{OH} | V _{DDOX} -1.2 | V _{DDOX} -0.9 | V _{DDOX} -0.7 | V | |
| Output Low Voltage | V _{OL} | V _{DDOX} -2.0 | V _{DDOX} -1.75 | V _{DDOX} -1.5 | V | |
| Output Duty Cycle | Duty Cycle | 45 | 50 | 55 | % | |
| Output Rise Time, 20% to 80% | t _{Rise} | | 250 | 350 | ps | R _T = 160Ω to GND, uniform transmission line up to 10 inches with 50Ω characteristic impedance, R _L = 100Ω differential, C _L ≤ 5pF |
| Output Fall Time, 80% to 20% | t _{Fall} | | 180 | 300 | ps | |
| Propagation Delay | t _{Delay} | 180 | 360 | 540 | ps | R _T = 160 Ω to GND, R _L = 50Ω differential, C _L ≤ 5pF |
| Output Skew | t _{Skew} | | 30 | 50 | ps | Skew specified between any two CLKouts with the same buffer type. Load conditions per output type are the same as propagation delay specifications. |
| Part-to-part Output Skew | t _{PDP} | | 80 | 120 | ps | |
| Additive RMS Jitter | t _j | | 55 | | fs | F _{IN} =100MHz Slew Rate≥3V/ns 1MHz to 20MHz |
| | | | 35 | | fs | F _{IN} =156.25MHz Slew Rate≥3V/ns 1MHz to 20MHz |
| | | | 25 | | fs | F _{IN} =625MHz Slew Rate≥3V/ns 1MHz to 20MHz |
| | | | 60 | 98 | fs | F _{IN} =100MHz Slew Rate≥3V/ns 10kHz to 20MHz |
| | | | 30 | 78 | fs | F _{IN} =156.25MHz Slew Rate≥3V/ns 10kHz to |

| Parameters | Symbol | Value | | | Unit | Notes |
|--|--------|-------|------|--|------------|---|
| | | | | | | 20MHz |
| Noise Floor $f_{\text{OFFSET}} \geq 10\text{MHz}$ | NF | | -161 | | dBc/ Hz | $F_{\text{IN}}=100\text{MHz}$ Slew Rate $\geq 3\text{V/ns}$ |
| | | | -159 | | dBc/ Hz | $F_{\text{IN}}=156.25\text{MHz}$ Slew Rate $\geq 3\text{V/ns}$ |
| | | | -154 | | dBc/ Hz | $F_{\text{IN}}=625\text{MHz}$ Slew Rate $\geq 3\text{V/ns}$ |

Table 9. HCSL Outputs Characteristics

Test Condition: $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $3.15\text{V} \leq V_{\text{DD}} \leq 3.45\text{V}$, $2.375\text{V} \leq V_{\text{DDOX}} \leq 2.625$ or $3.135\text{V} \leq V_{\text{DDOX}} \leq 3.45$, CLK driven differentially, input slew rate $\geq 3\text{V/ns}$.

| Parameters | Symbol | Value | | | Unit | Notes |
|--|-----------------------------------|-------|------|------|------------|---|
| | | Min. | Typ. | Max. | | |
| QAn/nQAn, QBn/nQBn | | | | | | |
| Output Frequency Range | F_{OUT} | 0 | | 400 | MHz | $R_L = 50\Omega$ to GND, $C_L \leq 5\text{pF}$ |
| Absolute Crossing Voltage | V_{CROSS} | 160 | 350 | 460 | mV | |
| Total Variation of V_{CROSS} | ΔV_{CROSS} | | | 140 | mV | |
| Output High Voltage | V_{OH} | 520 | 750 | 920 | mV | $T_A = 25^{\circ}\text{C}$, DC Measurement, $R_T = 50\Omega$ to GND |
| Output Low Voltage | V_{OL} | -150 | 0.5 | 150 | mV | |
| Output Duty Cycle | Duty Cycle | 45 | 50 | 55 | % | |
| Output Rise/Fall Time, 20% to 80% | $t_{\text{Rise}}/t_{\text{Fall}}$ | | 300 | 500 | ps | |
| Propagation Delay | t_{Delay} | 295 | 590 | 885 | ps | $R_T = 50\Omega$ to GND, $C_L \leq 5\text{pF}$ |
| Output Skew | t_{Skew} | | 30 | 50 | ps | Skew specified between any two CLKouts with the same buffer type. Load conditions per output type are the same as propagation delay specifications. |
| Part-to-part Output Skew | t_{PDP} | | 80 | 120 | ps | |
| Additive RMS Jitter | $t_{\text{j_PCIe}}$ | | 0.03 | 0.15 | ps | PCIe Gen 3, PLL BW = 2-5MHz, CDR = 10MHz, $F_{\text{IN}}=100\text{MHz}$ Slew Rate $\geq 0.6\text{V/ns}$ |
| | | | 0.03 | 0.05 | ps | PCIe Gen 4, PLL BW = 2-5MHz, CDR = 10MHz, $F_{\text{IN}}=100\text{MHz}$ Slew Rate $\geq 1.8\text{V/ns}$ |
| | t_{j} | | 77 | | fs | $V_{\text{DDO}} = 3.3\text{V}$, $R_T = 50\Omega$ to GND $F_{\text{IN}}=100\text{MHz}$ Slew Rate $\geq 3\text{V/ns}$ 1MHz to 20MHz |
| | | | 86 | | fs | $V_{\text{DDO}} = 3.3\text{V}$, $R_T = 50\Omega$ to GND $F_{\text{IN}}=156.25\text{Hz}$ Slew Rate $\geq 3\text{V/ns}$ 1MHz to 20MHz |
| Noise Floor $f_{\text{OFFSET}} \geq 10\text{MHz}$ | NF | | -161 | | dBc/ Hz | $V_{\text{DDO}} = 3.3\text{V}$, $R_T = 50\Omega$ to GND $F_{\text{IN}}=100\text{MHz}$ |

| Parameters | Symbol | Value | | | Unit | Notes |
|------------|--------|-------|------|--|--------|---|
| | | | | | | Slew Rate $\geq 3V/ns$ |
| | | | -156 | | dBc/Hz | $V_{DDO} = 3.3V$, $R_T = 50\Omega$ to GND $F_{IN} = 156.25Hz$ Slew Rate $\geq 3V/ns$ |

Table 10.LVCMOS Outputs Characteristics

Test Condition: $-40^{\circ}C \leq T_A \leq 85^{\circ}C$, $3.15V \leq V_{DD} \leq 3.45V$, $2.375V \leq V_{DDOX} \leq 2.625$ or $3.135V \leq V_{DDOX} \leq 3.45$, CLK driven differentially, input slew rate $\geq 3V/ns$.

| Parameters | Symbol | Value | | | Unit | Notes |
|---|------------------|------------------|------|------|--------|---|
| | | Min. | Typ. | Max. | | |
| Output High Voltage | V_{OH} | $V_{DDOX} - 0.1$ | | | V | 1mA Load |
| Output Low Voltage | V_{OL} | | | 0.1 | V | |
| Output High Current | I_{OH} | | 28 | | mA | $V_{DDOX} = 3.3V$ |
| | | | 20 | | mA | $V_{DDOX} = 2.5V$ |
| Output Low Current | I_{OL} | | 28 | | mA | $V_{DDOX} = 3.3V$ |
| | | | 20 | | mA | $V_{DDOX} = 2.5V$ |
| Output Frequency Range | F_{OUT} | 0 | | 300 | MHz | $CL \leq 5pF$ |
| Output Duty Cycle | Duty Cycle | 45 | 50 | 55 | % | 50% input clock duty cycle |
| Output Rise Time, 20% to 80% | t_{Rise} | | 225 | 500 | ps | 250MHz, uniform transmission line up to 10 inches with 50Ω characteristic impedance, $R_L = 50\Omega$ to GND, $C_L \leq 5pF$ |
| Output Fall Time, 20% to 80% | t_{Fall} | | 225 | 400 | ps | |
| Propagation Delay | t_{Delay} | 900 | 1475 | 2300 | ps | $V_{DDOX} = 3.3V$, $CL \leq 5pF$ |
| | | 1000 | 1550 | 2700 | ps | $V_{DDOX} = 2.5V$, $CL \leq 5pF$ |
| Additive RMS Jitter, BW = 1MHz to 20MHz | t_j | | 132 | | fs | $V_{DDO} = 3.3V$ $C_L \leq 5pF$ $F_{IN} = 100MHz$ |
| Noise Floor, $f_{OFFSET} \geq 10MHz$ | | | -158 | | dBc/Hz | Slew Rate $\geq 3V/ns$ |
| Output Enable/Disable Time | t_{EN}/t_{DIS} | | | 3 | Cycle | $C_L \leq 5pF$ |

5 FUNCTION DESCRIPTION

5.1 Control Signals

INS6310A has three groups of control signals:

- Input Selection
- Output Type Selection
- Reference Output Enable

Clock input selection is controlled using the SEL0 and SEL1 pins as shown in Table 11. Refer to Driving the Clock Inputs for clock input requirements. When CLK0 or CLK1 is selected, the crystal circuit is powered down. When Xin is selected, the crystal oscillator will start-up and its clock will be distributed to all outputs. Refer to Crystal Interface for more information. Alternatively, Xin may be driven by a single-ended clock, up to 250MHz, instead of a crystal.

Table 11. Input Selection

| SEL[1] | SEL[0] | Selected Input |
|--------|--------|-----------------------------------|
| 0 | 0 | CLK0/nCLK0 |
| 0 | 1 | CLK1/nCLK1 |
| 1 | x | X _{IN} /X _{OUT} |

The differential output buffer type for Bank A and Bank B outputs can be separately configured using the OTYPEA[1:0] and OTYPEB[1:0] inputs, respectively, as shown in table 12. For applications where all differential outputs are not needed, any unused output pin should be left floating with a minimum copper length to minimize capacitance and potential coupling and reduce power consumption. If an entire output bank will not be used, it is recommended to disable (Hi-Z) the bank to reduce power. Refer to Termination and Use of Clock Drivers for more information on output interface and termination techniques.

Table 12. Output Type Selection

| OTYPEx[1] | OTYPEx[0] | Output Type (BankA or B) |
|-----------|-----------|--------------------------|
| 0 | 0 | LVPECL |
| 0 | 1 | LVDS |
| 1 | 0 | HCSL |
| 1 | 1 | Hi-Z |

Notes: OTYPEx represent OTYPEA and OTYPEB

The reference output (REFOUT) provides a LVCMOS copy of the selected input clock. The LVCMOS output high level is referenced to the V_{DDO} voltage. REFOUT can be enabled or disabled using the enable input pin, REFOUT_OE, as shown in Table 13.

Table 13. Reference Output Enable

| REFOUT_OE | Reference Output State |
|-----------|------------------------|
| 0 | Hi-Z |
| 1 | Enabled |

5.2 Input Clocks

CLK/nCLK differential inputs: The INS6310A has two differential inputs (CLK0/nCLK0 and CLK1/nCLK1) that can accept AC or DC coupled 3.3V/2.5V LVPECL, LVDS, CML, SSTL and other differential and single-ended signals that meet the input requirements specified in ELECTRICAL CHARACTERISTICS. The device can accept a wide range of signals due to its wide input common mode voltage range (V_{CM}) and input voltage swing (V_{ID}). It is recommended that the inputs have a high slew rate of 3 V/ns (differential) or higher in case to degrade the noise floor and jitter. For this reason, a differential input signal is recommended over single-ended because it typically provides higher slew rate and common-mode noise rejection.

CLK/nCLK single-ended inputs: It is possible to drive it with a single-ended clock. For large single-ended input signals, such as 3.3V or 2.5V LVCMOS, a 50Ω load resistor should be placed near the input for signal attenuation to prevent input overdrive as well as for line termination to minimize reflections. The CLK input has an internal bias voltage of about 1.4V, so the input can be AC coupled as shown in Figure3. The output impedance of the LVCMOS driver plus R1 should be close to 50 Ω to match the characteristic impedance of the transmission line and load termination.



Figure 3. Single-Ended LVCMOS input, AC Coupling

A single-ended clock may also be DC coupled to CLKx as shown in Figure 4. A 50Ω load resistor should be placed near the CLKx input for signal attenuation and line termination. Because half of the single-ended swing of the driver ($V_{O,PP}/2$) drives CLKx, nCLKx should be externally biased to the midpoint voltage of the attenuated input swing ($(V_{O,PP}/2) \times 0.5$). The external bias voltage should be within the specified input common voltage (V_{CM}) range. This can be achieved using external biasing resistors in the kΩ range (R3 and R4) or another low-noise voltage reference. This will ensure the input swing crosses the threshold voltage at a point where the input slew rate is the highest.



Figure 4. Single-Ended LVCMOS input, DC Coupling

X_{IN}/X_{OUT}: If the crystal oscillator circuit is not used, it is possible to drive the X_{in} input with a single-ended external clock as shown in Figure 5. The input clock should be AC coupled to the X_{in} pin, which has an internally generated input bias voltage, and the X_{out} pin should be left floating. While X_{in} provides an alternative input to multiplex an external clock, it is recommended to use either differential input (CLK_x) since it offers higher operating frequency, better common mode, improved power supply noise rejection and greater performance over supply voltage and temperature variations.



Figure 5. X_{IN} Single-Ended LVCMOS Clock

The INS6310A has an integrated crystal oscillator circuit that supports a fundamental mode, AT-cut crystal. The crystal interface is shown in Figure 6, while C_L is specified for the crystal and C_{Shunt} is the sum of C_{IN} and PCB C_{STRAY}.

As shown in Figure 6, an external resistor, R_{LIMIT}, can be used to limit the crystal drive level if necessary. If the power dissipated in the selected crystal is higher than the drive level specified for the crystal with R_{LIMIT} shorted, then a larger resistor value is mandatory to avoid overdriving the crystal. However, if the power dissipated in the crystal is less than the drive level with R_{LIMIT} shorted, then a zero value for R_{LIMIT} can be used. As a starting point, a suggested value for RLIM is 1.5kΩ.

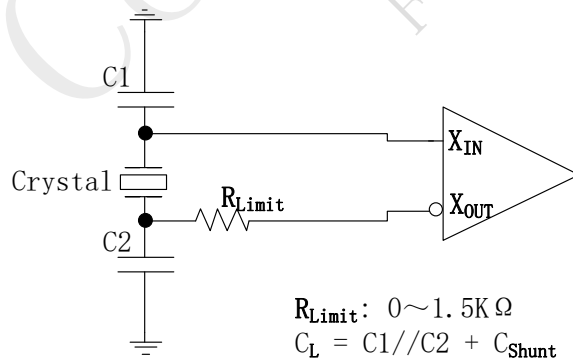


Figure 6. X_{IN}/X_{OUT} Crystal Interface

5.3 CLOCK OUTPUTS

INS6310A has two banks of 5 differential outputs and one LVCMOS output which can be independently supplied with 3.3V or 2.5V.

Table 14. Clock Outputs

| Bank | Outputs |
|--------|-------------------------|
| Bank A | QA0, QA1, QA2, QA3, QA4 |
| Bank B | QB0, QB1, QB2, QB3, QB4 |
| REFOUT | REFOUT |

Table 2 following will be the state of the outputs.

Table 15. Input Vs. Output States

| SEL[1] | Input Clock | Output State |
|------------|---------------------------------|--------------|
| Logic Low | CLKx=Open nCLKx=Open | Logic Low |
| | CLK= Logic High nCLK= Logic Low | Logic High |
| | CLK= Logic Low nCLK= Logic High | Logic Low |
| | CLK and nCLK short | Logic Low |
| Logic High | X _{IN} = Logic High | Logic Low |
| | X _{IN} = Logic Low | Logic High |

Notes

- Unused outputs should be left floating with a minimum copper length to minimize capacitance. In this way, this output will consume minimal output current because it has no load.

5.3.1 Termination and Use of Clock Drivers

When terminating clock drivers keep in mind these guidelines for optimum phase noise and jitter performance:

- Transmission line theory should be followed for good impedance matching to prevent reflections.
- Clock drivers should be presented with the proper loads.
 - LVDS outputs are current drivers and require a closed current loop.
 - HCSL drivers are switched current outputs and require a DC path to ground via 50Ω termination.
 - LVPECL outputs are open emitter and require a DC path to ground.
- Receivers should be presented with a signal biased to their specified DC bias level (common mode voltage) for proper operation. Some receivers have self-biasing inputs that automatically bias to the proper voltage level; in this case, the signal should normally be AC coupled.

It is possible to drive a non-LVPECL or non-LVDS receiver with a LVDS or LVPECL driver as long as the above guidelines are followed. Check the datasheet of the receiver or input being driven to determine the best termination and coupling method to be sure the receiver is biased at the optimum DC voltage (common mode voltage)

Termination for LVDS Driver

For DC coupled operation, terminate with 100Ω as close as possible to the LVDS receiver. For AC coupled operation by adding DC blocking capacitors, the load termination resistor and AC coupling capacitors should be placed as close as possible to the receiver inputs to minimize stub length, as shown in Figure 7



Figure 7. LVDS DC&AC Coupling

Termination for LVPECL Driver

For DC coupled operation of an LVPECL driver, terminate with $50\ \Omega$ to $V_{DDO} - 2V$. Alternatively terminate with a Thevenin equivalent circuit for V_{DDO} (output driver supply voltage) = 3.3V and 2.5V. In the Thevenin equivalent circuit, the resistor dividers set the output termination voltage (V_{TT}) to $V_{DDO} - 2V$. as shown in Figure 8



Figure 8. LVPECL DC Coupling

When AC coupling an LVPECL signal use $160\ \Omega$ emitter resistors (or $91\ \Omega$ for $V_{DDO} = 2.5V$) close to the LVPECL driver to provide a DC path to ground as shown in Figure 9. For proper receiver operation, the signal should be biased to the DC bias level (common mode voltage) specified by the receiver. The typical DC bias voltage (common mode voltage) for LVPECL receivers is 2.0V. Alternatively, a Thevenin equivalent circuit forms a valid termination as shown in Figure 9 for $V_{DDO} = 3.3V$ and 2.5V. This Thevenin circuit is different from the DC coupled example in Figure 8, since the voltage divider is setting the receiver input common mode voltage.



Figure 9. LVPECL AC coupling, Thevenin equivalent

Termination for HSCL Driver

For DC coupled operation of an HCSL driver, terminate with 50Ω to ground near the driver output as shown in Figure 10. Series resistors, R_s , may be used to limit overshoot due to the fast transient current. Because HCSL drivers require a DC path to ground, AC coupling is not allowed between the output drivers and the 50Ω termination resistors.



Figure 10. HCSL Operation, DC Coupling

5.4 Power Supply

The INS6310A operates from a 3.3V core supply and 3 independent 3.3V/2.5V output supplies.

VDD is INS6310A core supply voltage support 3.3V.

VDDOA, VDDOB and VDDOC are power supply for Bank A, B, C output buffers respectively. They can operate from 3.3V or 2.5V.

Notes

- V_{DDO} should be less than or equal to V_{DD} ($V_{DDO} \leq V_{DD}$)
 - .1uF or 0.01uF bypass capacitors should be placed very close to each supply pin
 - 1uF to 10uF Decoupling capacitors should be placed nearby
-

6 ENVIRONMENT

Table 16. ENVIRONMENT CONDITIONS

| Parameters | Value | Unit | Notes |
|------------|--------|------|---|
| ESD Level | ±2000V | V | HBM, Refer to ANSI/ESDA/JEDEC JS-001-2010 |
| | ±800V | V | CDM, Refer to JEDEC specification JESD22-C101 |

* HBM: Human body model

CDM: Charged-device model

7 PACKAGE OUTLINE

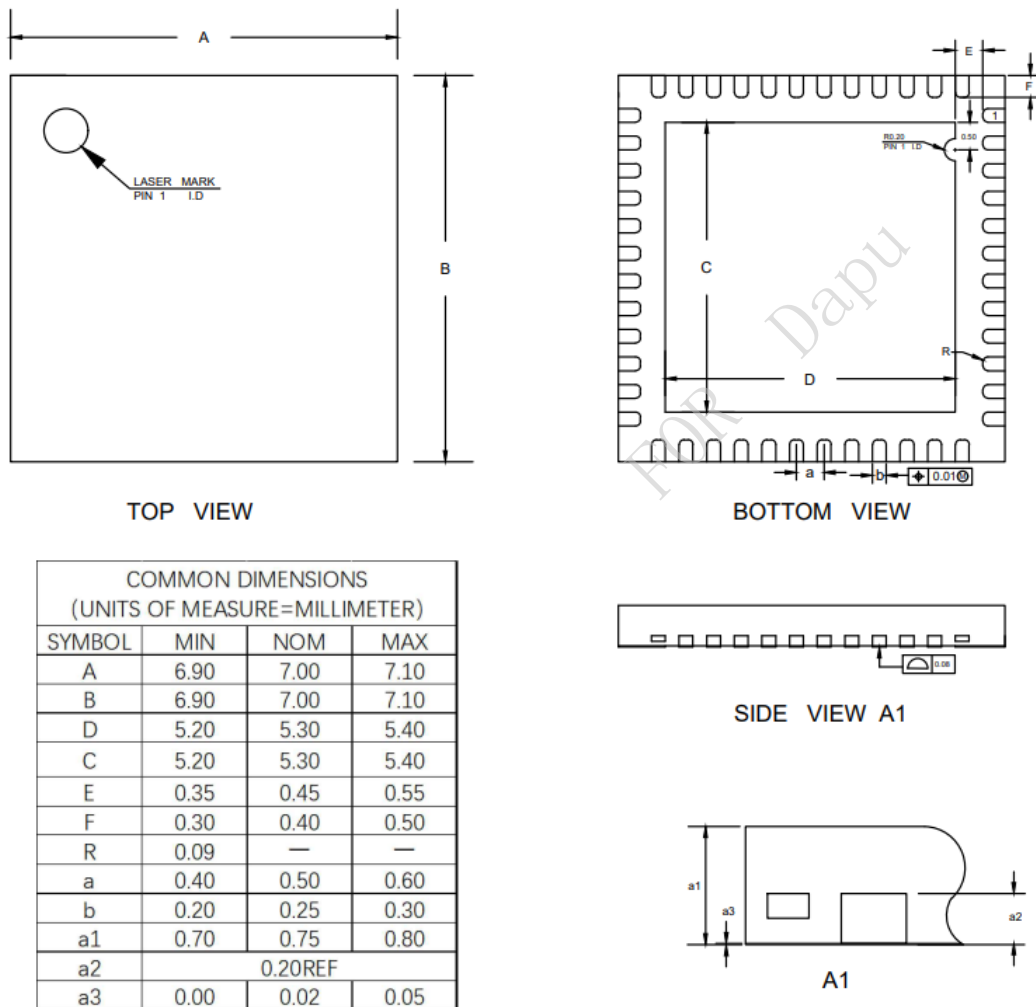


Figure 11. Package Outline Diagram