

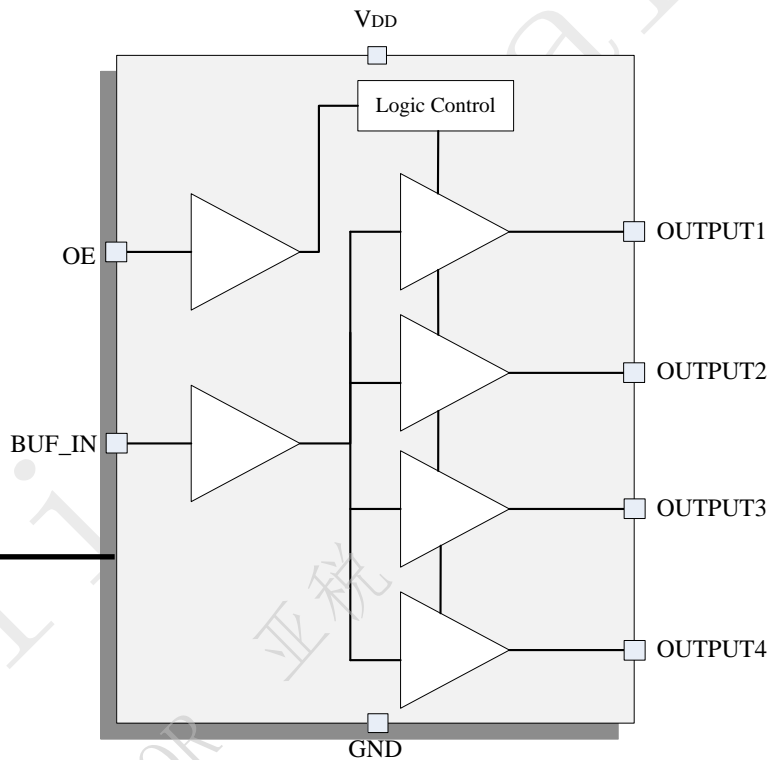
INS6104A —1:4 Low Skew Clock Buffer

FEATURES

- Low skew outputs (50ps)
- Low power CMOS technology
- Operating Voltages of 3.3V/2.5V \pm 5%
- Output Enable pin tri-states outputs
- 3.6 V tolerant input clock
- Totally Lead-Free & Fully RoHS Compliant
- Halogen and Antimony Free. “Green” Device
- Industrial temperature range: -40°C to +85°C
- Packaged: 8-pin SOIC

APPLICATIONS

- Wireless BBU, RRU and Wired Communication
- Servers, Computing, PCI Express (PCIe)
- Switches, Routers, Line Cards, Timing Cards



GENERAL DESCRIPTIONS

The INS6104A is a low skew, single input to four output, clock buffer. Perfect for fanning out multiple clock outputs. The input clock is distributed to four LVC MOS outputs which can be enabled or disabled by OE pin. The INS6104A operates from a 3.3V/2.5V power supply.

Table of Amendment

| Version | Revised Content | Draft | Revised Date |
|---------|-----------------|-------|--------------|
| V1.0 | First issued | | 2022.01.05 |
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1 GENERAL DESCRIPTION

The INS6104A is a low skew, single input to four output, clock buffer. Perfect for fanning out multiple clock outputs. The input clock is distributed to four LVCMOS outputs which can be enabled or disabled by OE pin. The INS6104A operates from a 3.3V/2.5V power supply.

2 FUNCTIONAL BLOCK DIAGRAM

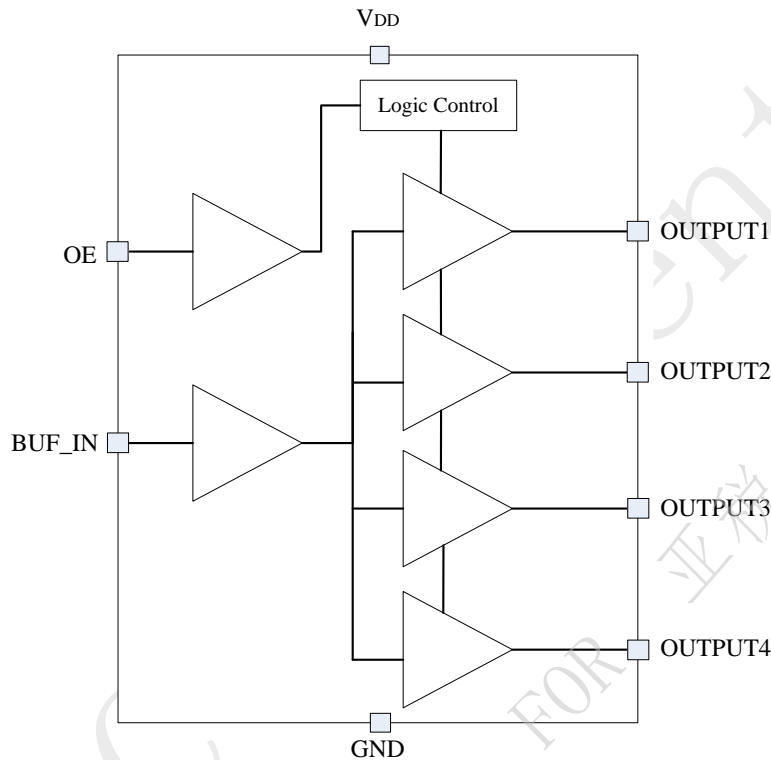


Figure 1. Block Diagram

3 PINOUTS

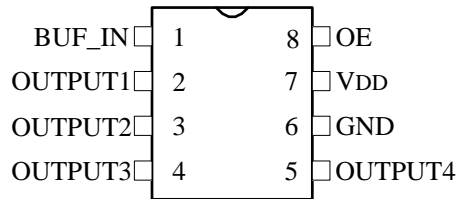


Figure 2. Pinouts Diagram

Table 1. Pin Definition

| PIN No. | PIN Name | TYPE | DESCRIPTIONS |
|---------|-----------------|------|--|
| 1 | BUF_IN | IN | Clock Input. 3.3 V tolerant input. |
| 2 | OUTPUT1 | OUT | Clock output 1 |
| 3 | OUTPUT2 | OUT | Clock output 2 |
| 4 | OUTPUT3 | OUT | Clock output 3 |
| 5 | OUTPUT4 | OUT | Clock output 4 |
| 6 | GND | GND | Ground |
| 7 | V _{DD} | PWR | 2.5V or 3.3V |
| 8 | OE | IN | Output Enable. Tri-states outputs when low. Connect to V _{DD} for normal operation. |

4 ELECTRICAL CHARACTERISTICS

Table 2. Absolute Maximum Ratings

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Parameter | Symbol | Rating | Unit |
|------------------------------|------------------|---------------------------|------|
| Power Supply | V _{DD} | -0.5~4.6 | V |
| Input Voltage | V _{IN} | -0.5~V _{DD} +0.5 | V |
| Output Voltage | V _{OUT} | -0.5~V _{DD} +0.5 | V |
| Storage Temperature Range | T _{STG} | -65~150 | °C |
| Maximum Junction Temperature | T _J | 150 | °C |
| Thermal Impedance | θ _{JA} | 123 | °C/W |

Table 3. Recommended Operating Conditions

Test Condition: $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$; It is recommended that the chip operates with the rated electrical range indicated in the table below.d

| Parameter | Symbol | Value | Unit | Comments |
|-----------|--------|-------|------|----------|
|-----------|--------|-------|------|----------|

| | | Min. | Typ. | Max. | | |
|--|------------------|-------|------|-------|----|---|
| Power Supply | V _{DD} | 3.135 | 3.3 | 3.465 | V | |
| | | 2.375 | 2.5 | 2.625 | | |
| Static Device Current | I _{VDD} | | 20 | | mA | V _{DD} =3.3V |
| Power dissipation capacitance per output | C _{PD} | | 9 | | pF | V _{DD} =3.3V, F _{OUT} =100MHz |
| Operating Temperature Range | T _A | -40 | | 85 | °C | |

Table 4. Control Signal Characteristics

Test Condition: $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $2.375\text{V} \leq V_{DD} \leq 3.465\text{V}$, $F_{IN/OUT}=100\text{MHz}$; Unless otherwise noted.

| Parameter | Symbol | Value | | | Unit |
|---------------------|-----------------|---------------------|------|---------------------|------|
| | | Min. | Typ. | Max. | |
| Control Signal (OE) | | | | | |
| Input High Current | I _{IH} | | | 40 | uA |
| Input Low Current | I _{IL} | -40 | | | uA |
| Input High Voltage | V _{IH} | 0.7*V _{DD} | | | V |
| Input Low Voltage | V _{IL} | | | 0.3*V _{DD} | V |

Table 5. BUF_IN Characteristics

Test Condition: $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $2.375\text{V} \leq V_{DD} \leq 3.465\text{V}$, Unless otherwise noted.

| Parameter | Symbol | Value | | | Unit |
|--------------------|----------------------|---------------------|------|---------------------|------|
| | | Min. | Typ. | Max. | |
| Frequency | F _{BUF_IN} | | | 100 | MHz |
| Input High Voltage | V _{BUF_INH} | 0.7*V _{DD} | | | V |
| Input Low Voltage | V _{BUF_INL} | -0.3 | | 0.3*V _{DD} | V |

Table 6. Output Characteristics

Test Condition: $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $2.375\text{V} \leq V_{DD} \leq 3.465\text{V}$, $F_{IN/OUT}=100\text{MHz}$, $C_L=5\text{pF}/50\ \Omega$; Unless otherwise noted.

| Parameter | Symbol | Value | | | Unit | Comments |
|---------------------|----------------------------------|---------------------|------|---------------------|------|---------------------------------|
| | | Min. | Typ. | Max. | | |
| Output High Voltage | V _{OH} | 0.8*V _{DD} | | | V | V _{DD} =2.375~3.465V |
| Output High Voltage | V _{OL} | | | 0.2*V _{DD} | V | V _{DDOX} =2.375~3.465V |
| Output impedance | R _O | | 15 | | Ω | V _{DD} =3.3V |
| | | | 20 | | Ω | V _{DD} =2.5V |
| Output Frequency | F _{OUT} | 0 | | 100 | MHz | |
| Duty Cycle | Duty Cycle | 45 | 50 | 55 | % | |
| Output Skew | t _{skew} ^(*) | | 30 | 50 | ps | |
| Part-to-part skew | t _{PDP} ^(*) | | | 2 | ns | |

| | | | | | | |
|---------------------------------|-----------------------|-----|------|-----|-------|---|
| Output Delay | t_{Delay} | 1.5 | 1.95 | 4.0 | ns | $V_{DD}=3.3V$ |
| | | 1.8 | 2.4 | 4.4 | ns | $V_{DD}=2.5V$ |
| Rise/Fall Time | t_{Rise} / t_{Fall} | | 3.0 | | ns | $V_{DD}=3.3V$ $C_L=15pF$ |
| | | | 4.4 | | ns | $V_{DD}=3.3V$ $C_L=50pF$ |
| | | | 5.0 | | ns | $V_{DD}=3.3V$ $C_L=100pF$ |
| Additive RMS Phase Jitter (RMS) | t_j | | 50 | | fs | $F_{OUT}=25MH$ Input skew rate $\geq 2V/ns$ $C_L=5pF$ 12kHzto20MHz |
| Output enable or disable time | t_{EN} | | | 2 | Cycle | |

* Parameter is specified by design, not tested in production

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5 FUNCTION DESCRIPTION

5.1 Control Signals

The outputs provide 4 LVCMOS copy of the input clock. The LVCMOS output high level is referenced to the V_{DD} voltage. The outputs can be enabled or disabled using the enable input pin, OE, as shown in Table 7.

Table 7. Reference Output Enable

| OE | Outputs State |
|----|---------------|
| 0 | Hi-Z |
| 1 | Enabled |

5.2 Input Clock

The BUF_IN input could be a LVCMOS clock up to 100MHz as shown in Figure 3. It is better to route the clock trace on the component side with a serial resistor close to the output pin ($\leq 200\text{mil}$).

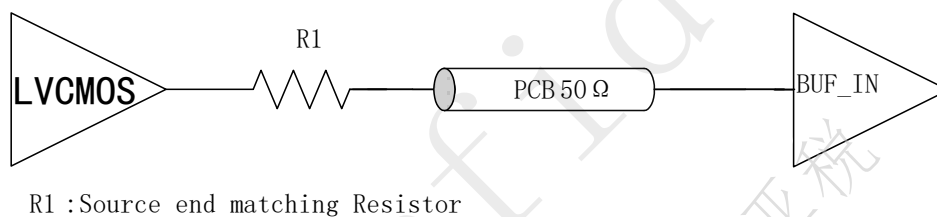


Figure 3. LVCMOS Input Clock

5.3 CLOCK OUTPUTS

INS6104A has 4 LVCMOS outputs OUTPUT1, OUTPUT2, OUTPUT3, OUTPUT4. A serial terminating resistor may be used on each clock output if the trace is longer than 1 inch.

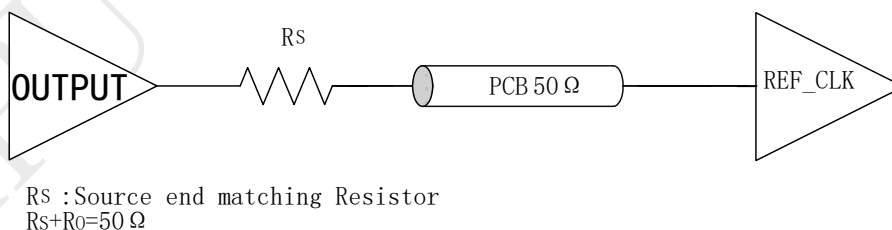


Figure 4. Output Termination

Notes

- Unused outputs could be left floating to minimize capacitance. In this way, this output will consume minimal output current because it has no load.

5.4 Power Supply

V_{DD} is INS6104A power supply voltage support 3.3V and 2.5V.

Notes

- .1uF or 0.01uF bypass capacitors should be placed very close to each supply pin
 - 1uF to 10uF Decoupling capacitors should be placed nearby
-

6 ENVIRONMENT

Table 8. ENVIRONMENT CONDITIONS

| Parameters | Value | Unit | Notes |
|------------|--------|------|---|
| ESD Level | ±2000V | V | HBM, Refer to ANSI/ESDA/JEDEC JS-001-2010 |
| | ±800V | V | CDM, Refer to JEDEC specification JESD22-C101 |

* HBM: Human body model

CDM: Charged-device model

7 PACKAGE OUTLINE

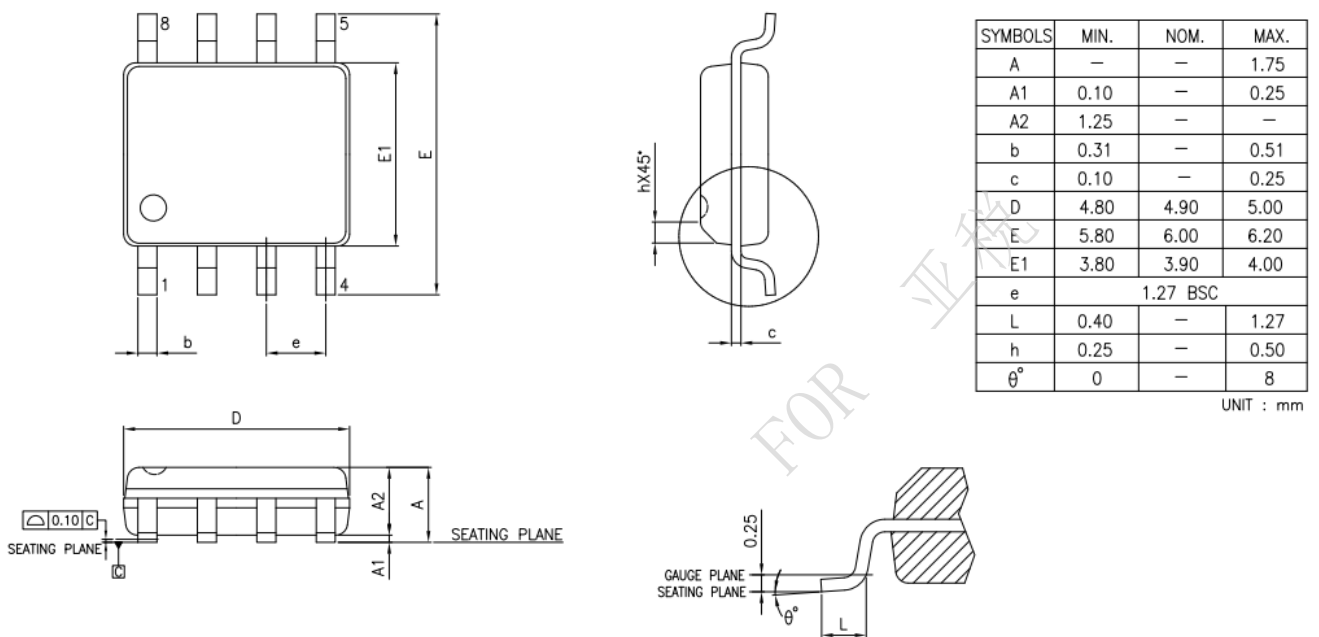


Figure 5. Package Outline Diagram