

To Customer: \_\_\_\_\_

# Realtime Clock Module

**INS5A4803**

## Datasheet

Document Version 1.0

Released on Dec. 30, 2022

| Product Name                     | Orderable Part Number |
|----------------------------------|-----------------------|
| INS5A4803<br>±5ppm @ -40°C~+85°C | INS5A4803             |
|                                  |                       |
|                                  |                       |

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# 1 Overview

INS5A4803 is a high-accuracy SPI bus interface real-time clock with low power consumption. It embeds a 32.768KHz TCXO. The high precise temperature sensor and temperature compensated circuit ensure the high clock accuracy. It supports calendar (year, month, day, hour, minute, second), clock and timer functions etc. The SOP package and AEC-Q100 compliant makes it suitable for automotive applications.

# 2 Block Diagram

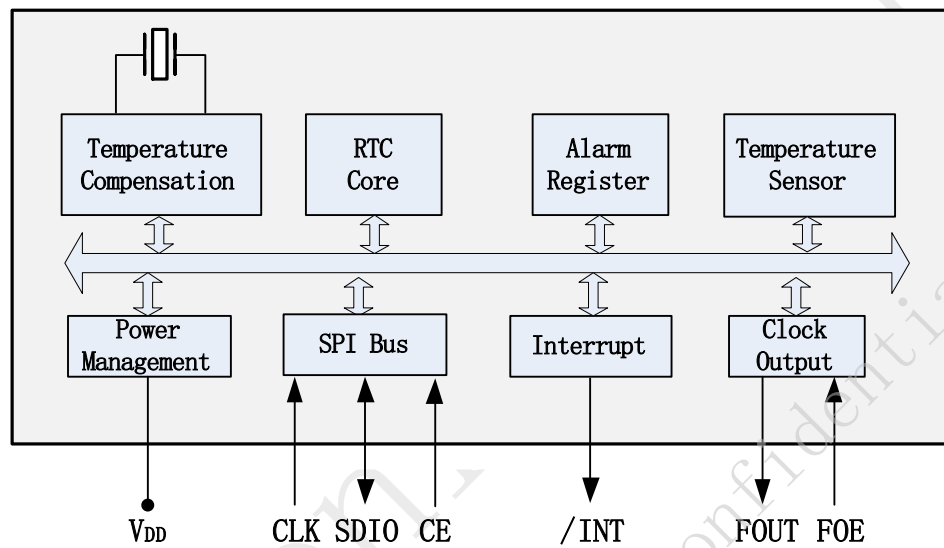
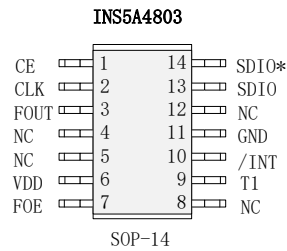


Figure 1. Block Diagram

# 3 Features

- Low current consumption: 1.0uA (Typ.)
- High stability:  
  - < ±5ppm @ -40°C~+85°C
- Communication Interface: SPI bus
- Build-in TCXO: 32.768KHz
- Build-in temperature sensor
- Power Supply Voltage: 1.6V~5.5V
- Operation Temperature Range: -40°C~+85°C
- Leap years autocorrection
- Timer output function with adjustable period
- Package: SOP14
- AEC-Q100 Compliant

## 4 Pin definition



**Table1. Pin Definition**

| Pin Number | Pin Name        | I/O     | Description   |
|------------|-----------------|---------|---|
| 1          | CE              | In      | 3-wire SPI chip select pin. Internal pull-down.<br>High: the chip is selected, access is allowed.<br>Low: access the chip is forbidden. |
| 2          | CLK             | In      | 3-wire SPI serial clock input pin. Cannot be left floating in normal mode.  |
| 3          | FOUT            | Out     | Frequency output. Controlled by FOE. Frequency can be set by FSEL bits.   |
| 4          | NC              | -       | Leave to be floating or connected to VDD or GND.  |
| 5          | NC              | -       | Leave to be floating or connected to VDD or GND.  |
| 6          | V <sub>DD</sub> | -       | Power supply  |
| 7          | FOE             | In      | FOUT output control pin. Cannot be left floating.<br>High: enable FOUT.<br>Low: FOUT Hi-Z.  |
| 8          | NC              | -       | Leave to be floating or connected to VDD or GND.  |
| 9          | T1              | -       | Ensure to be floating.  |
| 10         | /INT            | Out     | Interrupt Output, Open-Drain.   |
| 11         | GND             | -       | Ground  |
| 12         | NC              | -       | Leave to be floating or connected to VDD or GND.  |
| 13         | SDIO            | In/ Out | 3-wire SPI serial data input/output pin. Cannot be left floating in normal mode.  |
| 14         | SDIO*           | In/ Out | 3-wire SPI serial data input/output pin. Cannot be left floating in normal mode.  |

\*Note: pin13 and pin14 are connected internal.

## 5 Electrical Characteristics

### 5.1 Absolute Maximum Ratings

**Table2. Absolute Maximum Ratings**

| Parameter            | Symbol            | Value   |      |                      | Unit | Notes              |
|----------------------|-------------------|---------|------|----------------------|------|--------------------|
|                      |                   | Min.    | Typ. | Max.                 |      |                    |
| Power Supply Voltage | V <sub>DD</sub>   | -0.3    |      | 6.5                  | V    |                    |
| Input Voltage        | V <sub>IN</sub>   | GND-0.3 |      | 6.5                  | V    | FOE, CLK, SDIO, CE |
| Clock Output Voltage | V <sub>OUT1</sub> | GND-0.3 |      | V <sub>DD</sub> +0.3 | V    | FOUT               |
| Output Voltage       | V <sub>OUT2</sub> | GND-0.3 |      | 6.5                  | V    | SDIO, /INT         |
| Storage temperature  | T <sub>STG</sub>  | -55     |      | 125                  | °C   |                    |

### 5.2 Recommended Operating Conditions

**Table3. Recommended Operating Conditions**

| Parameter             | Symbol           | Value |      |      | Unit | Notes |
|-----------------------|------------------|-------|------|------|------|-------|
|                       |                  | Min.  | Typ. | Max. |      |       |
| Power Supply Voltage  | V <sub>DD</sub>  | 1.6   | 3.0  | 5.5  | V    |       |
| Operation temperature | T <sub>OPR</sub> | -40   | 25   | 85   | °C   |       |

Note 1: V<sub>DD</sub> need to be supplied with more than 2.5V at least for the oscillation to stabilize (oscillation start time t<sub>STA</sub>).

Note2: After powered off, ensure that V<sub>DD</sub>=GND for more than 10 seconds before next power on

Note3: If there is no special indication, the test conditions are GND = 0V, VDD = 2.5V ~ 5.5V, Ta = - 40 °C ~ + 85 °C

### 5.3 Frequency Characteristics

**Table4. Frequency Characteristics**

| Parameter                   | Symbol            | Value |      |      | Unit | Notes                 |
|-----------------------------|-------------------|-------|------|------|------|-----------------------|
|                             |                   | Min.  | Typ. | Max. |      |                       |
| Frequency stability         | Δf/f              | -5    |      | 5    | ppm  | -40°C~+85°C           |
| Oscillation start time      | t <sub>STA</sub>  |       |      | 1    | s    | @25°C                 |
| Year Aging                  | f <sub>a</sub>    | -3    |      | 3    | ppm  | @25°C, First year     |
| Temperature Sensor Accuracy | T <sub>emp</sub>  | -5    |      | 5    | °C   | V <sub>DD</sub> =3.0V |
| FOUT duty cycle             | t <sub>w</sub> /t | 40    | 50   | 60   | %    |                       |

Note: If there is no special indication, the test conditions are GND = 0V, VDD = 2.5V ~ 5.5V, Ta = - 40 °C ~ + 85 °C

### 5.4 DC Characteristics

**Table5. DC Characteristics**

| Parameter                    | Symbol           | Value               |      |                     | Unit | Notes  |   |
|------------------------------|------------------|---------------------|------|---------------------|------|--|---|
|                              |                  | Min.                | Typ. | Max.                |      |  |   |
| Average Current consumption1 | I <sub>DD1</sub> |                     | 1.25 | 5.1                 | uA   | V <sub>DD</sub> =5.0V  | f <sub>SCL</sub> =0Hz, FOE=GND, /INT = V <sub>DD</sub> ; FOUT off (High-Z); Compensation interval 2s;                   |
| Average Current consumption2 | I <sub>DD2</sub> |                     | 1.0  | 4.9                 |      | V <sub>DD</sub> =3.0V  |   |
| Average Current consumption3 | I <sub>DD3</sub> |                     | 5.8  | 20                  | uA   | V <sub>DD</sub> =5.0V  | f <sub>SCL</sub> =0Hz, FOE=V <sub>DD</sub> , /INT = V <sub>DD</sub> ; FOUT:32.768kHz, CL=0pF; Compensation interval 2s; |
| Average Current consumption4 | I <sub>DD4</sub> |                     | 3.8  | 19                  |      | V <sub>DD</sub> =3.0V  |   |
| High-level input voltage     | V <sub>IH</sub>  | 0.8*V <sub>DD</sub> |      | 5.5                 | V    | CE, CLK, SDIO, FOE   |   |
| Low-level input voltage      | V <sub>IL</sub>  | GND-0.3             |      | 0.2*V <sub>DD</sub> | V    |  |   |
| High-level output voltage    | V <sub>OH1</sub> | 4.0                 |      | 5.0                 | V    | V <sub>DD</sub> =5.0V, I <sub>OH</sub> = -1mA                | FOUT  |
|                              | V <sub>OH2</sub> | 2.2                 |      | 3.0                 |      | V <sub>DD</sub> =3.0V, I <sub>OH</sub> = -1mA                |   |
|                              | V <sub>OH3</sub> | 2.9                 |      | 3.0                 |      | V <sub>DD</sub> =3.0V, I <sub>OH</sub> = -100uA              |   |
| Low-level output voltage     | V <sub>OL1</sub> | GND                 |      | GND+0.5             | V    | V <sub>DD</sub> =5.0V, I <sub>OL</sub> = 1mA                 | FOUT  |
|                              | V <sub>OL2</sub> | GND                 |      | GND+0.8             |      | V <sub>DD</sub> =3.0V, I <sub>OL</sub> = 1mA                 |   |
|                              | V <sub>OL3</sub> | GND                 |      | GND+0.1             |      | V <sub>DD</sub> =3.0V, I <sub>OL</sub> = 100uA               |   |
|                              | V <sub>OL4</sub> | GND                 |      | GND+0.25            | V    | V <sub>DD</sub> =5.0V, I <sub>OL</sub> = 1mA                 | /INT  |
|                              | V <sub>OL5</sub> | GND                 |      | GND+0.4             |      | V <sub>DD</sub> =3.0V, I <sub>OL</sub> = 1mA                 |   |
|                              | V <sub>OL6</sub> | GND                 |      | GND+0.4             |      | V <sub>DD</sub> ≥3.0V, I <sub>OL</sub> = 3mA                 |   |
| Input leakage current        | I <sub>LK</sub>  | -0.5                |      | 0.5                 | uA   | CE, FOE, SDIO, CLK, V <sub>IN</sub> = V <sub>DD</sub> or GND |   |
| Output leakage current       | I <sub>OZ</sub>  | -0.5                |      | 0.5                 | uA   | FOUT, SDIO, /INT, V <sub>IN</sub> = V <sub>DD</sub> or GND   |   |

### 5.5 AC Characteristics

Table6. AC Characteristics

V<sub>DD</sub> =3.0V; GND=0V; Ta=-40°C~+85°C

| Parameter             | Symbol            | Value |      |      | Unit | Notes |
|-----------------------|-------------------|-------|------|------|------|-------|
|                       |                   | Min.  | Typ. | Max. |      |       |
| CLK clock cycle       | t <sub>CLK</sub>  | 330   | -    |      | ns   |       |
| CLK Low pulse width   | t <sub>LOW</sub>  | 160   | -    |      | ns   |       |
| CLK High pulse width  | t <sub>HIGH</sub> | 160   | -    |      | ns   |       |
| Write data setup time | t <sub>DS</sub>   | 50    | -    |      | ns   |       |
| Write data hold time  | t <sub>DH</sub>   | 50    | -    |      | ns   |       |
| CE setup time         | t <sub>CS</sub>   | 150   | -    |      | ns   |       |
| CE hold time          | t <sub>CH</sub>   | 150   | -    |      | ns   |       |



| Parameter            | Symbol     | Value |      |      | Unit | Notes   |
|----------------------|------------|-------|------|------|------|---------|
|                      |            | Min.  | Typ. | Max. |      |         |
| CLK rise & fall time | $t_{RF}$   |       | -    | 50   | ns   | 20%~80% |
| CE rise & fall time  | $t_{CERF}$ |       | -    | 50   | ns   | 20%~80% |

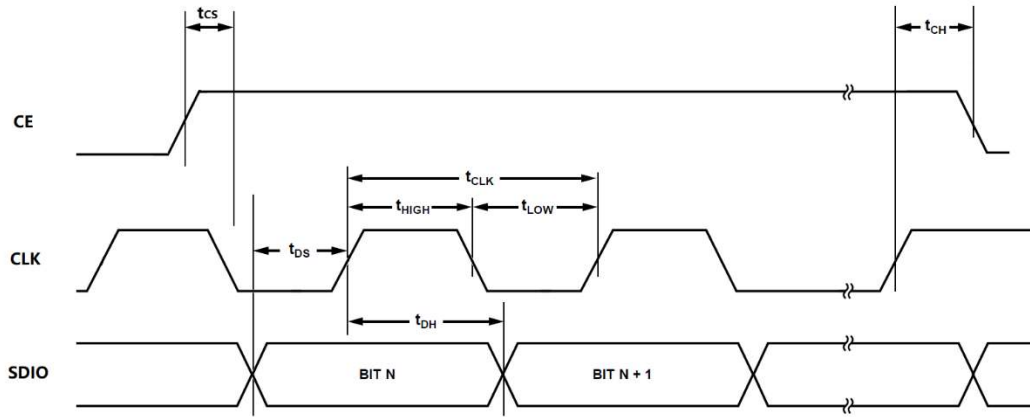


Figure 2. SPI bus Timing Chart

## 6 Registers

### 6.1 Register Lists

Address 0x00~0x0F: Basic Time and Calendar Registers

Address 0x10~0x1F: Extended Register Group 1

Address 0x20~30: Extended Register Group 2

Note: 0x10~16 and 0x00~06 with the same function, 0x1B~1F and 0x0B~0F with the same function

**Table 7. Basic Time and Calendar Registers**

| Address | Function           | bit7                           | bit6                             | bit5                           | bit4                            | bit3                             | bit2     | bit1     | bit0     | R/W |
|---------|--------------------|--------------------------------|----------------------------------|--------------------------------|---------------------------------|----------------------------------|----------|----------|----------|-----|
| 0x00    | SEC                | ○                              | BCD code, Second tens place, 0-5 |                                |                                 | BCD code, Second ones place, 0-9 |          |          |          | R/W |
| 0x01    | MIN                | ○                              | BCD code, Minute tens place, 0-5 |                                |                                 | BCD code, Minute ones place, 0-9 |          |          |          | R/W |
| 0x02    | HOUR               | ○                              | ○                                | BCD code, Hour tens place, 0-2 |                                 | BCD code, Hour ones place, 0-9   |          |          |          | R/W |
| 0x03    | WEEK               | ○                              | 6                                | 5                              | 4                               | 3                                | 2        | 1        | 0        | R/W |
| 0x04    | DAY                | ○                              | ○                                | BCD code, Day tens place, 0-3  |                                 | BCD code, Day ones place, 0-9    |          |          |          | R/W |
| 0x05    | MONTH              | ○                              | ○                                | ○                              | BCD code, Month tens place, 0-1 | BCD code, Month ones place, 0-9  |          |          |          | R/W |
| 0x06    | YEAR               | BCD code, Year tens place, 0-9 |                                  |                                |                                 | BCD code, Year ones place, 0-9   |          |          |          | R/W |
| 0x07    | RAM                | ●                              | ●                                | ●                              | ●                               | ●                                | ●        | ●        | ●        | R/W |
| 0x08    | MIN Alarm          | AE                             | BCD code, Minute tens place, 0-5 |                                |                                 | BCD code, Minute ones place, 0-9 |          |          |          | R/W |
| 0x09    | HOUR Alarm         | AE                             | ●                                | BCD code, Hour tens place, 0-2 |                                 | BCD code, Hour ones place, 0-9   |          |          |          | R/W |
| 0x0A    | WEEK Alarm         | AE                             | 6                                | 5                              | 4                               | 3                                | 2        | 1        | 0        | R/W |
|         | DAY Alarm          |                                | ●                                | BCD code, Day tens place, 0-3  |                                 | BCD code, Day ones place, 0-9    |          |          |          | R/W |
| 0x0B    | Timer Counter 0    | 128                            | 64                               | 32                             | 16                              | 8                                | 4        | 2        | 1        | R/W |
| 0x0C    | Timer Counter 1    | ●                              | ●                                | ●                              | ●                               | 2048                             | 1024     | 512      | 256      | R/W |
| 0x0D    | Extension Register | TEST                           | WADA                             | USEL                           | TE                              | FSEL [1]                         | FSEL [0] | TSEL [1] | TSEL [0] | R/W |
| 0x0E    | Flag Register      | ○                              | ○                                | UF                             | TF                              | AF                               | ○        | VLF      | Reserved | R/W |
| 0x0F    | Control Register   | CSEL [1]                       | CSEL [0]                         | UIE                            | TIE                             | AIE                              | ○        | ○        | RESET    | R/W |

**Table8. Extended Register Group 1**

| Address | Function           | bit7                           | bit6                             | bit5                           | bit4                            | bit3                             | bit2     | bit1     | bit0     | R/W |
|---------|--------------------|--------------------------------|----------------------------------|--------------------------------|---------------------------------|----------------------------------|----------|----------|----------|-----|
| 0x10    | SEC                | ○                              | BCD code, Second tens place, 0-5 |                                |                                 | BCD code, Second ones place, 0-9 |          |          |          | R/W |
| 0x11    | MIN                | ○                              | BCD code, Minute tens place, 0-5 |                                |                                 | BCD code, Minute ones place, 0-9 |          |          |          | R/W |
| 0x12    | HOUR               | ○                              | ○                                | BCD code, Hour tens place, 0-2 |                                 | BCD code, Hour ones place, 0-9   |          |          |          | R/W |
| 0x13    | WEEK               | ○                              | 6                                | 5                              | 4                               | 3                                | 2        | 1        | 0        | R/W |
| 0x14    | DAY                | ○                              | ○                                | BCD code, Day tens place, 0-3  |                                 | BCD code, Day ones place, 0-9    |          |          |          | R/W |
| 0x15    | MONTH              | ○                              | ○                                | ○                              | BCD code, Month tens place, 0-1 | BCD code, Month ones place, 0-9  |          |          |          | R/W |
| 0x16    | YEAR               | BCD code, Year tens place, 0-9 |                                  |                                |                                 | BCD code, Year ones place, 0-9   |          |          |          | R/W |
| 0x17    | TEMP               | 128                            | 64                               | 32                             | 16                              | 8                                | 4        | 2        | 1        | R   |
| 0x18    | RSV                | Reserved                       |                                  |                                |                                 |                                  |          |          |          | -   |
| 0x19    | Not use            | ○                              | ○                                | ○                              | ○                               | ○                                | ○        | ○        | ○        | R   |
| 0x1A    | Not use            | ○                              | ○                                | ○                              | ○                               | ○                                | ○        | ○        | ○        | R   |
| 0x1B    | Timer Counter 0    | 128                            | 64                               | 32                             | 16                              | 8                                | 4        | 2        | 1        | R/W |
| 0x1C    | Timer Counter 1    | ●                              | ●                                | ●                              | ●                               | 2048                             | 1024     | 512      | 256      | R/W |
| 0x1D    | Extension Register | TEST                           | WADA                             | USEL                           | TE                              | FSEL [1]                         | FSEL [0] | TSEL [1] | TSEL [0] | R/W |
| 0x1E    | Flag Register      | ○                              | ○                                | UF                             | TF                              | AF                               | ○        | VLF      | Reserved | R/W |
| 0x1F    | Control Register   | CSEL [1]                       | CSEL [0]                         | UIE                            | TIE                             | AIE                              | ○        | ○        | RESET    | R/W |

**Table9. Extended Register Group2**

| Address | Function          | bit7                        | bit6  | bit5  | bit4  | bit3        | bit2  | bit1  | bit0  | R/W |
|---------|-------------------|-----------------------------|-------|-------|-------|-------------|-------|-------|-------|-----|
| 0x20    | Device ID         | VendorID[3:0]               |       |       |       | Ver[3:0]    |       |       |       | R   |
| 0x21    | RSV               | Reserved: Ensure to be 0x80 |       |       |       |             |       |       |       | R/W |
| 0x22-24 | RSV               | Reserved: Ensure to be 0x00 |       |       |       |             |       |       |       | R/W |
| 0x25    | Frequency Offset0 | S [9]                       | S [8] | S [7] | S [6] | S [5]       | S [4] | S [3] | S [2] | R/W |
| 0x26    | Frequency Offset1 | S [1]                       | S [0] | D [5] | D [4] | D [3]       | D [2] | D [1] | D [0] | R/W |
| 0x27    | SubSEC            | Reserved                    |       |       |       | SubSEC[3:0] |       |       |       | R   |
| 0x28-30 | RSV               | Reserved: Ensure to be 0x00 |       |       |       |             |       |       |       | R/W |

Note:

1, After power-up reset or in case VLF bit returns “1”, make sure to initialize all registers to default state before using the RTC. Ensure all inputs are in the required range and the defined values are set for the reserved bits in case the clock cannot work normally.

- ✓ During the initial power-up, below bits will be in the state as below:
  - Initial 0:TEST, WADA, USEL, TE, FSEL[1:0], TSEL[0], UF, TF, AF, CSEL[1], UIE, TIE, RESET,
  - Initial 1:VLF, CSEL[0].
- ✓ All other register values are undefined, so make sure to reset the module before using it.
- ✓ The bits marked with “○” can be read out “0” only after initializing.
- ✓ The bits marked with “●” are RAM bits which can be used to write or read any data.
- ✓ Only 0 can be written to UF, TF, AF, VLF bits.
- ✓ Make sure “0” to be written for TEST bits which are used for testing only.
- ✓ Reserved bits must be set to the defined values accordingly.

## 6.2 Details of Registers

### 6.2.1 Clock counter registers

| Address | Function | bit7 | bit6                             | bit5                           | bit4 | bit3                             | bit2 | bit1 | bit0 | Default |
|---------|----------|------|----------------------------------|--------------------------------|------|----------------------------------|------|------|------|---------|
| 0x00/10 | SEC      | ○    | BCD code, Second tens place, 0-5 |                                |      | BCD code, Second ones place, 0-9 |      |      |      | 0x00    |
| 0x01/11 | MIN      | ○    | BCD code, Minute tens place, 0-5 |                                |      | BCD code, Minute ones place, 0-9 |      |      |      | 0x00    |
| 0x02/12 | HOUR     | ○    | ○                                | BCD code, Hour tens place, 0-2 |      | BCD code, Hour ones place, 0-9   |      |      |      | 0x00    |

SEC: BCD format, Value: 0~59

MIN: BCD format, Value: 0~59

HOUR: BCD format, Value: 0~23

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|------|------|------|------|------|------|---------|
| 0x03/13 | WEEK     | ○    | 6    | 5    | 4    | 3    | 2    | 1    | 0    | 0x40    |

WEEK: Value 01h, 02h, 04h, 08h, 10h, 20h, 40h. Only one bit can be set to 1 each time, all others must be set to 0.

**Table10. WEEK Register**

| WEEK      | Data | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|-----------|------|------|------|------|------|------|------|------|------|
| Sunday    | 01h  | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 1    |
| Monday    | 02h  | 0    | 0    | 0    | 0    | 0    | 0    | 1    | 0    |
| Tuesday   | 04h  | 0    | 0    | 0    | 0    | 0    | 1    | 0    | 0    |
| Wednesday | 08h  | 0    | 0    | 0    | 0    | 1    | 0    | 0    | 0    |
| Thursday  | 10h  | 0    | 0    | 0    | 1    | 0    | 0    | 0    | 0    |

| WEEK     | Data | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|----------|------|------|------|------|------|------|------|------|------|
| Friday   | 20h  | 0    | 0    | 1    | 0    | 0    | 0    | 0    | 0    |
| Saturday | 40h  | 0    | 1    | 0    | 0    | 0    | 0    | 0    | 0    |

| Address | Function | bit7 | bit6 | bit5                          | bit4 | bit3                          | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|-------------------------------|------|-------------------------------|------|------|------|---------|
| 0x04/14 | DAY      | ○    | ○    | BCD code, Day tens place, 0-3 |      | BCD code, Day ones place, 0-9 |      |      |      | 0x01    |

DAY: BCD format, the value range will be adjusted automatically according to the month setting and if a leap year or not .

**Table11. DAY Register Value**

| Month                   | Day Value Range |
|-------------------------|-----------------|
| 1, 3, 5, 7, 8, 10, 12   | 1~31            |
| 4, 6, 9, 11             | 1~30            |
| February in normal year | 1~28            |
| February in leap year   | 1~29            |

| Address | Function | bit7                           | bit6 | bit5 | bit4                            | bit3                            | bit2 | bit1 | bit0 | Default |
|---------|----------|--------------------------------|------|------|---------------------------------|---------------------------------|------|------|------|---------|
| 0x05/15 | MONTH    | ○                              | ○    | ○    | BCD code, Month tens place, 0-1 | BCD code, Month ones place, 0-9 |      |      |      | 0x01    |
| 0x06/16 | YEAR     | BCD code, Year tens place, 0-9 |      |      |                                 | BCD code, Year ones place, 0-9  |      |      |      | 0x00    |

MONTH: BCD format, Value1~12

YEAR: BCD format, Value0~99(2000~2099)

Example: 2020/01/01 Wednesday 21:18:36

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------|----------|------|------|------|------|------|------|------|------|
| 0x00/10 | SEC      | ○    | 0    | 1    | 1    | 0    | 1    | 1    | 0    |
| 0x01/11 | MIN      | ○    | 0    | 0    | 1    | 1    | 0    | 0    | 0    |
| 0x02/12 | HOUR     | ○    | ○    | 1    | 0    | 0    | 0    | 0    | 1    |
| 0x03/13 | WEEK     | ○    | 0    | 0    | 0    | 1    | 0    | 0    | 0    |
| 0x04/14 | DAY      | ○    | ○    | 0    | 0    | 0    | 0    | 0    | 1    |
| 0x05/15 | MONTH    | ○    | ○    | ○    | 0    | 0    | 0    | 0    | 1    |
| 0x06/16 | YEAR     | 0    | 0    | 1    | 0    | 0    | 0    | 0    | 0    |

### 6.2.2 Alarm registers

| Address | Function   | bit7 | bit6                             | bit5                           | bit4 | bit3                             | bit2 | bit1 | bit0 | Default |
|---------|------------|------|----------------------------------|--------------------------------|------|----------------------------------|------|------|------|---------|
| 0x08    | MIN Alarm  | AE   | BCD code, Minute tens place, 0-5 |                                |      | BCD code, Minute ones place, 0-9 |      |      |      | 0x00    |
| 0x09    | HOUR Alarm | AE   | ●                                | BCD code, Hour tens place, 0-2 |      | BCD code, Minute ones place, 0-9 |      |      |      | 0x00    |
| 0x0A    | WEEK Alarm | AE   | 6                                | 5                              | 4    | 3                                | 2    | 1    | 0    | 0x00    |
|         | DAY Alarm  |      | ●                                | BCD code, Day tens place, 0-3  |      | BCD code, Day ones place, 0-9    |      |      |      |         |

According to AIE, AF, WADA bits setting, the alarm interrupt will be generated once the current time match the settings in the above registers, the /INT pin goes to low level and AF bit is set to ‘1’ to record an alarm interrupt event has occurred.

WEEK Alarm/DAY Alarm: Controlled by WADA bit in 0x0D register

AE: Alarm Enable bit, 0-enable; 1-disenable

AF: Defined in 0x0E register bit3

AIE: Defined in 0x0F register bit3

### 6.2.3 Timer control registers

| Address | Function        | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|-----------------|------|------|------|------|------|------|------|------|---------|
| 0x0B/1B | Timer Counter 0 | 128  | 64   | 32   | 16   | 8    | 4    | 2    | 1    | 0x00    |
| 0x0C/1C | Timer Counter 1 | ●    | ●    | ●    | ●    | 2048 | 1024 | 512  | 256  | 0x00    |

According to TE, TF, TIE, TSEL[1:0] bits setting, a timer interrupt will be generated once the value counts down to 0 from the one set in the above registers.

TE: Defined in 0x0D register bit4

TF: Defined in 0x0E register bit4

TIE: Defined in 0x0F register bit4

TSEL [1:0]: Defined in 0x0D register bit1 and bit0

### 6.2.4 Extension registers

| Address | Function           | bit7 | bit6 | bit5 | bit4 | bit3    | bit2    | bit1    | bit0    | Default |
|---------|--------------------|------|------|------|------|---------|---------|---------|---------|---------|
| 0x0D/1D | Extension Register | TEST | WADA | USEL | TE   | FSEL[1] | FSEL[0] | TSEL[1] | TSEL[0] | 0x02    |

TEST: Test bit, must be set to“0”

WADA: Week Alarm/Day Alarm control bit, decide 0x0A register as DAY Alarm or WEEK Alarm. 0-WEEK alarm, 1-DAY alarm

USEL: Update Interrupt Select bit, 0-output interrupt once a second, 1-output interrupt once a minute

TE: Timer Enable bit, 0-disable, 1-enable

FSEL[1], FSEL[0]:FOUT frequency setting:

| FSEL[1] | FSEL[0] | FOUT Frequency     |
|---------|---------|--------------------|
| 0       | 0       | 32.768KHz(Default) |
| 0       | 1       | 1024Hz             |
| 1       | 0       | 1Hz                |
| 1       | 1       | 32.768KHz          |

TSEL[1], TSEL[0]:Timer countdown period(source clock) setting:

| TSEL[1] | TSEL[0] | Source clock |
|---------|---------|--------------|
| 0       | 0       | 4096Hz       |
| 0       | 1       | 64Hz         |
| 1       | 0       | 1Hz          |
| 1       | 1       | 1/60Hz       |

### 6.2.5 Flag registers

| Address | Function      | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0     | Default |
|---------|---------------|------|------|------|------|------|------|------|----------|---------|
| 0x0E/1E | Flag Register | ○    | ○    | UF   | TF   | AF   | ○    | VLF  | Reserved | 0x03    |

UF: Update flag bit. When time update interrupt event occurs, it will be set to “1” and keeps “1” until a “0” is written to it.

TF: Timer Flag bit. When a fixed-cycle timer interrupt event occurs, it will be set to “1” and keeps “1” until a “0” is written to it.

AF: Alarm Flag bit. When an alarm interrupt event occurs, it will be set to “1” and keeps “1” until a “0” is written to it.

VLF: Voltage Low Flag bit. When supply voltage is lower than 1.6V, it will be set to “1” and keeps “1” until a “0” is written to it.

### 6.2.6 Control registers

| Address | Function         | bit7     | bit6     | bit5 | bit4 | bit3 | bit2 | bit1 | bit0  | Default |
|---------|------------------|----------|----------|------|------|------|------|------|-------|---------|
| 0x0F/1F | Control Register | CSEL [1] | CSEL [0] | UIE  | TIE  | AIE  | ○    | ○    | RESET | 0x40    |

CSEL[1], CSEL[0]: Compensation interval Select 1, 0 bits, used to set temperature compensation interval.

| CSEL[1] | CSEL[0] | Compensation interval |
|---------|---------|-----------------------|
| 0       | 0       | 0.5s                  |
| 0       | 1       | 2s(default)           |
| 1       | 0       | 10s                   |
| 1       | 1       | 30s                   |

UIE: Update Interrupt Enable bit. When UF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).

TIE: Timer Interrupt Enable bit: When TF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).

AIE: Alarm Interrupt Enable bit: When AF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).

RESET: Reset IC, prepared for the synchronized starting of time or timer.

### 6.2.7 Temperature register

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------|----------|------|------|------|------|------|------|------|------|---------|
| 0x17    | TEMP     | 128  | 64   | 32   | 16   | 8    | 4    | 2    | 1    | 0x00    |

Read digital temperature data,  $Temp[^\circ C] = (TEMP[7:0] * 2 - 147.5) / 3.0448$ .

### 6.2.8 Device ID register

| Address | Function  | bit7           | bit6 | bit5 | bit4 | bit3     | bit2 | bit1 | bit0 | Default |
|---------|-----------|----------------|------|------|------|----------|------|------|------|---------|
| 0x20    | Device ID | Vendor ID[3:0] |      |      |      | Ver[3:0] |      |      |      | 0xD2    |

Vendor ID[3:0]:The fixed value is defined as Vendor ID[3:0]=1101b=Dh to represent DAPU.

Ver[3:0]: version of the IC

### 6.2.9 RSV register

| Address       | Function | bit7                   | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Default |
|---------------|----------|------------------------|------|------|------|------|------|------|------|---------|
| 0x21          | RSV      | Reserved: must be 0x80 |      |      |      |      |      |      |      | 0x80    |
| 0x22~<br>0x24 | RSV      | Reserved: must be 0x00 |      |      |      |      |      |      |      | 0x00    |

### 6.2.10 Frequency Offset register

| Address | Function          | bit7     | bit6     | bit5     | bit4     | bit3     | bit2  | bit1  | bit0  | Default |
|---------|-------------------|----------|----------|----------|----------|----------|-------|-------|-------|---------|
| 0x25    | Frequency Offset0 | Reserved | Reserved | Reserved | Reserved | Reserved | S [4] | S [3] | S [2] | 0x00    |
| 0x26    | Frequency Offset1 | S [1]    | S [0]    | D [5]    | D [4]    | D [3]    | D [2] | D [1] | D [0] | 0x00    |



S [4:0]: Sign bits. Only 2b' 0 0000 and 2b' 1 1111 is legitimate.

D [5:0]: Data bits

| S [4:0]    | D [5:0]    | Frequency Adjustment (ppm)      |
|------------|------------|---------------------------------|
| 2b' 0 0000 | 2b'00 0000 | 0 (Default)                     |
|            | 2b'00 0001 | -0.1                            |
|            | 2b'00 0010 | -0.2                            |
|            | ...        | ...                             |
|            | 2b'11 1110 | -6.2                            |
|            | 2b'11 1111 | -6.3                            |
| 2b' 1 1111 | 2b'11 1111 | +0.1                            |
|            | 2b'11 1110 | +0.2                            |
|            | ...        | ...                             |
|            | 2b'00 0010 | +6.2                            |
|            | 2b'00 0001 | +6.3                            |
| Other's    | Other's    | Invalid value, must be avoided. |

Note: \*The Frequency offset register affects the frequency stability. Please be careful if you adjust it.

The offset function is effective for frequency adjustment at the normal temperature.

The single adjustment amount of 0.1ppm is approximate value.

### 6.2.11 Sub-second timer register

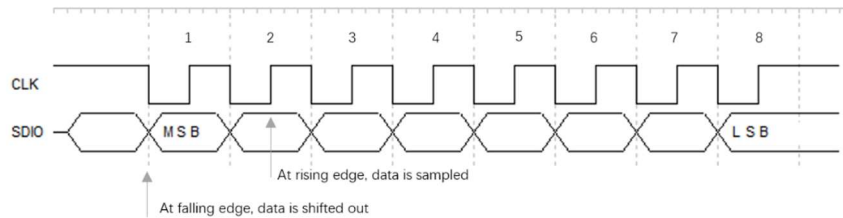
| Address | Function | bit7     | bit6 | bit5 | bit4 | bit3        | bit2 | bit1 | bit0 | Default |
|---------|----------|----------|------|------|------|-------------|------|------|------|---------|
| 0x27    | SubSEC   | Reserved |      |      |      | SubSEC[3:0] |      |      |      | 0x00    |

SubSEC[3:0]: sub second bit, and unit is 1/16s.

### 6.3 SPI Bus Interface

It is assumed CPU is master and INS5A4803 is slave in this section.

The INS5A4803 includes SPI as the slave interface. The INS5A4803 registers can be accessed via an SPI bus. The following figure shows the specifications of the INS5A4803 SPI interface. Data length is 8 bits and MSB first. CLK keeps high at idle. Maximum communication speed is 4Mbits/s. Address auto-increment function is included. The CE pin has a built-in pull-down.



#### 6.3.1 Write process

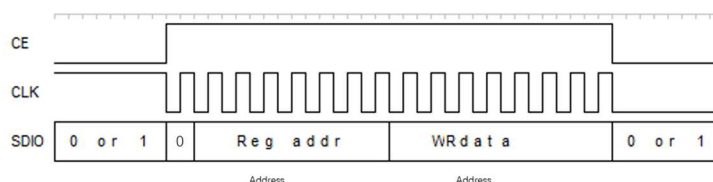
After the host pulls up the CE signal, the INS5A4803 is selected as the slave device to be accessed. Then the host starts to output CLK. The host first sends an 8-bit address data to the SDIO pin, the highest bit is the write flag bit, and the lower seven bits are the register address.

| Bit7           | Bit6                            | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|----------------|---------------------------------|------|------|------|------|------|------|
| 0              | Register address                |      |      |      |      |      |      |
| Write flag bit | 0x00~0x30, Refer to Section 6.1 |      |      |      |      |      |      |

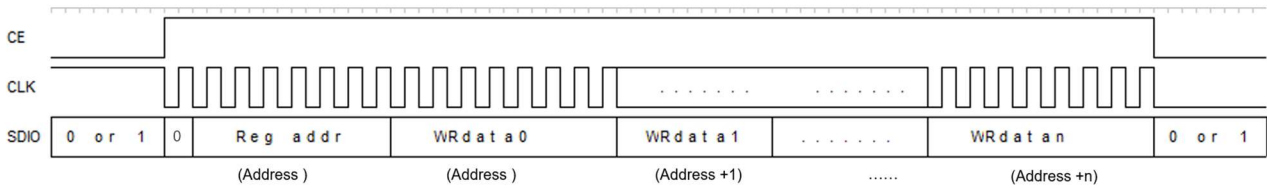
During the register data writing operation, each time 8-bit data is written, the data will be stored in the specified register address. When writing continuously, the lower 4 bits of the register address will be incremented automatically. When the low 4 bits of the register address exceed 0xF, they are recognized as 0x0. The high-order 3-bit address of the register is not incremented automatically. If necessary, cancel the CE signal and restart the next write operation.

Do not set the CE signal to low level before the last 8-bit data is completely transmitted. If the CE signal is set to low level during transmission, 8-bit data that has not been sent will be lost and will not be written to the register.

Single register write operation:



Continuous register write operation:



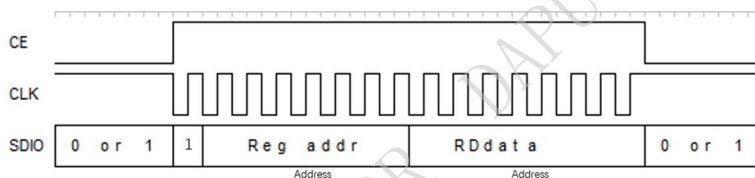
6.3.2 Read process

After the host pulls up the CE signal, the INS5A4803 is selected as the slave device to be accessed. Then the host starts to output CLK. The host first sends an 8-bit address data (register address) to the DIO pin of the INS5A4803, including the read flag bit. After receiving the address data, the INS5A4803 sends the read data from the DIO pin to the host in 8-bit units until the host stops outputting the clock.

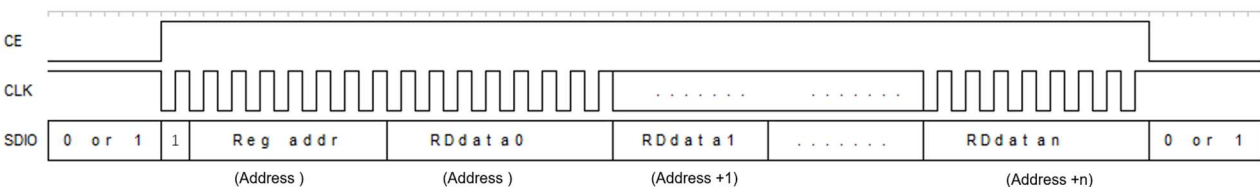
| Bit7          | Bit6                            | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------------|---------------------------------|------|------|------|------|------|------|
| 1             | Register address                |      |      |      |      |      |      |
| Read flag bit | 0x00~0x30, Refer to Section 6.1 |      |      |      |      |      |      |

When reading continuously, the lower 4 bits of the register address will be incremented automatically. When the low 4 bits of the register address exceed 0xF, they are recognized as 0x0. The high-order 3-bit address of the register is not incremented automatically. If necessary, cancel the CE signal and restart the next read operation.

Single register read operation:

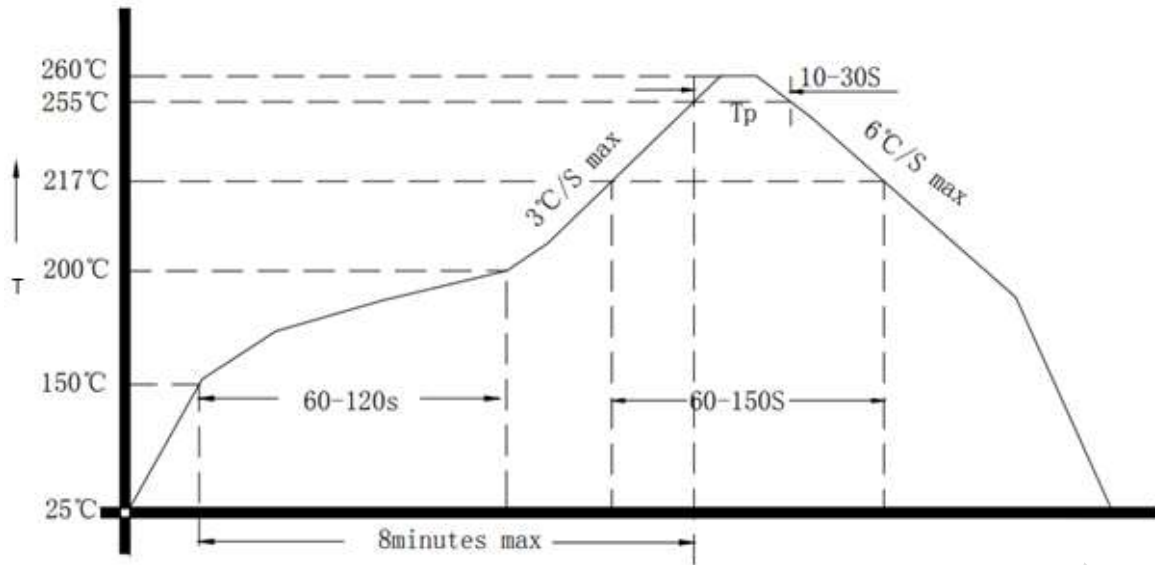


Continuous register read operation:



## 7 Reflow Soldering Curve

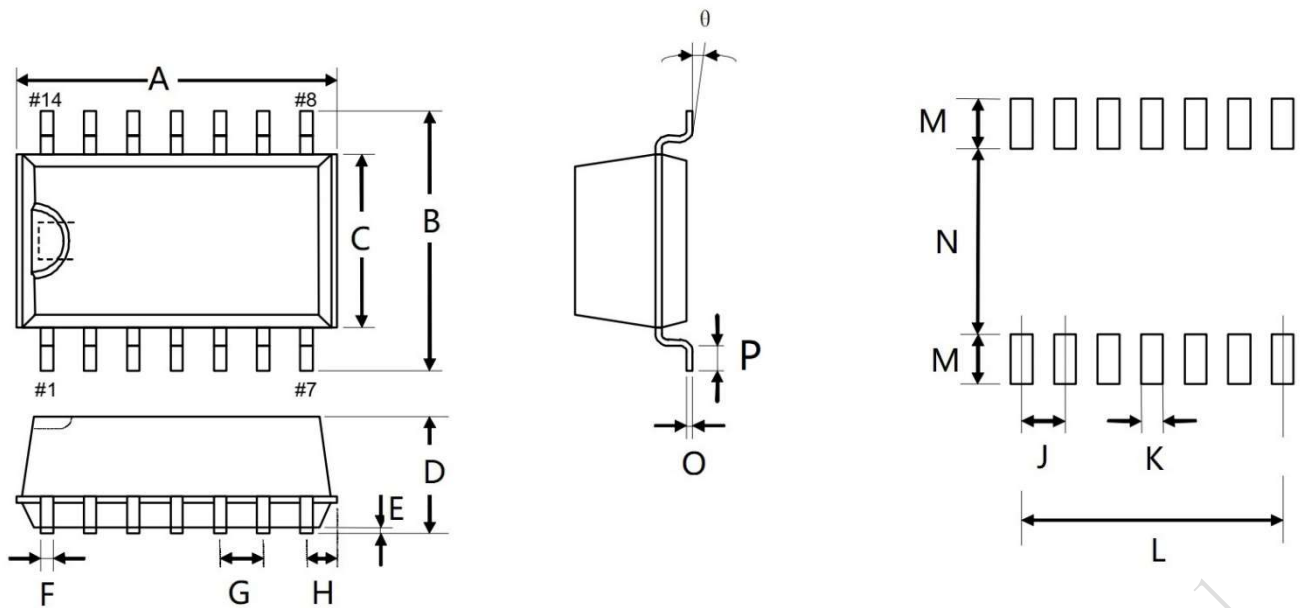
Standard: IPC/JEDEC J-STD-020



Reflow Soldering Curve

Note: It is suggested to solder IC under the condition shown in the curve above. Must pay attention to the temperature and time when manual soldering, if the temperature over +260°C, or you will make the xo performance bad, even damage it.

### 8 Package Dimension



| Dimension | Min.  | Typ.  | Max.  |
|-----------|-------|-------|-------|
| A         | 10.0  | 10.1  | 10.2  |
| B         | 7.2   | 7.4   | 7.6   |
| C         | 4.9   | 5.0   | 5.1   |
| D         | 3.1   | 3.2   | 3.3   |
| E         | 0.055 | --    | 0.205 |
| F         | --    | 0.406 | --    |
| G         | --    | 1.27  | --    |
| H         | --    | 1.2   | --    |
| P         | 0.5   | 0.6   | 0.7   |
| O         | --    | 0.13  | --    |
| θ         | 1°    |       | 8°    |

Unit: mm

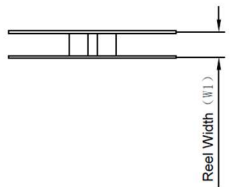
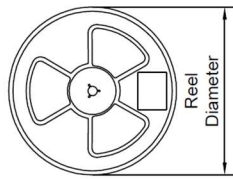
| Dimension | Typ. |
|-----------|------|
| J         | 1.27 |
| K         | 0.7  |
| L         | 7.62 |
| M         | 1.4  |
| N         | 5.4  |

Unit: mm

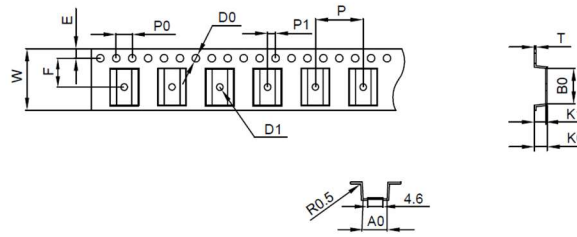
Figure 3. Recommended Soldering Pattern and Dimension

# 9 Packing Information

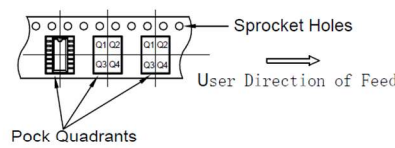
REEL DIMENSIONS



TAPE DIMENSIONS



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



| Device    | Package Type | Pins | SPQ     | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm)  | B0 (mm)   | D0 (mm)       | D1 (mm)       | E (mm)    | F (mm)   | T (mm)    | K0 (mm)  | K1 (mm)  | W (mm)         | P (mm)    | P0 (mm)  | P1 (mm)  | PIN1 Quadrant |
|-----------|--------------|------|---------|--------------------|--------------------|----------|-----------|---------------|---------------|-----------|----------|-----------|----------|----------|----------------|-----------|----------|----------|---------------|
| INS5A4803 | SOP          | 14   | 1500pcs | 330                | 16                 | 8.0 ±0.1 | 10.4 ±0.1 | 1.5 +0.1 -0.0 | 1.5 +0.1 -0.0 | 1.75 ±0.1 | 7.5 ±0.1 | 0.3 ±0.05 | 3.8 ±0.1 | 3.5 ±0.1 | 16.0 +0.3 -0.3 | 12.0 ±0.1 | 4.0 ±0.1 | 2.0 ±0.1 | Q1            |

Figure 4. Reel and tape

## 10 Contact Information

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