I2C Programmable Any-Frequency CMOS Clock Generator

FEATURES

- Generates up to 3 non-integer-related frequencies from 2.5KHz to 250MHz
- I2C user definable configuration
- Exact frequency synthesis at each output (0 ppm error)
- Low output period jitter: <70pS (typ.)
- Configurable spread spectrum selectable at each output
- Operates from a low-cost, fixed frequency crystal: 25 or 27MHz
- Single-ended clock input accepts 2.8 to 40MHz
- Supports static phase offset
- Programmable rise/fall time control
- Glitch-less frequency changes
- Separate voltage supply pins provide level translation:
  - Core VDD: 2.5 or 3.3V
  - Output VDDO: 1.8, 2.5 or 3.3V
- Excellent PSRR eliminates external power supply filtering
- Very low power consumption
- Adjustable output delay
- Package type: MSOP10
- PCIE Gen 1 compatible
- Supports HCSL compatible swing)

APPLICATIONS

- HDTV, DVD/Blue-ray, Set-top box
- Audio/video equipment, gaming
- Printers, scanners, projectors
- Handheld Instrumentation
- Residential gateways
- Networking/Communication
- Servers, Storage
- XO Replacement

GENERAL DESCRIPTIONS

The INS8D5351A-GT is an I2C configurable clock generator that is ideally suited for replacing crystals, crystal oscillators, phase-locked loops (PLLs), and fanout buffers in cost-sensitive applications.

Based on a PLL+ high resolution MultiSynth fractional divider architecture, the INS8D5351A-GT can generate any frequency up to 250MHz on each of its outputs with 0ppm error. The INS8D5351A-GT can generate up to 3 free-running clocks using an internal oscillator for replacing crystals and crystal oscillators.

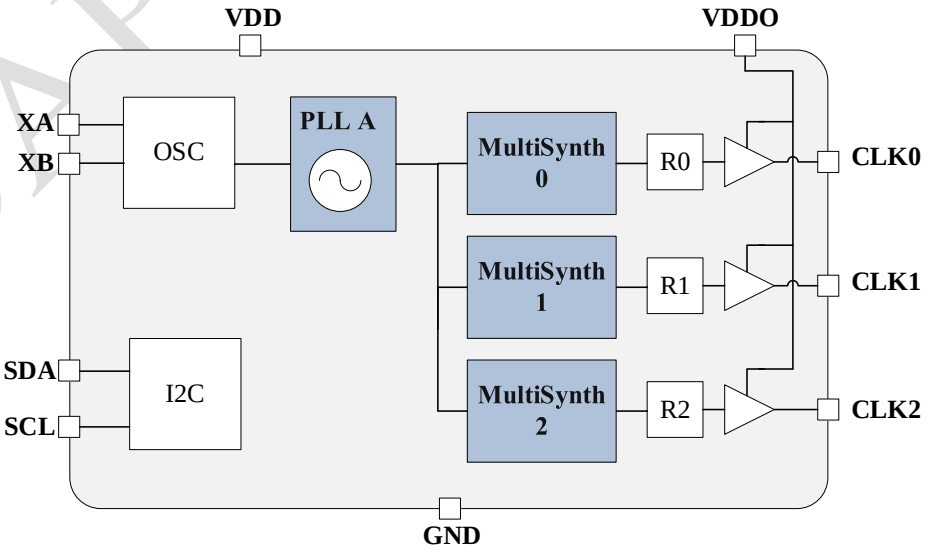

Figure 1. Block Diagram

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1. Pinouts

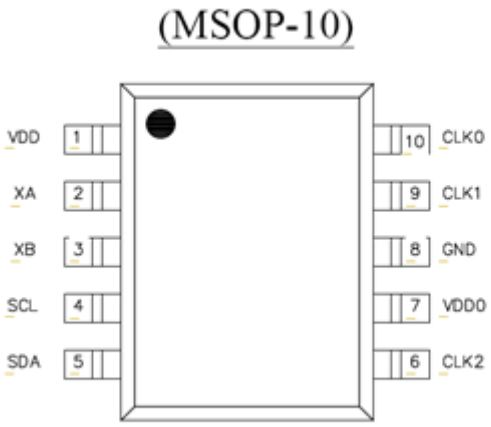


Figure 2. Pinout Diagram (Top view)

Table1. Pin Descriptions

Number	Name	Type	Description
1	VDD	P	Core voltage power supply pin.
2	XA	I	Input pin for external crystal.
3	XB	O	Output pin for external crystal.
4	SCL	I	Serial clock input for the I2C bus. This pin must be pulled up to VDD using a pull-up resistor of at least 1KΩ.
5	SDA	I/O	Serial data input for the I2C bus. This pin must be pulled up to VDD using a pull-up resistor of at least 1KΩ
6	CLK2	O	Output clock 2
7	VDDO	P	Output voltage power supply pin for CLK0, CLK1 and CLK2.
8	GND	P	Ground
9	CLK1	O	Output clock 1.
10	CLK0	O	Output clock 0.

Notes: I = Input, O = Output, P = Power.

2. Electrical Parameter

2.1 Absolute Maximum Ratings

Table2. Absolute Maximum Ratings

Stresses beyond below listed absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Parameter	Symbol	Rating	Unit	Comments
DC Supply Voltage	V_{DD_MAX}	-0.3~3.8	V	VDD, VDDO
Output Voltage	V_{OUT_CLK}	-0.3~VDDO+0.3	V	(CLK0/1/2)
Input Voltage	V_{IN_CLKIN}	-0.3~3.8	V	SCL，SDA
	$V_{IN\_XA/XB}$	-0.3~1.3	V	XA，XB
Junction Temperature	T_J	-55~150	℃	
Soldering Temperature	T_{PK}	260	℃	
Soldering Temperature Time at T_{PK}	T_P	20~40	S	
Thermal Resistance Junction to Ambient of MSOP10	JA	131	℃/W	Still air
ESD		±2000	V	

2.2 Recommended Operating Conditions

Table3. Recommended Operating Conditions

All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25°C unless otherwise noted. VDD and VDDO can be operated at independent voltages. Power supply sequencing for VDD and VDDO requires that VDDO be powered up either before or at the same time as VDD.

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Core Supply Voltage	V_{DD}	3.0	3.3	3.6	V
		2.25	2.5	2.75	V
Output Buffer Voltage	V_{DDO}	1.71	1.8	1.89	V
		2.25	2.5	2.75	V
		3.0	3.3	3.6	V
Operating Temperature	T_A	-40	25	85	℃

2.3 DC CHARACTERISTICS

Table4. Control Signal Characteristics

Test Condition：VDD = 2.5V ± 10%, or 3.3V ± 10%， TA = -40 to 85℃

Parameter	Symbol	Value			Unit	Comments
		Min.	Typ.	Max.		
Core Supply Current	I_{DD}		12	25	mA	Enable 3 outputs
Output Buffer Supply Current (Per Output)	I_{DDO}		2	6	mA	CLK0/1/2 ≤ 100MHz, CL = 5pF

Parameter	Symbol	Value			Unit	Comments
		Min.	Typ.	Max.		
Input Current	I_{IN}			10	uA	SDA, SCL
Output Impedance	Z_O		50		Ω	3.3V VDDO, default high driver

2.4 AC CHARACTERISTICS

Table5. AC Characteristics

Test Condition：VDD = 2.5V ± 10%, or 3.3V ± 10%， TA = -40 to 85℃

Parameter	Symbol	Value			Unit	Comments
		Min.	Typ.	Max.		
Power-up Time	t_{RDY}		2	10	ms	From VDD = VDDMIN to valid output clock, CL = 5pF, fCLKn > 1MHz
Power-up Time, PLL Bypass Mode	t_{BYP}		0.5	1	ms	From VDD = VDDMIN to valid output clock, CL = 5pF, fCLKn > 1MHz
Output Frequency Transition Time	t_{FREQ}			10	us	fCLKn > 1MHz
Output Phase Offset	P_{STEP}		333		ps/step	
INPUT CLOCK CHARACTERISTICS						
Crystal Frequency	f_{XTAL}	10	27	40	MHz	V_{CC}=3.3V, DP_R, DN_L = 1.5V, R_L = 50 Ω
Input Frequency	f_{OSCin}	2.8		40	MHz	XA Single-Ended Input, XB floating
OUTPUT CLOCK CHARACTERISTICS						
Frequency Range(1)	F_{CLK}	0.0025		250	MHz	
Load Capacitance	C_L			15	pF	
Duty Cycle	$t_{W/T}$	45	50	55	%	FCLK≤160MHz, measured at V_{DD}/2
		40	50	60	%	FCLK > 160MHz, measured at V_{DD}/2
Rise/Fall Time	t_r		1	1.5	ns	20%~80%, CL = 5pF, Default high drive strength
	t_f		1	1.5	ns	
Output High Voltage	V_{OH}	V_{DD}-0.6			V	C_L = 5pF
Output Low Voltage	V_{OL}			0.6	V	C_L = 5pF
Period Jitter(2,3)	J_{PER}		70	155	ps	Peak to peak, 3 outputs running

Parameter	Symbol	Value			Unit	Comments
		Min.	Typ.	Max.		
Cycle-to-Cycle Jitter(2,3)	J_{CC}		70	150	ps	Peak to peak, 3 outputs running
CRYSTAL REQUIREMENTS(4)						
Crystal Frequency	f_{XTAL}	10	27	40	MHz	
Load Capacitance(4)	C_L	6		12	pF	
Equivalent Series Resistance	ESR			150	Ω	
Crystal Max Drive Level	d_L	100			uW	

* Note:

(1) Only two unique frequencies above 112.5MHz can be simultaneously output.

(2) Measured over 10K cycles. Jitter is only specified at the default high drive strength (50Ω output impedance).

(3) Jitter is highly dependent on device frequency configuration. Specifications represent a "worst case, real world" frequency plan; actual performance may be substantially better. Three-output 10 MSOP package measured with clock outputs of 74.25, 24.576 and 48MHz

4) Crystals which require load capacitances of 6, 8, or 10pF should use the device's internal load capacitance for optimum performance. See register 183 bits 7:6. A crystal with a 12pF load capacitance requirement should use a combination of the internal 10pF load capacitance in addition to external 2pF load capacitance (e.g., by using 4pF capacitors on XA and XB).

2.5 I²C SPECIFICATION

Table6. I²C Characteristics

Parameter	Symbol	Standard mode 100Ksps		Fast mode 400Ksps		Unit	Test Condition
		Min.	Max.	Min.	Max.		
Low Level Input Voltage	V_{ILI2C}	-0.3	0.3x V_{DDI2}	-0.3	0.3x V_{DDI2C}	V	
High Level Input Voltage	V_{IHI2C}	0.7x V_{DDI2C}	3.6	0.7x V_{DDI2C}	3.6	V	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	--	--	0.1	--	V	
Low Level Output Voltage (open drain or open collector) at 3mA sink current	V_{OLI2C}[1]	0	0.4	0	0.4	V	V_{DDI2C}[1]=2.5/ 3.3V
Input Current	I_{II2C}	-10	10	-10	10	μA	
Capacitance for Each I/O Pin	C_{II2C}	--	4	--	4	pF	V_{IN} = -0.1 to V_{DDI2C}
I²C Bus Timeout	T_{TO}	25	35	25	35	mS	Timeout Enabled

1) Note：Only I2C pull-up voltage (VDDI2C) of 2.25 to 3.6V are supported.

3. FUNCTIONAL DESCRIPTION

The INS8D5351A-GT is a versatile I2C programmable clock generator that is ideally suited for replacing crystals, crystal oscillators. A block diagram showing the general architecture of the INS8D5351A-GT is shown in Figure 3. The device consists of an input stage, two synthesis stages, and an output stage.

The input stage accepts an external crystal (XTAL) or a clock input (CLKIN). The first stage of synthesis is an integer-N PLL A which multiplies the input frequencies to a high-frequency intermediate clock A. The second stage uses high resolution MultiSynth fractional dividers to generate the desired output frequencies with low jitter. Additional integer division is provided at the output stage for generating output frequencies as low as 2.5 kHz.

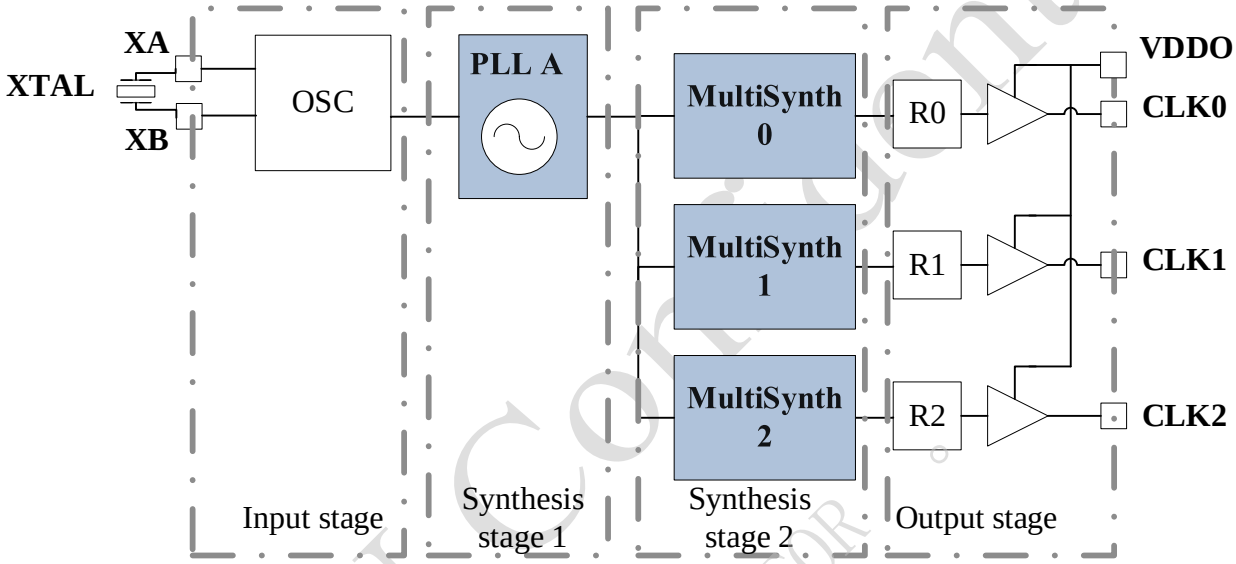


Figure 3. Block Diagram

3.1 Input Stage

Crystal Inputs (XA, XB)

The INS8D5351A-GT uses a fixed-frequency standard AT-cut crystal as a reference to the internal oscillator. The output of the oscillator can be used to provide a free-running reference to the PLL A for generating asynchronous clocks. The output frequency of the oscillator will operate at the crystal frequency, from 10MHz to 40MHz. Internal load capacitors are provided to eliminate the need for external components when connecting a crystal to the INS8D5351A-GT. The total internal XTAL load capacitance (C_L) can be selected to be 0, 6, 8, or 10pF. Crystals with alternate load capacitance requirements are supported using additional external load capacitance ≤ 2pF (e.g., by using ≤ 4pF capacitors on XA and XB) as shown in Figure 4.

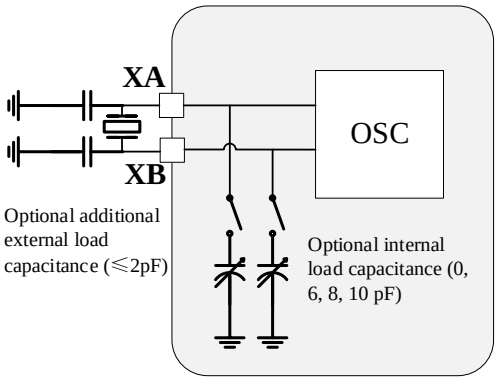


Figure 4. External XTAL with Optional Load Capacitors

External Clock Input

The INS8D5351A-GT can be driven with a clock signal through the XA input pin. This is especially useful when in need of generating clock outputs in two synchronization domains. With the INS8D5351A-GT, one reference clock can be provided at XA as shown in figure 5. The external clock input from 10 to 40MHz is used as a clock reference for the PLL A when generating synchronous clock outputs.

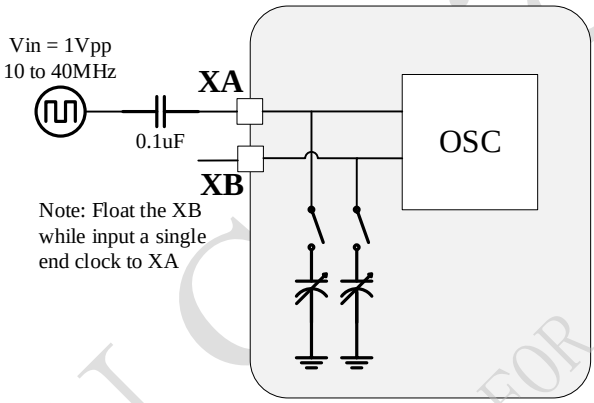


Figure 5. Single end Clock input

3.2 Synthesis Stages

The INS8D5351A-GT uses two stages of synthesis to generate its final output clocks. The stage 1 uses PLL A to multiply the lower frequency input reference to a high-frequency intermediate clock. The stage 2 uses high resolution MultiSynth fractional dividers to generate the required output frequencies. Only two unique frequencies above 112.5MHz can be simultaneously output.

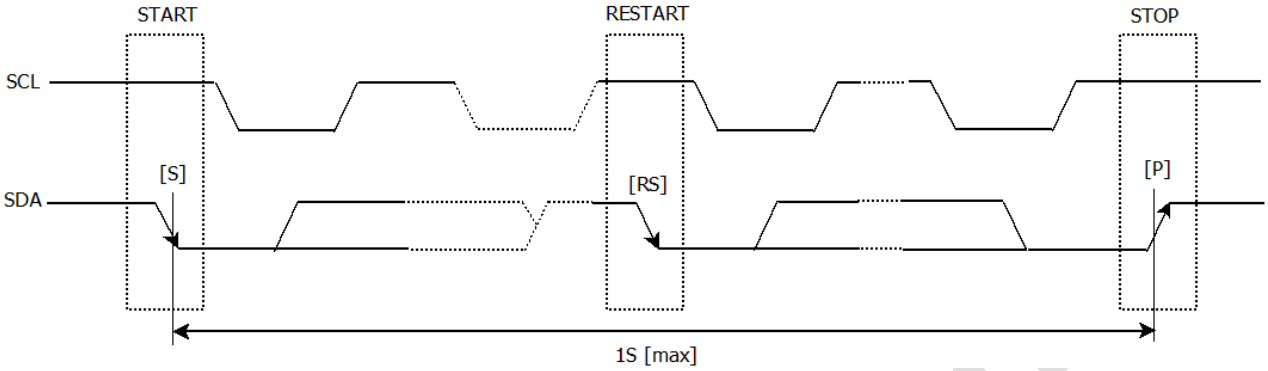
3.3 Output Stage

An additional level of division (R) is available at the output stage for generating clocks as low as 2.5 kHz. All output drivers generate CMOS level outputs with separate output voltage supply pins (VDDO) allowing a different voltage signal level (1.8, 2.5, or 3.3 V).

4. CONFIGURING THE INS8D5351A-GT

The INS8D5351A-GT is a highly flexible clock generator which is entirely configurable through its I2C interface.

4.1 I2C Bus Interface



The I2C interface operates in slave mode with 7-bit addressing and can operate in Standard-Mode (100 kbps) or Fast-Mode (400 kbps) and supports burst data transfer with auto address increments.

The I2C bus consists of a bidirectional serial data line (SDA) and a serial clock input (SCL) as shown in Figure 6. Both the SDA and SCL pins must be connected to the VDD supply via an external pull-up as recommended by the I2C specification.

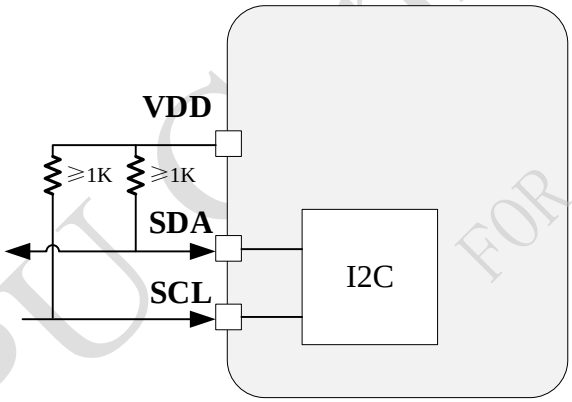


Figure 6. I2C Interface

4.1.1 Slave Address

The 7-bit device (slave) address of the INS8D5351A-GT consist of a 6-bit fixed address plus a user selectable LSB bit as shown in Table 7. The LSB bit is selectable as 0 or 1 using the optional A0 pin which is useful for applications that require more than one INS8D5351A-GT on a single I2C bus.

Table7. I²C Bus Slave Address

ADDR	Transfer data	Slave address							R/W
		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Low Level	61h (Read)	1	1	0	0	0	0	0	1 (Read)
	C0h (Write)	1	1	0	0	0	0	0	0 (Write)
	C3h (Read)	1	1	0	0	0	0	1	1 (Read)

ADDR	Transfer data	Slave address							R/W
		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
High	C2h (Write)	1	1	0	0	0	0	1	0 (Write)

INS8D5351A-GT I^{2}C bus Slave Address is [1100 00*].

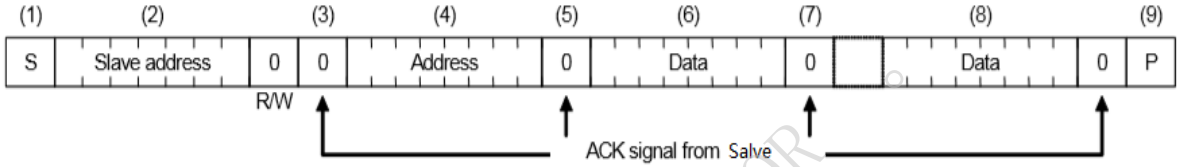
4.1.2 I2C bus protocol

It is assumed CPU is master and INS8D5351A-GT is slave in this section.

Write process

I^{2}C bus includes an address auto-increment function, once the initial address has been specified, the INS8D5351A-GT increments (+1) the address automatically after each data is sent, then to write next data.

(1) CPU sends start condition[S]
(2) CPU sends INS8D5351A-GT 's slave address with R/W bit to be set to write mode
(3) CPU verifies ACK signal from INS8D5351A-GT
(4) CPU sends write register address to INS8D5351A-GT
(5) CPU verifies ACK signal from INS8D5351A-GT
(6) CPU sends write data to the address specified at step (4)
(7) CPU verifies ACK signal from INS8D5351A-GT
(8) Repeat (6) (7) if multiple bytes need to be written, address will be incremented automatically
(9) CPU ends stop condition[P]

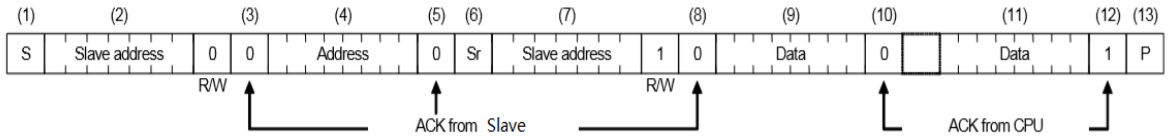


Read process

There are two cases for read process.

Case 1: Setting the register address for reading from INS8D5351A-GT

(1) CPU sends start condition[S]
(2) CPU sends INS8D5351A-GT 's slave address with R/W bit to be set to write mode
(3) CPU verifies ACK signal from INS8D5351A-GT
(4) CPU sends register address for reading from INS8D5351A-GT
(5) CPU verifies ACK signal from INS8D5351A-GT
(6) CPU sends RESTART condition [Sr]
(7) CPU sends INS8D5351A-GT 's slave address with R/W bit to be set to read mode
(8) CPU verifies ACK signal from INS8D5351A-GT
(9) CPU reads data from the specified address in step (4)
(10)CPU sends ACK signal to INS8D5351A-GT
(11)Repeat (9) (10) if multiple bytes need to be read, address will be incremented automatically
(12)CPU sends ACK signal for "1" to INS8D5351A-GT
(13)CPU sends stop condition[P]



Case 2: Writing the slave address to be read with read mode directly and without register address setting.

(1) CPU sends START condition [S]

(2) CPU sends INS8D5351A-GT 's slave address with R/W bit to be set to read mode

(3) CPU verifies ACK signal from INS8D5351A-GT

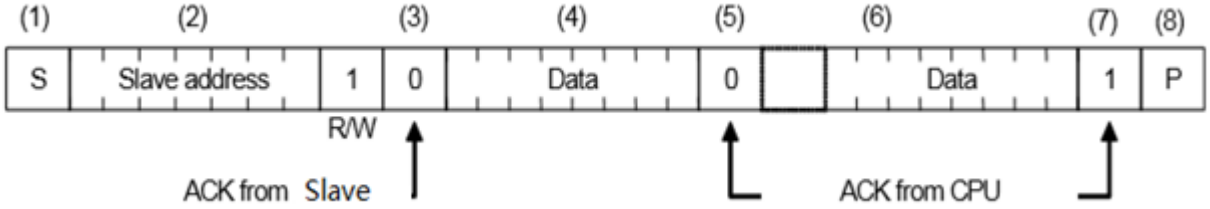
(4) CPU reads data from the latest register address which is updated by the last write data process or read data process

(5) CPU sends ACK signal to INS8D5351A-GT

(6) Repeat (9) (10) if multiple bytes need to be read, address will be incremented automatically

(7) CPU sends ACK signal for "1" to INS8D5351A-GT

(8) CPU sends stop condition[P]



4.2 Write a Custom Configuration to RAM

Many of the functions and features of the INS8D5351A-GT are controlled by reading and writing to the RAM space using the I2C interface. The following is a list of the common features that are controllable through the I2C interface.

Read Status Indicators:

- Crystal Reference Loss of signal, LOS_XTAL, reg0[3]
- PLL A and/or MultiSynth Loss of lock, LOL_M or LOL_S, reg0[6:5]

■ Configuration of multiplication and divider values for the PLLs, dividers

■ Set output clock options

- Enable/disable for each clock output
- Invert/non-invert for each clock output
- Output divider values (2n, n=1...7)
- Output state when disabled (stop Hi, stop Low, Hi-Z)
- Output phase offset

INS8D5351A-GT can be programmed via I2C by following the steps shown in Figure 7. Refer to "Appendix-1:

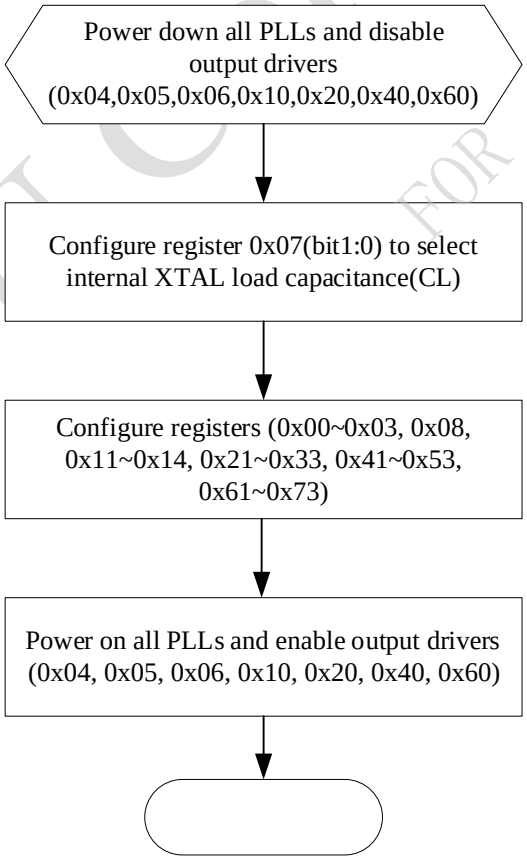


Figure 7. I2C Programming procedure

5. TYPICAL APPLICATION

5.1 INS8D5351A-GT replaces Multiple Clocks and XOs

The INS8D5351A-GT is a user-definable custom clock generator that is ideally suited for replacing crystals and crystal oscillators in cost-sensitive applications. An example application is shown in figure 8.

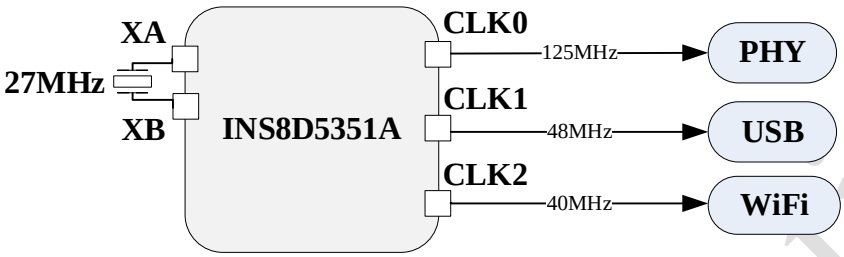


Figure 8. Using INS8D5351A-GT to replace multiple crystals, crystal oscillators

5.2 HCSL Compatible Outputs

The INS8D5351A-GT can be configured to support HCSL compatible swing when the VDDO of the output power supply is set to 2.5 V.

The circuit in the figure 9 below must be applied to each of the two clocks used, and one of the clocks in the pair must also be inverted to generate a differential pair. See register setting CLKx_INV.

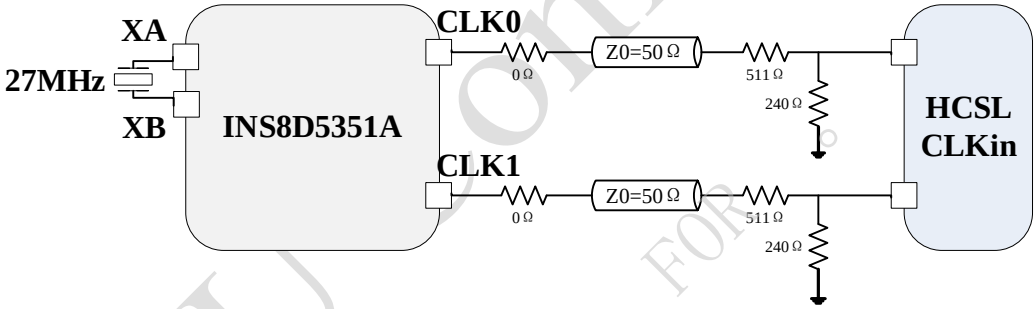


Figure 9. INS8D5351A-GT Output is HCSL compatible

6. DESIGN CONSIDERATIONS

The INS8D5351A-GT is a self-contained clock generator that requires very few external components. The following general guidelines are recommended to ensure optimum performance.

6.1 Power Supply Decoupling/Filtering

The INS8D5351A-GT has built-in power supply filtering circuitry and extensive internal Low Drop Out (LDO) voltage regulators to help minimize the number of external bypass components. All that is recommended is one 0.1 to 1.0 µF decoupling capacitor per power supply pin. This capacitor should be mounted as close to the VDD and VDDO pins as possible without using vias.

6.2 Power Supply Sequence

The VDD and VDDO power supply pins have been separated to allow flexibility in output signal levels. Power supply sequencing for VDD and VDDO requires that all VDDO be powered up either before or at the same time as VDD.

6.3 External Crystal

The external crystal should be mounted as close to the pins as possible using short PCB traces. The XA and XB traces should be kept away from other high-speed signal traces.

6.4 External Crystal Load Capacitors

The INS8D5351A-GT provides the option of using internal and external crystal load capacitors. If internal load capacitance is insufficient, capacitors of value less than 2pF may be used to increased equivalent load capacitance. If external load capacitors are used, they should be placed as close to the XA/XB pads as possible.

6.5 Unused Pins

Unused XB pins should be left floating. Unused output pins (CLK0~CLK2) should be left floating.

6.6 Trace Characteristics

The INS8D5351A-GT features various output current drive strengths. It is recommended to configure the trace characteristics as shown in figure 10 when the default high drive strength is used.

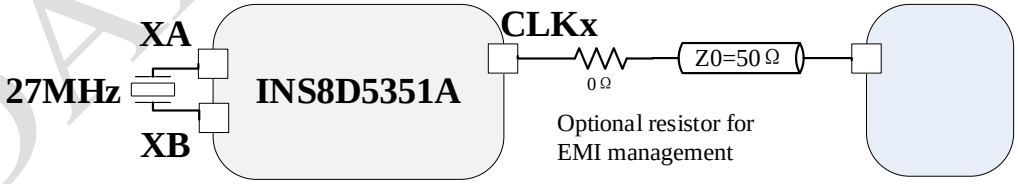
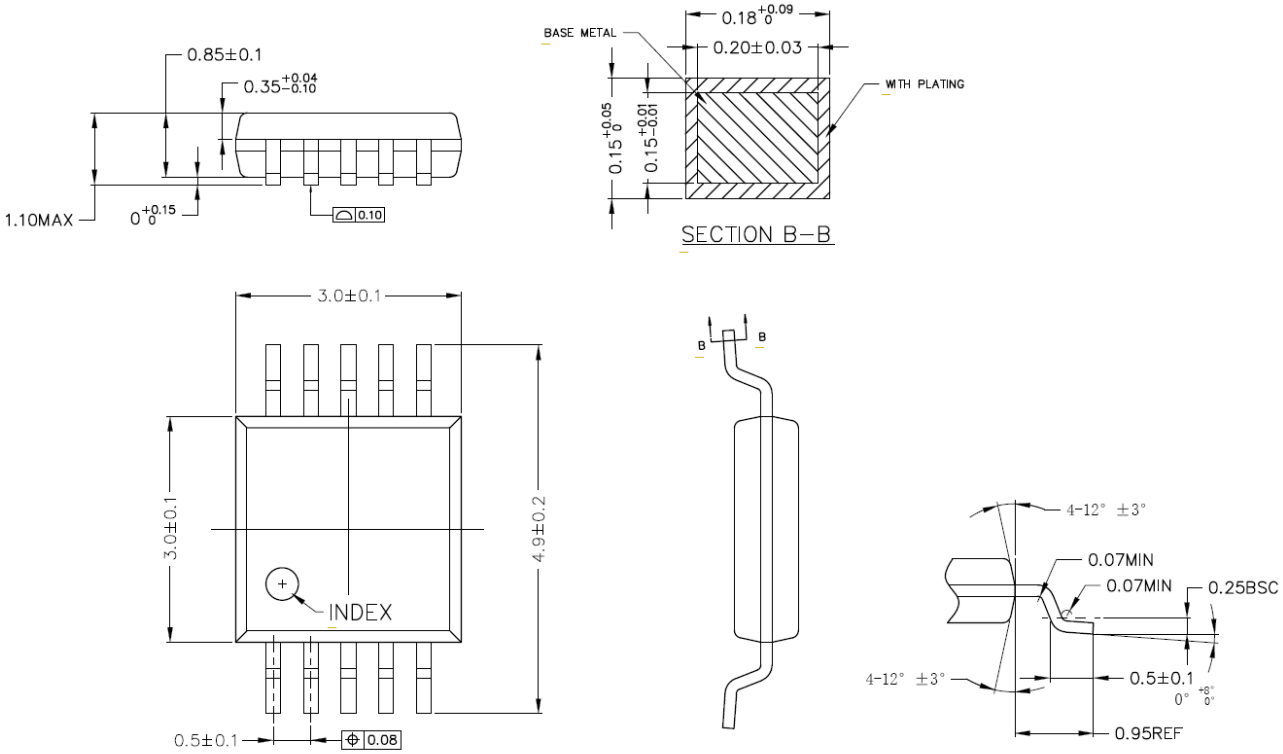


Figure 10. Recommended trace characteristics with default drive strength setting

7. Mechanical Structure (mm)

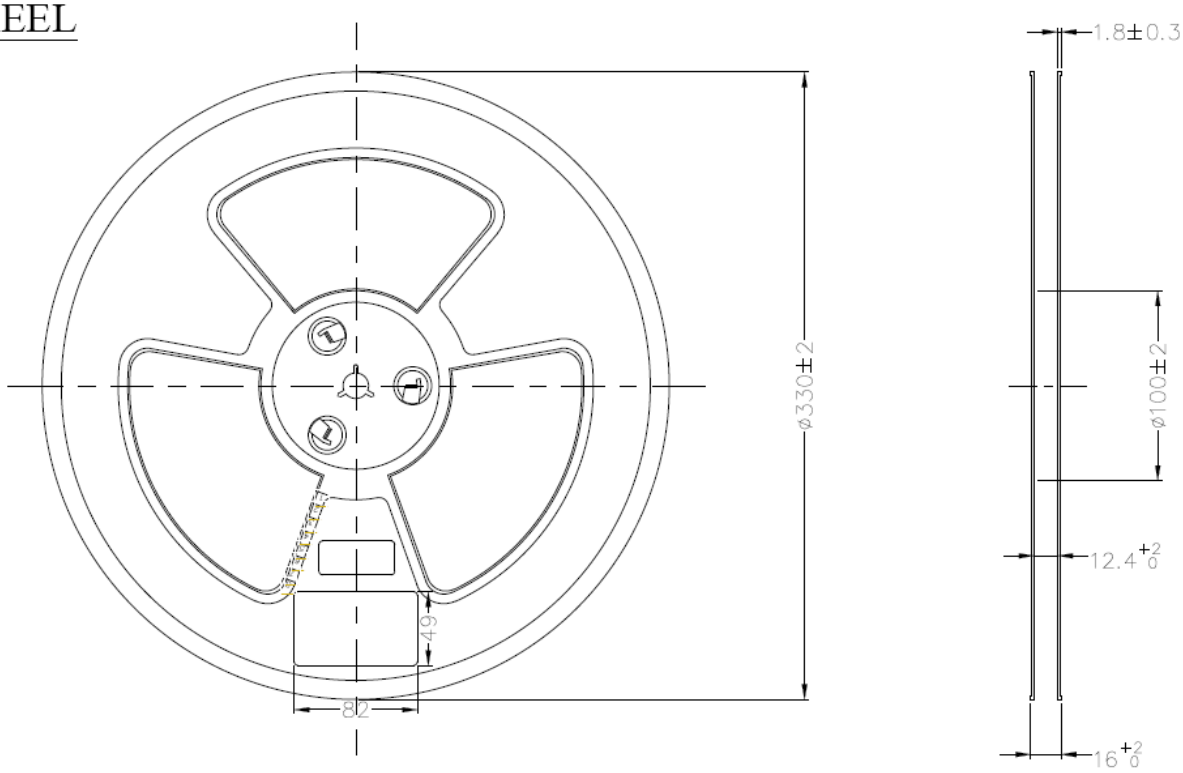


NOTES: 1. ALL DIMENSIONS IN LILLIMETER REFER TO JEDEC STANDARD MO−187 BA
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. INDEX ø0.60±0.10 WITH 0.05MAX DEPTH.

Figure 11. 10-Pin MSOP Package Outline Diagram

TAPE AND REEL INFORMATION(MSOP10)

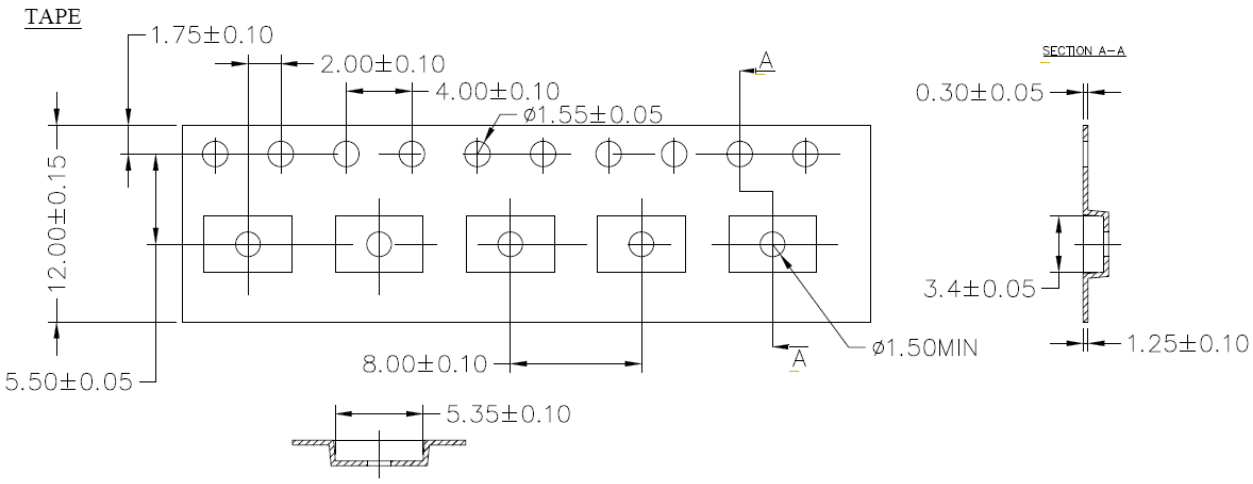
REEL



Notes:

1. Material: Polystyrene
2. Flaneness: ≤ 3 mm
3. Unit: mm
4. Surface Resistance: 10^5-10^11Ω
5. Unmarked tolerance: ±0.25

TAPE



Technical Requirements:

1. 10 sprocket hole pitch cumulative tolerance ±0.2mm
2. Carrier cabber is within 1mm per 250mm
3. All dimensions meet EIA-481-D requirements

Figure 12. Tape and Reel information (MSOP-10)

Appendix-1

Refer to "AN5351-1: Manually Generating an INS8D5351A-GT Register Map" for a detailed description of INS8D5351A-GT registers.