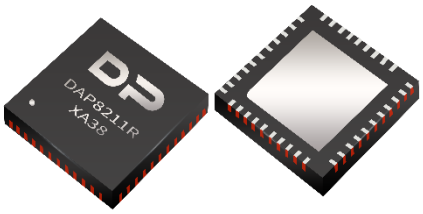
DAP8211R(I) —Gigabit Ethernet PHY

Overview



The DAP8211R(I) device is a robust, low power, single port Gigabit Ethernet and fully featured Physical Layer transceiver which is compliant with IEEE802.3 10BASE-Te, IEEE802.3u 100BASE-TX and IEEE802.3ab 1000BASE-T Ethernet protocols.

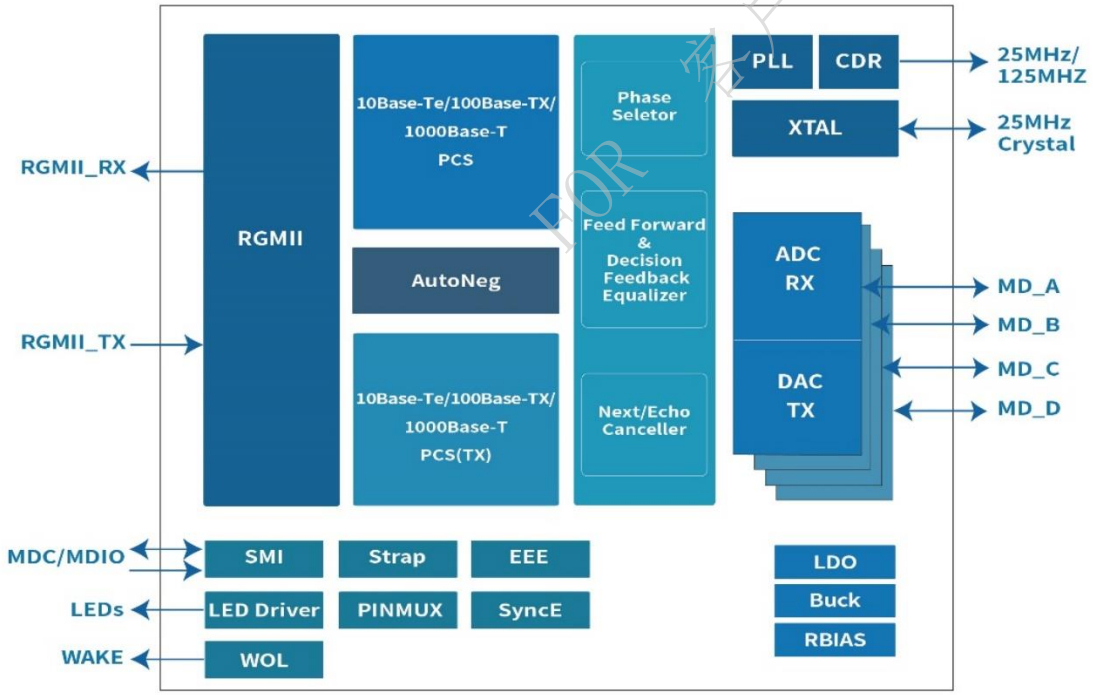
This device interfaces directly to the MAC layer through RGMII (Reduced GMII). It supports RGMII to Copper.

The DAP8211R(I) is designed for easy implementation of 10/100/1000 Mbps Ethernet LANs. The MDI ports interfaces directly to twisted pair media through the external transformer.

Additionally, the DAP8211R(I) provides precision clock synchronization, including a synchronous Ethernet clock output.
The DAP8211R(I) supports single 3.3V power supply and configurable RGMII I/O voltage supporting 3.3V, 2.5V and 1.8V.

Designed for low power, EEE and Wake-on-LAN can be used to lower system power consumption.

Block Diagram



Key Features

- RGMII MAC interface
- 1000BASE-T IEEE 802.3ab /100BASE-TX IEEE 802.3u/10BASE-Te IEEE 802.3 Compliant
- EEE(IEEE 802.3az-2010)
- Supports SyncE
- WoL (Wake-on-LAN)
- Sleep Mode
- Crossover Detection & Auto-Correction
- Supports Parallel Detection
- Supports Base Line Wander Correction
- Supports Interrupt function
- Automatic polarity correction
- Integrate Linear/Buck Switching Regulator
- 120 meters at 1000Mbps over CAT.5E cable
- Configurable I/O voltage (3.3 V, 2.5 V, 1.8 V) signaling for RGMII
- 3.3V single power supply
- 3 LEDs for Network Status
- 25MHz external crystal/oscillator
- Output 25MHz/125MHz clock for MAC
- Operation Temperature Range: 0℃ ~ +70℃
  -40℃ ~ +85℃
- Package: QFN 40-pin (5mm x 5mm)

Part Number	RGMII to Copper	WoL	1000Base-T	100Base-TX	10Base-Te	EEE	SyncE	Integrated Buck	Temp.	Package
DAP8211R	●	●	●	●	●	●	●	●	0℃ ~ +70℃	QFN40
DAP8211RI	●	●	●	●	●	●	●	●	-40℃ ~ +85℃	QFN40

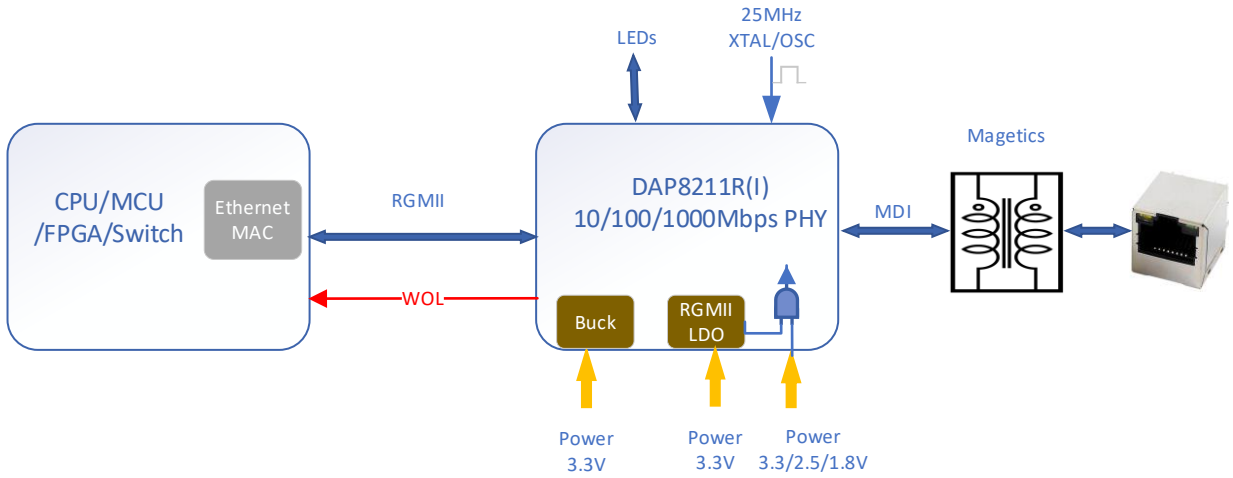
●: Support

x: Not Support

Applications

- Enterprise & SOHO
- Wireless Router
- Industrial controls and automation
- LED Display
- Motor drives
- Industrial factory automation
- Field Bus Support
- Industrial embedded computing
- Wired and wireless communications infrastructure
- Test and measurement
- Consumer electronics

Applications Diagram



Revision History

Revision	Change Contents	Prepared by	Revised Date
V1.0	First Issued		2022.2.14
V1.1	Update the dimensions		2022.2.22
V1.2	1. Add DAP8211RI 2. Correct the parameters in table 3, 4 and 5. 3. Correct the RGMII I/O Voltage selection table in chapter 3.3.9. 4. LED_2_FORCE_MODE 11: force LED Blink at Blink Mode2 10: force LED Blink at Blink Mode1 5. Add chapter 2.5.1 Power Sequence		2022.5.22

Index

1 Pin Definition

1.1 QFN40 Pin Assignments

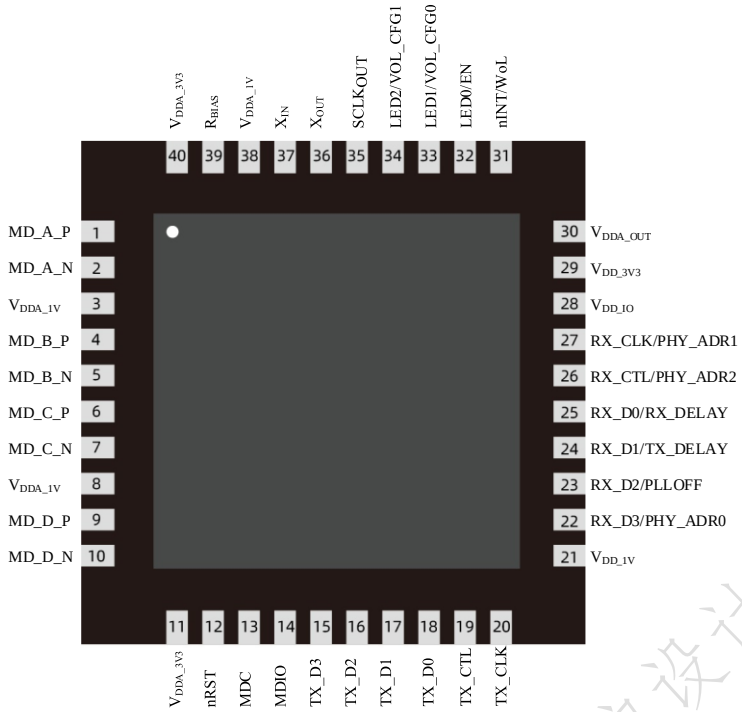


Figure 1 Package 40-Pin (Top View)

I：Input Signal

O：Output Signal

PWR：Power Supply

GND: Ground

EPAD: Exposed thermal PAD

Table1. Pin Definition

Pin Number	Pin Name	I/O	Description
POWER AND GROUND			
11, 40	V_{DDA_3V3}	PWR	3.3V Analog Supply. A 1μF and 0.1μF capacitor are required to GND for each pin.
3, 8, 38	V_{DDA_1V}	PWR	1.1V/1.2V Analog Supply. A 1μF and 0.1μF capacitor are required to GND for each pin.
21	V_{DD_1V}	PWR	Digital Core Power. 1.1V/1.2V
28	V_{DD_IO}	PWR	Digital I/O power input for RGMII I/O, MDC/MDIO

			If disabled the internal LDO, `V_{DD_IO} should be supplied by the external power supply. This pin need a bulk capacitor and a decoupling capacitor .
29	V_{DD_3V3}	PWR	3.3V Digital power input for others IO excluding RGMII, MDIO
30	V_{DDA_OUT}	PWR_O	For DAP8211R(I), Regulator power output 1.1V. A 2.2μH inductor is required.
41	EPAD	GND	Exposed PAD Ground
CLOCK			
35	$SCLK_{OUT}$	O	25/125MHz Clock Output. • Reference Clock Generated from Internal PLL • Recovered clock from UTP for SyncE. • Synchronized with the 25 MHz reference clock
36	X_{OUT}	O	Crystal Output: 25-MHz crystal output If external oscillator provides clock to X_{IN} , the X_{OUT} must be floating. If external oscillator provides clock to X_{OUT} , the X_{IN} must be GND.
37	X_{IN}	I	Crystal Input: 25-MHz crystal input If external oscillator provides clock to X_{IN} , the X_{OUT} must be floating. If external oscillator provides clock to X_{OUT} , the X_{IN} must be GND.
MEDIA DEPENDENT INTERFACE			
1	MD_A_P	I/O	Media Dependent Interface, Differential Transmit and Receive 1st Signals
2	MD_A_N	I/O	Media Dependent Interface, Differential Transmit and Receive 1st Signals
4	MD_B_P	I/O	Media Dependent Interface, Differential Transmit and Receive 2nd Signals
5	MD_B_N	I/O	Media Dependent Interface, Differential Transmit and Receive 2nd Signals
6	MD_C_P	I/O	Media Dependent Interface, Differential Transmit and Receive 3rd Signals
7	MD_C_N	I/O	Media Dependent Interface, Differential Transmit and Receive 3rd Signals
9	MD_D_P	I/O	Media Dependent Interface, Differential Transmit and Receive 4th Signals
10	MD_D_N	I/O	Media Dependent Interface, Differential Transmit and Receive 4th Signals
MANAGEMENT INTERFACE			
12	nRST	I	Reset: The active low RESET initializes or reinitializes the PHY. All internal registers reinitialize to the default state after reset. Note: The reset signal must be held low at least 10 ms, suggest to be pulled up.
13	MDC	I/PD	Management Data Clock
14	MDIO	I/O/PU	Input/Output of Management Data.
31	nINT/nPME	O/OD	This pin is shared by two functions, keep this pin floating if either of the functions is not used. 1. Interrupt (supports 3.3V pull up). Set low if the specified events happened; active low.

			2. Power Management Event (supports 3.3V pull up). Set low if received a magic packet or Wake-Up frame, or wake up event; active low.
RGMII Interface			
15	TX_D3	I/PD	RGMII Transmit Data. Data is transmitted from MAC to PHY
16	TX_D2	I/PD	RGMII Transmit Data. Data is transmitted from MAC to PHY
17	TX_D1	I/PD	RGMII Transmit Data. Data is transmitted from MAC to PHY
18	TX_D0	I/PD	RGMII Transmit Data. Data is transmitted from MAC to PHY
19	TX_CTL	I/PD	RGMII Transmit Control Signal
20	TX_CLK	I/PD	RGMII Transmit Reference Clock, 125Mhz, 25MHz, or 2.5MHz
22	RX_D3/PHY_ADR0	O/LI/PD	RGMII Receiver Data. Data is transmitted from PHY to MAC. PHY Address[0]
23	RX_D2/PLLOFF	O/LI/PD	RGMII Receiver Data. Data is transmitted from PHY to MAC. In sleep mode, PLL off configuration when pulled down.
24	RX_D1/TX_DELAY	O/LI/PD	RGMII Receiver Data. Data is transmitted from PHY to MAC. RGMII transmit timing delay control. Pull up to add 2ns delay to TXC for TXD latching for 125MHz TX_CLK.
25	RX_D0/RX_DELAY	O/LI/PU	RGMII Receiver Data. Data is transmitted from PHY to MAC. RGMII receive timing delay control. Pull-up to add: 2ns delay on RX_CLK when RX_CLK is 125MHz Or 8ns delay on RX_CLK when RX_CLK is 25MHz/2.5MHz, which shall be used to latch RXD.
26	RX_CTL/PHY_ADR2	O/LI/PD	RGMII Receiver Control signal. PHY Address[2]
27	RX_CLK/PHY_ADR1	O/LI/PD	RGMII Receiver Reference Clock. 125Mhz, 25MHz, or 2.5MHz PHY Address [1]
LED			
32	LED0/EN_{LDO}	O/LI/PU	LED0 Light = Link up at 10Mbps Blinking = Transiting or Receiving Enable LDO
33	LED1/VOL_CFG0	O/LI/PU	LED1 Light = Link up at 100Mbps Blinking = Transiting or Receiving RGMII Voltage Configure[0]
34	LED2/VOL_CFG1	O/LI/PD	LED2 Light = Link up at 1000Mbps Blinking = Transiting or Receiving

			RGMII Voltage Configure[1]
Others			
39	RBIAS	O	Bias Resistor Connection. External 2.49 kΩ 1% resistor connection to GND.

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

Table2. **Absolute Maximum Ratings**

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage	V_{DD_3V3} V_{DDA_3V3}	-0.5		3.63	V	
	V_{DD_1V} V_{DDA_1V}	-0.3		1.32	V	
	V_{DD_IO}	-0.5		3.63	V	
Storage temperature	T_{STG}			150	℃	
Operating Junction Temperature	T_{Jun}	-40		125	℃	
Lead Soldering Temperature				260	℃	

2.2 Recommended Operating Conditions

Table3. **Recommended Operating Conditions**

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
3.3V Power Supply Voltage	V_{DD_3V3} V_{DDA_3V3}	2.97	3.3	3.63	V	
1.0V Power Supply Voltage	V_{DD_1V}	1.045	1.10	1.32	V	
	V_{DDA_1V}	1.045	1.10	1.32	V	
3.3V Power Supply Voltage	V_{DD_IO}	2.97	3.3	3.63	V	
2.5V Power Supply Voltage	V_{DD_IO}	2.25	2.5	2.75	V	
1.8V Power Supply Voltage	V_{DD_IO}	1.62	1.8	1.98	V	
Max. Junction	T_{JUNC}	0		125	℃	

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Temperature						
Operation temperature	T_{OPR}	0	25	70	℃	DAP8211R
		-40	25	85	℃	DAP8211RI
Thermal resistance - junction to ambient	θ_{JA}		32		℃/W	JEDEC with no air flow TA=25°C
Thermal resistance - junction to board	θ_{JB}		12		℃/W	JEDEC with no air flow
Thermal resistance - junction to top case	θ_{JC-Top}		27		℃/W	JEDEC with no air flow

2.3 DC Characteristics

Table4. **DC Characteristics**

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
High-level input voltage	V_{IH1}	2.0			V	V_{DDIO}=3.3V
	V_{IH2}	1.7			V	V_{DDIO}=2.5V
	V_{IH3}	1.2			V	V_{DDIO}=1.8V
Low-level input voltage	V_{IL1}			0.8	V	V_{DDIO}=3.3V
	V_{IL2}			0.7	V	V_{DDIO}=2.5V
	V_{IL3}			0.5	V	V_{DDIO}=1.8V
High-level output voltage	V_{OH1}	2.4		3.63	V	V_{DDIO}=3.3V, I_{OH}=-20mA
	V_{OH2}	2.0		2.8		V_{DDIO}=2.5V, I_{OH}=-20mA
	V_{OH3}	1.62		2.1		V_{DDIO}=1.8V, I_{OH}=-10mA
Low-level output voltage	V_{OL1}	-0.3		0.4	V	V_{DDIO}=3.3V, I_{OH}=20mA
	V_{OL2}	-0.3		0.4		V_{DDIO}=2.5V, I_{OH}=20mA
	V_{OL3}	-0.3		0.4		V_{DDIO}=1.8V, I_{OH}=10mA

2.4 Clock Characteristics

Table5. **Clock Characteristics**

Parameter	Symbol	Value			Unit	Comments
		Min.	Typ.	Max.		
Crystal Requirement						
Frequency	$F_{XIN/XOUT}$		25		MHz	
Tolerance	Δ f/f	-50		50	ppm	
ESR	ESR			50	Ω	
Drive Level	DL			0.5	mW	
Oscillator Characteristics						
Frequency	F_{XIN}		25		MHz	**Comments**
Input High Voltage	V_{XINH}	1.4		V_{DDA_3V3}+0.3	V	
Input Low Voltage	V_{XINL}			0.7	V	
DutyCycle	Duty_Cycle	40		60	%	
Tolerance	Δ f/f	-50		50	ppm	
Rise/Fall Time				10	ns	10%~90%

2.5 Timing Characteristics

2.5.1 Power Sequence

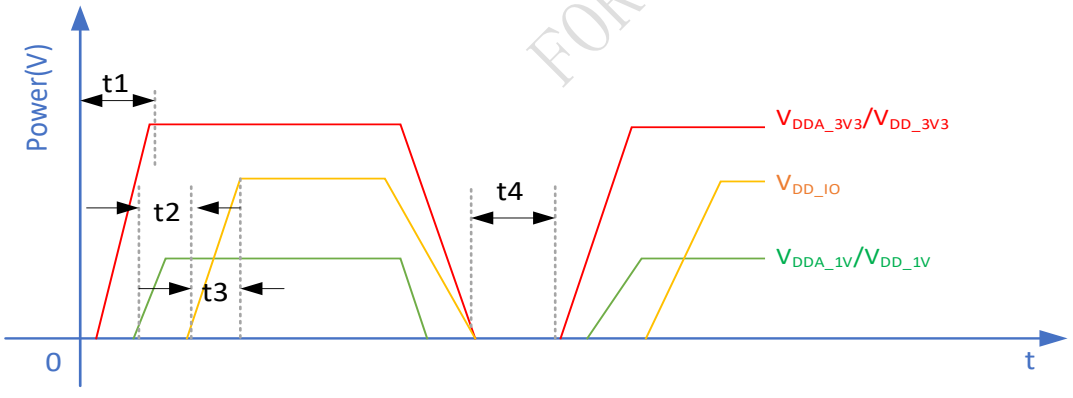


Figure 1. Power Sequence

Table6. Power Sequence

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
V_{DD_3V3}/V_{DDA_3V3} Rising Time*	t1	0.5			ms
Core Logic Ready Time	t2	2.5			ms
Internal LDO Ready Time	t3	100			ms
Power Down Duration	t4	100			ms

*DAP8211R(I) doesn't support fast power rising.

2.5.2Reset Timing

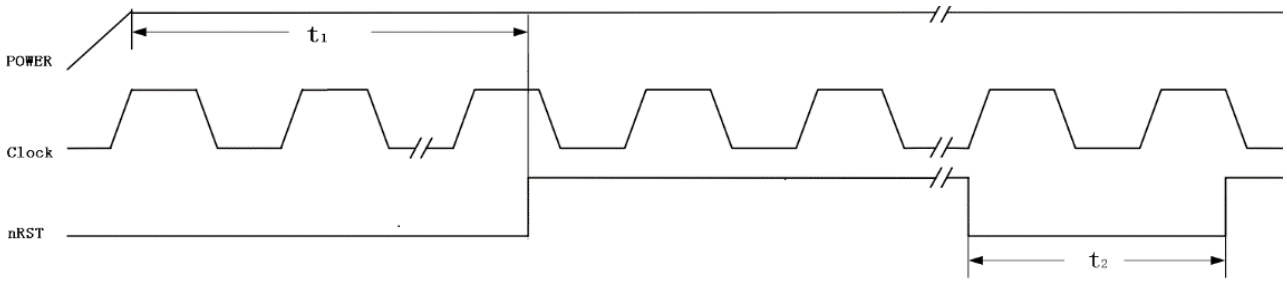


Figure 2. Reset Timing

Table7. Reset Timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Reset de-assert time after power on	t1	10			ms
Minimum reset pulse during normal operation	t_2	10			ms

2.5.3 RGMII Interface Timing

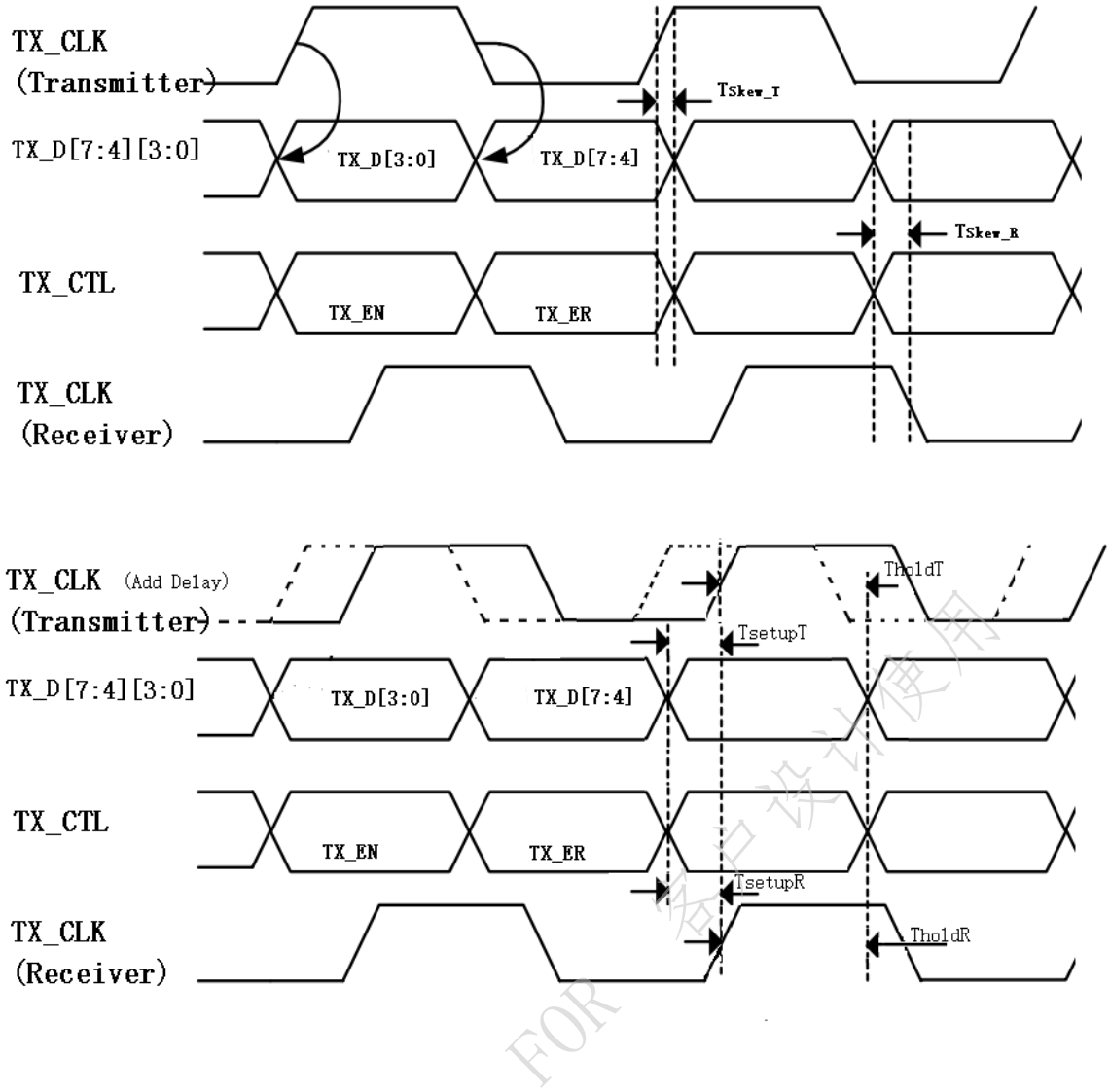


Figure 3. RGMII Transmit Timing

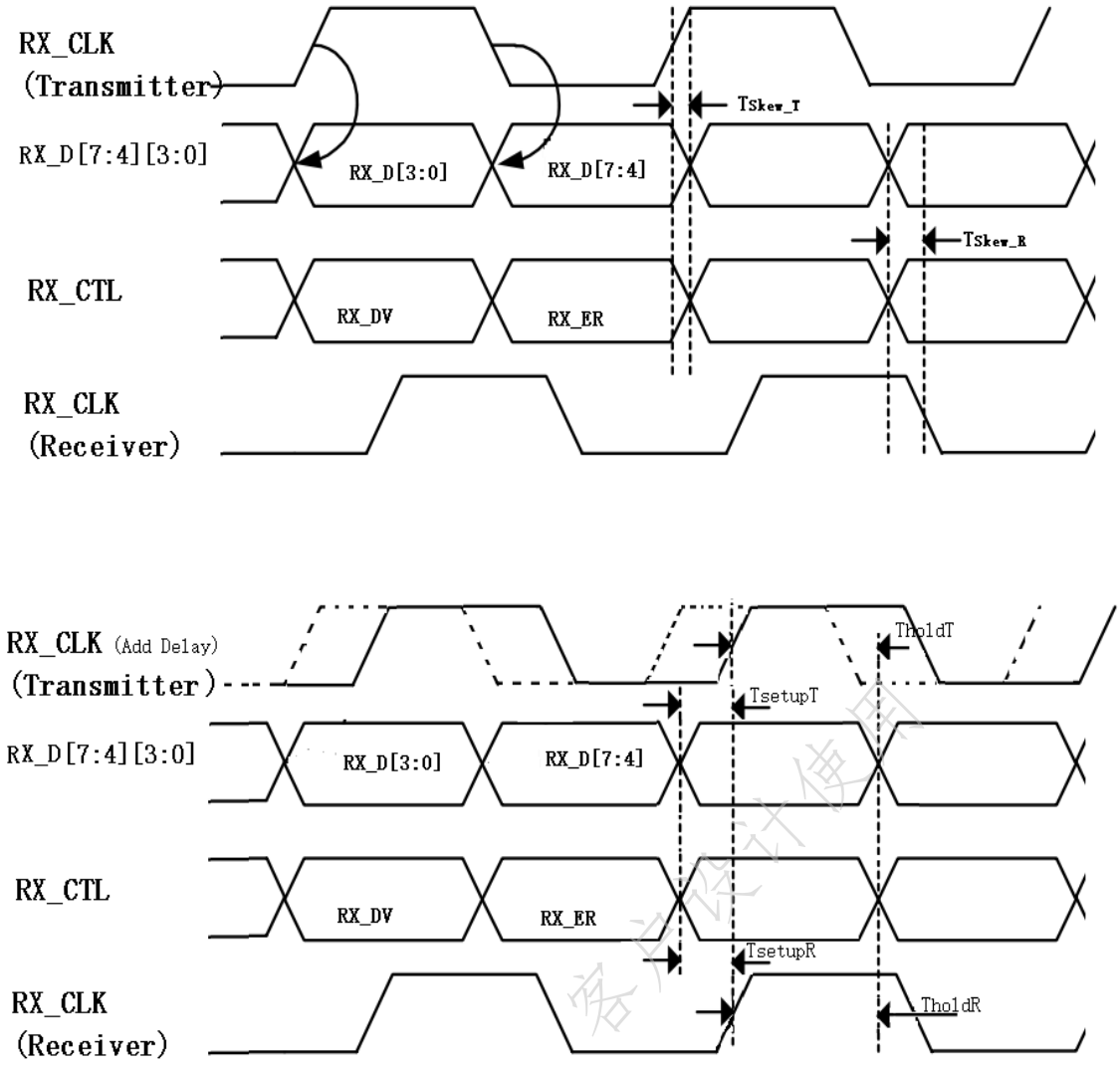


Figure 4. RGMII Receive Timing

Table8. RGMII Timing

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Clock Cycle Duration	T_{Cycle}	7.2	8.0	8.8	ns	
Duty Cycle	Duty	45	50	55	%	1000Base-T
		40	50	60	%	100Base-TX 10Base-Te
Rise/Fall Time	T_{Rise}/T_{Fall}			0.75	ns	20~80%
Data to Clock output Skew (at receiver)	T_{Skew_R}	1			ns	
Data to Clock output Skew (at transmitter)	T_{Skew_T}	-0.5		0.5	ns	

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Data to Clock Output Setup Time at transmitter (with delay integrated at transmitter)	TsetupT	1.0	2.0		ns	
Clock to Data Output Hold Time at transmitter (with delay integrated at transmitter)	TholdT	1.0	2.0		ns	
Data to Clock Input Setup Time at receiver (with delay integrated at transmitter)	TsetupR	1.0	2.0		ns	
Clock to Data Input Hold Time at receiver (with delay integrated at transmitter)	TholdR	1.0	2.0		ns	

2.5.4 SMI Interface Timing

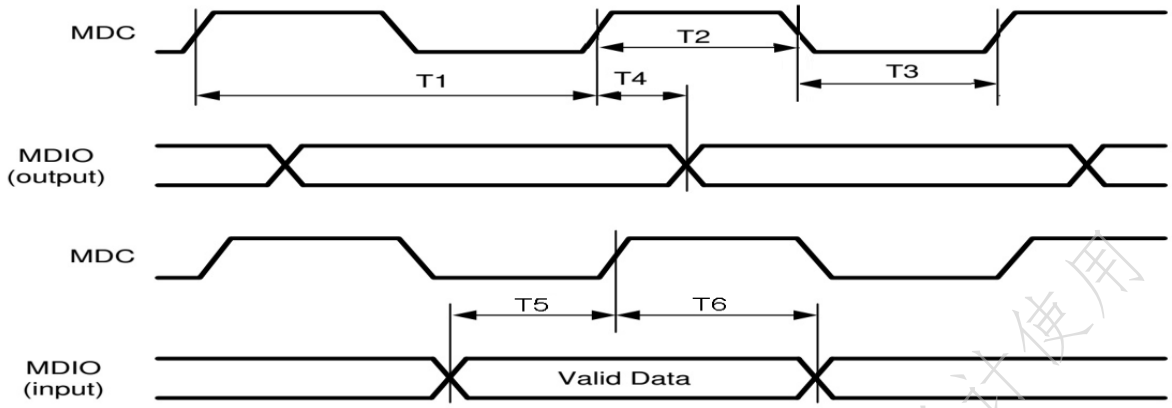


Figure 5. SMI interface Timing

Table9. RGMII Timing

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
MDC Clock Cycle Duration	T1	80			ns	
MDC Clock High Level Duration	T2	32				
MDC Clock Low Level Duration	T3	32				
MDC to MDIO (output) delay time	T4			20		
MDIO (input) to MDC setup time	T5	10				
MDIO (input) to MDC hold time	T6	10				

3 Detail Description

3.1 Block Diagram

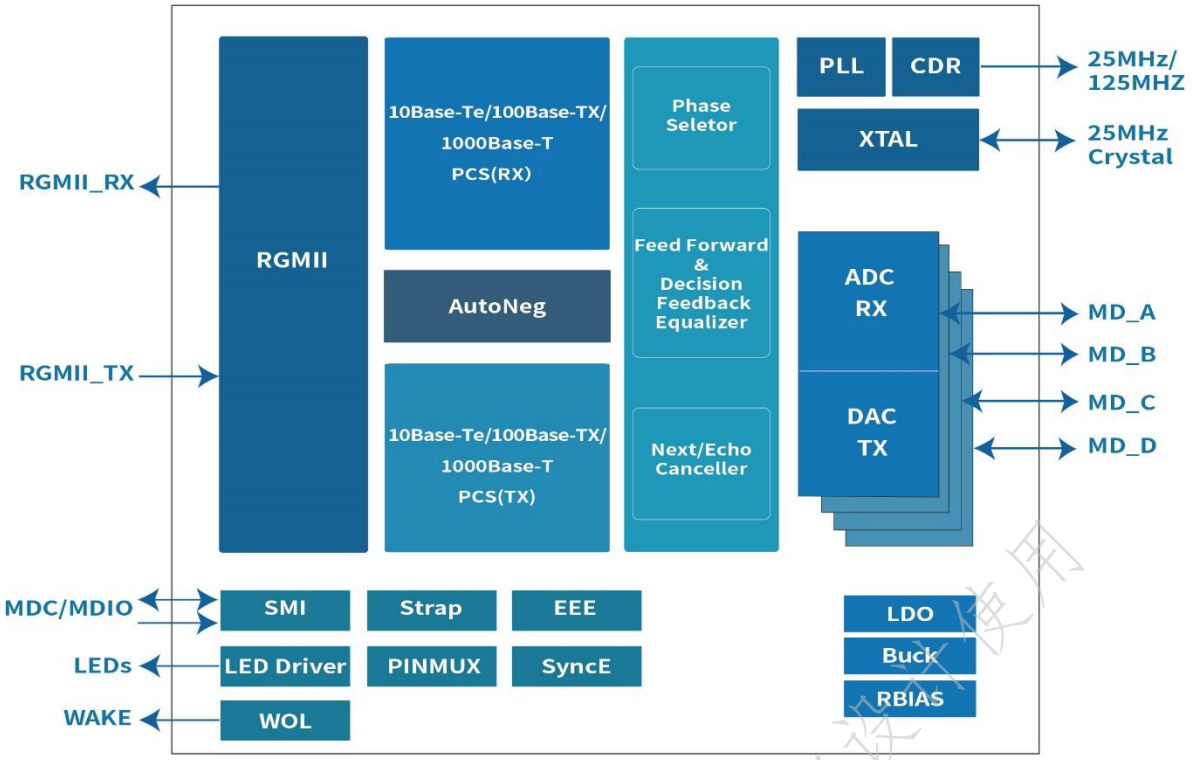


Figure 6. Block Diagram

3.2 Feature Description

3.2.1 WoL (Wake-on-LAN)

Wake-on-LAN provides a mechanism to detect dedicated frames and inform the connected MAC through either a register status change, WoL indication, or an interrupt flag. The connected devices (MAC) placed above the Physical Layer to operate in a low power mode until special magic packet are detected.

3.2.1.1 Magic Packet

If register field WOL_CON bit3 is set to “1”, Magic Packet Event is enabled. Magic Packet is defined as 6 bytes of “FF” followed by 16 iterations of the destination address, which is the waked up MAC address that is defined in register field WOL_MAC_ADDH, WOL_MAC_ADDM, WOL_MAC_ADDL. A “1” in register INTSR bit 6 indicates there is a Magic Packet received and it would be cleared after read.

3.2.2 IEEE 802.3az-2010 (EEE)

The DAP8211R(I) supports IEEE 802.3az-2010(EEE: Energy Efficient Ethernet). EEE defines a negotiation method to enable link partners to decide whether EEE is supported.

Based on link utilization efficiency and EEE protocol, the transitions would work in different mode. When no packets are being transmitted, DAP8211R(I) would work in Low Power Idle mode to save power. As soon as packets to be transmitted, DAP8211R(I) returns to normal mode, and this doesn't impact the link status and dropping frames.

3.2.3 SyncE

DAP8211R(I) supports Sync-E function.

When this function is enabled in slave mode, recovered 25MHz/125MHz clock will be output through CLK_{OUT} pad.

If the device is in master mode, the CLK_{OUT} will output the clock based on the local free run PLL.

3.2.4 nINT/nPME

The nINT/nPME pin (pin 31) is designed to notify both interrupt and WoL events. It is nINT mode at default. It could generate interrupts to external SOC.

DAP8211R(I) provides an active low interrupt output based on change of the PHY status. Every interrupt condition is represented by the read-only general interrupt status register (Interrupt Status Register (Basic register 0x13)).

The interrupts can be individually enable or disable by setting or clearing bits in the interrupt enable register (Interrupt Mask Register (Basic register 0x12)).

If nPME mode is selected (Ext_0xa00a, bit[6]=1), pin 31 becomes a fully functional nPME pin. Note that the interrupt function is disabled in this mode.

The behavior of nINT is level-triggered, the behavior of nPME is level-triggered or pulse-triggered which is controled by EXT 0xA00A bit[0].

3.2.5 MDI Interface

DAP8211R(I) supports the 1000Base-T, 100Base-TX and 10Base-Te standard as defined by the IEEE 802.3, 802.3ab and 802.3u standards.

In 1000Base-T mode, the PHY will use four pairs MDI channels for communication at 125MBaud/s through D/A or A/D converter. The communicated data are encoded/decoded in 4D-PAM5 and RGMII works at a clock speed of 125MHz. For transmitter, pulse shaping and slew rate control technology are used to eliminate EMI problem. A hybrid analog front end is employed to reduce near-end echo, which allows transmitter and receiver to share one transformer. In the digital domain, echo cancellation, cross-talk cancellation, baseline drift cancellation and adaptive equalization are realized

In 100Base-TX mode, the PHY will use two pairs MDI channels (Pairs A and B) for communication. The communicated data are encoded/decoded in 4B/5B and RGMII works at a clock speed of 25MHz.

In 10Base-Te mode, the PHY will also use two MDI channels (Pairs A and B) for communication. The communicated data are encoded/decoded in Manchester and RGMII works at a clock speed of 2.5MHz.

3.2.6 MAC Interface(RGMII)

The DAP8211R(I) supports RGMII 2.0 interface between MAC and PHY. The RGMII(Reduced Gigabit Media Independent Interface) is designed to reduce the number of pins required to interconnect the MAC and PHY (12 pins for RGMII). There are 6 pins for transmit path and 6 pins for receive path. For 100M/10M application, RGMII is similar to MII. The only difference is that tx_er/rx_er is transmitted by TX_CTL/RX_CTL on the falling edge of clock. Both rising and falling edges of the clock are used. For 1000M, the GTX_CLK and RX_CLK clocks are 125 MHz, and for 10 M and 100 M, the clock frequencies are 2.5 MHz and 25 MHz respectively.

3.2.7 Management Interface

The management interface provides access to the internal registers through the MDC and MDIO pins. The MDC signal is the management data clock reference to the MDIO signal, and clock rates up to 12.5MHz. The MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC. The MDIO pin needs a pull-up resistor.

3.2.8 Loopback Mode

There are several options for loopback mode that test and verify various functional blocks within the PHY. Enabling loopback mode allows in-circuit testing of the digital and analog data paths. Generally, the DAP8211R(I) may be configured to 4 loopback modes.

Loopback Mode	**Description**
PCS Loopback	When BMCR register field Loopback is set to “1”, data sent through RGMII will route to PCS layer rx port through PCS TX path. Then these data will route back to RGMII RX pad through PCS RX path.
External Loopback	An external loopback stub allows testing the complete data path without the need of a link partner. In this case it seems the data send through RGMII TX interface with be forwarded to RGMII RX interface through MDI interface
Remote Loopback	When MISC_CON register field Remote_loopback is set to “1”, data transmitted from rgmii tx interface will route back to rgmii rx interface. This checks if rgmii works correctly for remote link.

3.2.9 Hardware Configuration

The RGMII I/O pad voltage, RGMII TX/RX clock delay, and PHY address can be set by hardware. These configurations are setup through dedicated IO pin with external pullup/pulldown resistor. When power on reset is de-asserted, the hardware circuit will sample values on these dedicated IO pin.

<table>
<tr><th>Part Number</th><th>Dedicated IO</th><th>Description</th></tr>
<tr><td rowspan="6">DAP8211R(I)</td><td>ADR[2:0]</td><td>Set the PHY address for the device. It supports the PHY address from 0x0 to 0x7. The 0x0 is a broadcast address on default. This function can be disabled by setting MDIO config.</td></tr>
<tr><td>RXDLY</td><td>RGMII rx clock delay setting.
1: add 2ns delay on RX_CLK when RX_CLK is 125MHz
add 8ns delay on RX_CLK when RX_CLK is 25MHz/2.5MHz,
0: no delay</td></tr>
<tr><td>TXDLY</td><td>RGMII tx clock delay setting.
1: add 2ns to TX_CLK
0: no delay</td></tr>
<tr><td>PLLOFF</td><td>In sleep mode, PLL off configuration.</td></tr>
<tr><td>EN_{LDO}</td><td>Control of internal LDO for IO supply:
1: disable internal LDO, external power supply is for IO.
0: enable internal LDO.
IO supply is determined by strap VOL_CFG [1:0].</td></tr>
<tr><td>VOL_CFG[1:0]</td><td>RGMII I/O Voltage selection:
<table>
<tr><th>VOL_CFG[1:0]</th><th>External Power Supply</th><th>Internal LDO</th></tr>
<tr><td>00</td><td>3.3V</td><td>NA</td></tr>
<tr><td>01</td><td>2.5V</td><td>2.5V</td></tr>
<tr><td>10</td><td>1.8V</td><td>1.8V</td></tr>
<tr><td>11</td><td>1.8V</td><td>1.8V</td></tr>
</table></td></tr>
</table>

3.2.10 Auto-Negotiation

DAP8211R(I) supports Auto-Negotiation function which is defined in 802.3. Auto negotiation is enabled by default and can be disabled by register configuration.

Auto negotiation supports choosing the operation mode automatically by comparing its own abilities and link partner abilities. The advertised abilities include:

- Speed: 10/100/1000Mbps
- Duplex mode: full duplex/ half duplex

Auto negotiation is initialized when the following scenarios happen:

- Power-up/Hardware/Software reset
- Auto negotiation restart
- Transition from power down to power up
- Link down

3.2.11 Crossover Detection and Auto-Correction

The function implements crossover detection automatically for MDI/MDIX cables which easies connection process. The DAP8211R(I) also implements polarity auto correction when cable happens to have wrong polarity connected.

3.2.12 Baseline Wander Correction

DAP8211R(I) uses an advanced baseline wander cancellation circuit that continuously monitors and compensates for this effect, minimizing the impact of DC baseline shift on the overall error rate. Baseline wander is due to the AC coupling of the Ethernet link to the transceiver and the inability of the AC coupling to maintain voltage levels over short periods of time. As a result, the transmitted pulse is distorted, resulting in an incorrect sampling value for the affected pulse. Baseline wander is more problematic in 1000Base-T environments than in 100Base-TX environments due to DC baseline drift in transmitted and received signals.

3.2.13 Echo Cancellation

DAP8211R(I) supports echo cancellation. A hybrid circuit is used to transmit and receive simultaneously on each pair. A signal reflects back as an echo if the transmitter is not perfectly matched to the line. Other connector or cable imperfections, such as patch panel discontinuity and variations in cable impedance along the twisted pair cable, also result in drastic SNR degradation on the receive signal. The device implements a digital echo canceller to adjust for echo and is adaptive to compensate for the varied channel conditions.

3.2.14 Crosstalk Cancellation

DAP8211R(I) supports crosstalk cancellation.

The 1000Base-T physical layer uses all four pairs of wires to transmit data. Because four twisted pair pairs are tied together, significant high-frequency crosstalk occurs between the tied adjacent pairs. The device uses three parallel crosstalk cancellers on each receiving channel to eliminate the crosstalk. DAP8211R(I) eliminates the crosstalk by subtracting estimates of these signals from the equalizer output.

3.2.15 LED Configuration

DAP8211R(I) has three LED outputs for indicator.

The LEDs can be programmed to different status functions from their default value. The LED interface can either be controlled by the PHY or controlled manually, independent of the state of the PHY. They can be used to indicate operation speed, duplex mode, and link status. The LEDs can be programmed to different status functions from their default value. They can also be controlled directly from the register interface.

Because the LED pins are duplexed with the hardware configure dedicated pins, the external circuit required for hardware configure and LED circuit must be considered in order to avoid confliction.

3.2.16 Clock

DAP8211R(I) can use crystal or oscillator as clock reference input.

If use oscillator or other clock sources, use $X_{IN/OUT}$ as clock input pin, and another pin should be left floating or ground.

3.2.17 Sleep Mode

DAP8211R(I) (D) will enter sleep mode when UTP port link down and no signals over UTP cable for 40 seconds.

In sleep mode, DAP8211R(I) (D) will disable almost all the circuits except crystal clock, 10BASE-Te and MDC/MDIO interface.

In sleep mode, at regular intervals, DAP8211R(I) (D) will wake up and transmit signals via TRXP1/TRXN1. The time interval is a random value of about 2.7s.

DAP8211R(I) (D) exits sleep mode once it detects a UTP line signal

3.2.18 Power Supply

DAP8211R(I) integrates the internal switching regulator or linear regulator that regulates 3.3V power source to 1.1V power output for core power.

DAP8211R(I) with switching regulator is preferred with lower power dissipation.

DAP8211R(I) implements an option for the RGMII power pins and supports 3.3/2.5/1.8V IO voltage. For DAP8211R(I), RGMII power could be supplied from an internal regulator (2.5/1.8V) or from an external power source (3.3/2.5/1.8V).

The max ripple of 3.3V should be under 100mV, that of V_{DD_1V} should be under 80mV, and that of V_{DDA_1V} should be under 50mV.

3.2.19 Reset

The DAP8211R(I) can be reset by a hardware or software reset.

The DAP8211R(I) has a nRST pin to reset the chip. For a complete PHY reset, this pin must be asserted low for at least 10ms for the internal regulator. All registers will return to default values after a hardware reset. After nRST is released, DAP8211R(I) latches input value on strapping pins which are used as configuration information to provide flexibility in application.

IEEE registers software reset is accomplished by setting the reset bit (bit 15) of the BMCR register (address 0x0000). This bit resets the IEEE-defined standard registers.

4 Registers

The DAP8211R(I) includes 3 register groups.

	Register Group	**Description**
1	Basic Register	Basic Register based on IEEE802.3
2	Package Generation Extended Register	The Package Generation register based on Extended register mapping
3	General Extend Register	General Extend Register based on Extended Register Mapping
4	MMD Register	Extend Register based on MMD Register Mapping

Register Access Types

Type	**Description**
RW	Read and write
RO	Read only.
SC	Self-clear. If default value is '0' ('1'), writing a '1' ('0') to this register field causes the function to be activated immediately, and then the field will be automatically cleared to '0' ('1').
RC	Read clear.
SWC	Software reset to 0.
SWS	Software reset to 1.
PS	Default value depends on power on strapping.
LH	Latch high.
LL	Latch Low.

4.1 Basic Register

Item	Address	Function	
	Offset	Register Name	Description
1	0x0	BMCR	Basic Mode Control
2	0x1	BMSR	Basic Mode Status
3	0x2	PHYID1	PHY Identifier Register #1
4	0x3	PHYID2	PHY Identifier Register #2
5	0x4	ANAR	Auto-Negotiation Advertisement
6	0x5	ANLPA	Auto-Negotiation Link Partner Ability
7	0x6	ANE	Auto-Negotiate Expansion
8	0x7	ANNPT	Auto-Negotiate Next Page Transmit
9	0x8	ANNPR	Auto-Negotiate Next Page Receive
10	0x9	GBC	1000BaseT control
11	0xA	GBS	1000BaseT status
12	0xD	MMD_AC	MMD Access Control
13	0xE	MMD_AAD	MMD Access Address and Data
14	0xF	GBES	1000BaseT extended status
15	0x10	PHYCR	PHY Control Register
16	0x11	PHYSR	PHY Status Register
17	0x12	INTCR	Interrupt Control Register
18	0x13	INTSR	Interrupt Status Register
19	0x14	SPCR	Speed Configuration Register
20	0x15	RECR	Receiver Error Counter Register
21	0x1E	EXT_ADD	Extended Register Address Register
22	0x1F	EXT_DATA	Extended Register Data Register

4.1.1 BMCR(Basic Mode Control，Address: Register 0)

Table10. **BMCR**

Bit	Name	Default	Description	Access
15	Reset	0	Reset. 1: PHY reset 0: Normal operation Software Reset. Writing a '1' to this bit to reset the PHY states machine. Register 0 (BMCR) and register 1 (BMSR) will return to default values once the reset operation is done.	RW SC
14	Loopback	0	Loopback Mode. 1: Enable PCS loopback mode 0: Disable PCS loopback mode This bit controls the MII loopback. Data inside the PHY which originally	RW SWC

			comes from the MAC will be sent back to the MAC after MII loopback is enabled, but in the meantime, link will be broken.	
13	Speed[0]	0	Speed Select Bit in forced mode. 11: Reserved 10: 1000Mbps 01:100Mbps 00: 10Mbps After completing auto negotiation, this bit will reflect the speed status.	RW
12	AN_E	1	Auto-Negotiation Enable. 1: Enable Auto-Negotiation 0: Disable Auto-Negotiation	RW
11	PWD	0	Power Down. 1: Power down（only Management Interface and logic are active；link is down） 0: Normal Operation	RW SWC
10	Isolate	0	Isolate. 1: Isolate. RGMII interface is isolated； the serial management interface（MDC，MDIO）is still active. When this bit is asserted, the PHY ignores TX_D[3:0] , and TXCTL inputs, and presents a high impedance on RXC, RXCTL, RX_D[3:0] 0: Normal Operation	RW SWC
9	RS_ AN	0	Restart Auto-Negotiation. 1: Restart Auto-Negotiation 0: Normal operation	RW SC SWS
8	Duplex	1	duplex mode set if auto-negotiation is disabled (register0 bit 12=0). 1: Full duplex 0: Half duplex After completing auto-negotiation, this bit will reflect the duplex status. 1: Full duplex 0: Half duplex	RW
7	Collision Test	0	Collision Test. 1: Enable Collision Test 0: Normal Operation	RW SWC
6	Speed [1]	0	Speed Select Bit 1 Refer to bit [13].	RW
5:0	Reserved	0x0	Reserved	RO

4.1.2 BMSR（Basic Mode Status，Address: Register 1）

Table11. **BMSR**

Bit	Name	Default	Description	Access
15	100Base-T4	0	100Base-T4 Capability. 1: 100Base-T4 support	RO

			0: not 100Base-T4 support	
14	100Base-TX_F	1	100Base-TX (full) Duplex Capability. 1= full-duplex 100Base-TX can be performed by PHY. 0=full-duplex 100Base-TX can't be performed by PHY.	RO
13	100Base-TX_H	1	100Base-TX (half) Duplex Capability. 1= half-duplex 100Base-TX can be performed by PHY. 0= half-duplex 100Base-TX can't be performed by PHY.	RO
12	10Base-T_F	1	10Base-T (full) Duplex Capability. 1= full-duplex 10Base-T can be performed by PHY. 0=full-duplex 10Base-T can't be performed by PHY.	RO
11	10Base-T_H	1	10Base-T (half) Duplex Capability. 1= half-duplex 10Base-T can be performed by PHY. 0= half-duplex 10Base-T can't be performed by PHY.	RO
10	100Base-T2_F	0	100Base-T2 (full) Duplex Capability. 1= full-duplex 100Base-T2 can be performed by PHY. 0=full-duplex 100Base-T2 can't be performed by PHY.	RO
9	100Base-T2_H	0	100Base-T2(half) Duplex Capability. 1= half-duplex 10Base-T can be performed by PHY. 0= half-duplex 10Base-T can't be performed by PHY.	RO
8	Extended Status	1	1000Base-T Extended Status Register. 1: Extended status information in Register 0x0F 0: No extended status information in Register 0x0F	RO
7	Unidirect_Ability	0	1: PHY able to transmit from MII regardless of whether the PHY has determined that a valid link has been established 0: PHY able to transmit from MII only when the PHY has determined that a valid link has been established	RO
6	MF _PS	1	1=The PHY will accept management frames with preamble suppressed. A minimum of 32 preamble bits are required: the first management interface read/write transaction after reset. One idle bit is required between any two management transactions as per IEEE 802.3u specifications. 0= not accept management frames	RO
5	AN	0	Auto-Negotiation Complete. 0=Auto-Negotiation process is not complete. 1=Auto-Negotiation process is complete.	RO SWC
4	Remote Fault	0	Remote Fault. 0=Remote fault condition is not detected. 1=Remote fault condition is detected (cleared on read or by reset). When in 100Base-FX mode, this bit means an in-band signal Far-End-Fault has been detected (see Far End Fault Indication,).	RO RC SWC LH

3	AN_A	1	Auto-Negotiation Ability. 1=Auto-Negotiation can be performed by PHY 0=Auto-Negotiation can't be performed by PHY	RO
2	Link Status	0	Link Status。 1: Linked 0: Not Linked This bit indicates whether the link was lost since the last read.: the current link status, read this register twice.	RO LL SWC
1	Jabber Detect	0	Jabber Detect。 1：Jabber condition detected 0：No Jabber detected	RO RC SWC LH
0	Ex_Capability	1	1: Extended register capable (permanently=1) 0: Not extended register capable	RO

4.1.3 PHYID1（PHY Identifier Register #1，Address: Register 2）

Table12. **PHYID1**

Bit	Name	Default	Description	Access
15:0	OUI_MSB		Organizationally Unique Identifier Bit [5:0]	RO

4.1.4 PHYID2（PHY Identifier Register #2，Address： Register 3）

Table13. **PHYID2**

Bit	Name	Default	Description	Access
15:10	OUI_LSB		Organizationally Unique Identifier Bit [5:0]	RO
9:4	Model Number		Manufacture's Model Number	RO
3:0	Revision Number		Revision Number	RO

4.1.5 ANAR（Auto-Negotiation Advertising，Address: Register 4）

This register contains the advertised abilities of this device as they will be transmitted to its link partner during auto-negotiation.

Table14. **ANAR**

Bit	Name	Default	Description	Access
15	Next Page	0	Next Page Bit. If 1000BASE-T is advertised, the required next pages are automatically transmitted. This bit must be set to 0 if no	RW

			additional next page is needed. 0: Not advertised 1: Advertise	
14	ACK	0	Acknowledge 1: Acknowledge reception of link partner capability data word 0: Do not acknowledge reception	RO
13	Remote Fault	0	Remote Fault 1：Set Remote Fault bit 0：No Remote Fault bit	RW
12	Ext_NP	1	Extended EXT page enable control bit 1 = Local device supports transmission of extended next pages 0 = Local device does not support transmission of extended next pages.	RW
11	Asymmetric_PAUSE	0	Asymmetric PAUSE 1: Advertise asymmetric pause support 0: No support of asymmetric pause	RW
10	Pause	0	1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented.	RW
9	100Base-T4	0	1: 100Base-T4 is supported by local node 0: 100Base-T4 not supported by local node	RO
8	100Base-TX_F	1	1: 100Base-TX full duplex is supported by local node 0: 100Base-TX full duplex not supported by local node	RW
7	100Base-TX_H	1	1: 100Base-TX half duplex is supported by local node 0: 100Base-TX half duplex not supported by local node	RW
6	10Base-Te-F	1	1: 10Base-Te full duplex supported by local node 0: 10Base-Te full duplex not supported by local node	RW
5	10Base-Te_H	1	1: 10Base-Te half duplex is supported by local node 0: 10Base-Te half duplex not supported by local node	RW
4:0	Selector Field	0x1	Binary Encoded Selector Supported by This Node. Currently only CSMA/CD 00001 is specified. No other protocols are supported.	RW

4.1.6 ANLPA (Auto-Negotiation Link Partner Ability, Address: Register 5)

This register contains the advertised abilities of the Link Partner as received during auto-negotiation. The content changes after a successful auto-negotiation if Next-pages are supported.

Table15. **ANLPA**

Bit	Name	Default	Description	Access
15	Next Page	0	Next Page Indication of link partner. 0: capability datapage 1: no capability datapage	RO RWC

14	ACK	0	Acknowledge 1: Link partner acknowledges reception of local node's capability data word 0: No acknowledgement	RO RWC
13	Remote Fault	0	Remote Fault 1: Link partner is indicating a remote fault 0: Link partner is not indicating a remote fault	RO RWC
12	Reserved	-	Reserved.	RO RWC
11	Asymmetric_PAUSE	0	Technology Ability Field. 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause	RO RWC
10	PAUSE	0	Technology Ability Field. 1 = Link partner supports pause operation 0 = Link partner does not support pause operation	RO RWC
9	100BASE-T4	0	Technology Ability Field. 1 = Link partner supports 100BASE-T4 0 = Link partner does not support100BASE-T4	RO RWC
8	100BASETX_FULL_DUPLEX	0	Technology Ability Field. 1 = Link partner supports 100BASE-TX fullduplex 0 = Link partner does not support 100BASE-TX full-duplex	RO RWC
7	100BASETX_HALF_DUPLEX	0	Technology Ability Field. 1 = Link partner supports 100BASE-TX half duplex 0 = Link partner does not support 100BASE-TX half-duplex	RO RWC
6	10BASE Te_FULL_DUPLEX	0	Technology Ability Field. 1 = Link partner supports 10BASE-Te fullduplex 0 = Link partner does not support 10BASE-Te full-duplex	RO RWC
5	10BASETe_HALF_DUPLEX	0	Technology Ability Field. 1 = Link partner supports 10BASE-Te half duplex 0 = Link partner does not support 10BASE-Te half-duplex	RO RWC
4:0	Selector Field	0x0	Link Partner's Binary Encoded Node Selector. Currently only CSMA/CD 00001 is specified.	RO RWC

4.1.7 ANE (Auto-Negotiation Expansion Address: Register 6)

This register contains additional status: NWay auto-negotiation.

Table16. **ANE**

Bit	Name	Default	Description	Access
15:5	Reserved	-	Reserved.	RO
4	Parallel Detection Fault	0	Parallel Detection Fault 1: A fault has been detected via the Parallel Detection function 0: No fault has been detected via the Parallel Detection function	RO RC LH SWC
3	Link Partner Next Page Ability	0	Link Partner Next Page Ability 1: Link Partner is Next Page able 0: Link Partner is not Next Page able	RO LH SWC
2	Local Next Page Ability	1	Local Next Page Ability 1: Next Page is able 0: Not Next Page able	RO
1	Page Received	0	1: A New Page has been received 0: A New Page has not been received	RO RC LH
0	LP_AN_A	0	Link Partner Auto-Negotiation Ability If Auto-Negotiation is Enabled, This Bit Means: 1: Link Partner is Auto-Negotiation able 0: Link Partner is not Auto-Negotiation able	RO

4.1.8 ANNPT (Auto-Negotiation Next Page Transmit Address: Register 0x7)

Table17. **ANNPT**

Bit	Name	Default	Description	Access
15	Next Page	0	Next Page Indication. 1: More next pages to send 0: No more next pages to send	RW
14	Reserved	0	Reserved.	RO
13	Message Page	1	Message Page. 1: Message Page 0: Unformatted Page	RW
12	Acknowledge2	0	Acknowledge2 1: Local device has the ability to comply with the message received 0: Local device has no ability to comply with the message received	RW
11	Toggle	0	Toggle Bit.	RO
10:0	Message/Unformatted Field	0x1	Content of Message/Unformatted Page.	RW

4.1.9 ANNPR (Auto-Negotiation Next Page Receive Address: Register 0x8)

Table18. **ANNPR**

Bit	Name	Default	Description	Access
15	Next Page	0	Next Page Indication. 1: More next pages 0: No more next pages	RO
14	Acknowledge	0	Acknowledge.	RO
13	Message Page	0	Message Page. 1: Message Page 0: Unformatted Page	RO
12	Acknowledge2	0	Acknowledge2	RO
11	Toggle	0	Toggle Bit.	RO
10:0	Message/Unformatted Field	0x0	Content of Message/Unformatted Page.	RO

4.1.10 GBC (1000Base-T Control Address: Register 0x9)

Table19. **GBC**

Bit	Name	Default	Description	Access
15:13	Test Mode	0x0	Test Mode Select. 000: Normal Mode 001: Test Mode 1 - Transmit WaveformTest 010: Test Mode 2 - Transmit Jitter Test (MASTER mode) 011: Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100: Test Mode 4 - Transmit Distortion Test 101, 110, 111: Reserved	RW
12	M/S Enable	0	MASTER/SLAVE Manual Configuration Enable 1: Manual MASTER/SLAVE configuration 0: Automatic MASTER/SLAVE	RW
11	M/S Configure	0	Configure Master/Slave Value. 1: Manual configure as MASTER 0: Manual configure as SLAVE	RW
10	Port Type	0	Advertise Device Type Preference. 1: Prefer multi-port device (MASTER) 0: Prefer single port device (SLAVE)	RW
9	1000BASE-T Full Duplex	1	Advertise 1000BASE-T Full-Duplex Capability. 1: Advertise 0: Do not advertise	RW
8	1000BASE-T Half-Duplex	0	Advertise 1000BASE-T Half Duplex Capability. 1: Advertise 0: Do not advertise	RW
7:0	Reserved	0x0	Reserved.	RO

4.1.11 GBS (1000Base-T Status Address: Register 0xA)

Table20. **GBS**

Bit	Name	Default	Description	Access
15	MASTER/ SLAVE CONFIGURATION FAULT	0	Master / Slave Manual Configuration Fault Detected: 1 = Manual Master/Slave Configuration fault detected. 0 = No Manual Master/Slave Configuration fault detected This register bit will clear on read,	RO RC SWC LH
14	MASTER/ SLAVE CONFIGURATION RESOLUTION	0	Master / Slave Configuration Results: 1 = Configuration resolved to MASTER. 0 = Configuration resolved to SLAVE.	RO
13	LOCAL RECEIVER STATUS	0	Local Receiver Status: 1 = Local receiver is OK. 0 = Local receiver is not OK.	RO
12	Remote Receiver	0	1 = Remote Receiver OK 0 = Remote Receiver not OK	RO
11	1000BASE-T Full Duplex	0	Advertise 1000BASE-T Full-Duplex Capability. 1: Advertise 0: Do not advertise	RO
10	1000BASE-T HALF DUPLEX	0	Link Partner 1000BASE-T Half Duplex Capable: 1 = Link Partner capable of 1000Base-T Half Duplex. 0 = Link partner not capable of 1000Base-T Half Duplex	RO
9:8	Reserved	0	Reserved.	RO
7:0	Idle Error Count	0x0	MSB of Idle Error Counter. The register indicates the idle error count since the last read operation performed to this register. The counter pegs at 11111111 and does not roll over.	RO

4.1.12 MMD_AC (MMD Access Control; Address: Register 0xD)

Table21. **MMD_AC**

Bit	Name	Default	Description	Access
15:14	MMD Function	0x0	MMD Function about Data and Address 00: Address 01: Data; no post increment 10: Data; post increment on reads and writes 11: Data; post increment on writes only	RW
13:5	RSVD	0x0	Reserved.	RO
4:0	Device_ADD	0x0	MMD device address. 00001: MMD1	RW

			00011: MMD3 00111: MMD7	

Note 1: Used in conjunction with the MAADR (Register 14) to provide access to the MMD address space.

Note 2: If the access of MAADR is: address (Function=00) then it is directed to the address register within the MMD associated with the value in the Device_ADD field.

Note 3: If the access of MAADR is: data (Function=00) then both the Device_ADD field and the MMD address register direct the MAADR data accesses to the appropriate registers within the MMD.

4.1.13 MMD_AAD (MMD Access Address Data, Address: Register 0xE)

Table22. **MMD_AAD**

Bit	Name	Default	Description	Access
15:0	Address Data	0x0	[15:14] =00 It means MMD DEVAD's address register [15:14] =01, 10, or 11 It means MMD DEVAD's data register as indicated by the contents of its address register	RW

4.1.14 1000BTS (1000BASE-T Status Register, Address: Register 0xF)

Table23. **4.15 1000BTS**

Bit	Name	Default	Description	Access
15	1000BASE-X FULL DUPLEX	0	1000BASE-X Full Duplex Support: 1 = 1000BASE-X Full Duplex is supported by the local device. 0 = 1000BASE-X Full Duplex is not supported by the local device.	RO
14	1000BASE-X HALF DUPLEX	0	1000BASE-X Half Duplex Support: 1 = 1000BASE-X Half Duplex is supported by the local device. 0 = 1000BASE-X Half Duplex is not supported by the local device.	RO
13	1000BASE-T FULL DUPLEX	1	1000BASE-T Full Duplex Support: 1 = 1000BASE-T Full Duplex is supported by the local device. 0 = 1000BASE-T Full Duplex is not supported by the local device.	RO
12	1000BASE-T HALF DUPLEX	0	1000BASE-T Half Duplex Support: 1 = 1000BASE-T Half Duplex is supported by the local device. 0 = 1000BASE-X Half Duplex is not supported by the local device.	RO
11:0	RSVD	0x0	Reserved.	RO

4.1.15 PHYCR (PHY Control Register, Address: Register 0x10)

Table24. **PHYCR**

Bit	Name	Default	Description	Access

15:7	RSVD	0x0	Reserved.	RO
6:5	MDI_CROSSOVER	0x3	MDI Crosssover Mode: 11 = Enable automatic crossover 10 = Reserved 01 = Manual MDI-X configuration 00 = Manual MDI configuration	RW
4	RSVD	0	Reserved.	RO
3	CRS-TX	0	This bit is effective in 10BASE-Te half-duplex mode and 100BASE-TX mode: 1 = Assert CRS on transmitting or receiving 0 = Never assert CRS on transmitting, only assert it on receiving.	RW
2	EN_SEQ_Test	0	1 = SQE test enabled, 0 = SQE test disabled Note: SQE Test is automatically disabled in full-duplex mode regardless the setting in this	RW
1	POL_REV	1	If polarity reversal is disabled, the polarity is forced to be normal in 10BASE-Te. 1 = Polarity Reversal Enabled 0 = Polarity Reversal Disabled	RW
0	DIS_JAB	0	1 = Disable 10BASE-Te jabber detection function 0 = Enable 10BASE-Te jabber detection function	RW

4.1.16 PHYSR (PHY Status Register, Address: Register 0x11)

Table25. **PHYSR**

Bit	Name	Default	Description	Access
15:14	SPEED SELECTION	0x0	Speed Select Status: 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps	RO
13	DUPLEX MODE	0	Duplex Mode Status: 1 = Full Duplex 0 = Half Duplex.	RO
12	PAGE RECEIVED	0	Page Received: This bit is latched high and will be cleared upon a read. 1 = Page received. 0 = No page received.	RO
11	SPEED DUPLEX RESOLVED	0	Speed Duplex Resolution Status: 1 = Auto-Negotiation has completed or is disabled. 0 = Auto-Negotiation is enabled and has not completed	RO
10	LINK_STATUS	0	1 = Link up 0 = Link down	RO
9:7	RSVD	0x0	Reserved.	RO
6	MDI Crossover Status	0	1 = MDIX 0 = MDI	RO
5	Wirespeed downgrade	0	1 = Downgrade 0 = No Downgrade	RO

4	RSVD	0	Reserved.	RO
3	Transmit Pause	0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed. This bit indicates MAC pause resolution. This bit is for information purposes only and is not used by the device. When in force mode, this bit is set to be 0. 1 = Transmit pause enabled 0 = Transmit pause disabled	RO
2	Receive Pause	0	This status bit is valid only when bit[11] is 1. Bit[11] is set when Auto-Negotiation is completed. This bit indicates MAC pause resolution. This bit is for information purposes only and is not used by the device. When in force mode, this bit is set to be 0. 1 = Receive pause enabled 0 = Receive pause disabled	RO
1	Polarity	0	1 = Reverted polarity 0 = Normal polarity	RO
0	Jabber	0	1 = Jabber 0 = No jabber	RO

4.1.17 INTCR (Interrupt Control Register, Address: Register 0x12)

Table26. **INTCR**

Bit	**Name**	**Default**	**Description**	**Access**
15:14	AN_ERR_INT_EN	0x0	Enable Auto-Negotiation Error Interrupt: 1 = Enable Auto-Negotiation Error interrupt. 0 = Disable Auto-Negotiation Error interrupt.	RW
14	SPEED_CHNG_INT_EN	0	Enable Speed Change Interrupt: 1 = Enable Speed Change interrupt. 0 = Disable Speed Change interrupt.	RW
13	DUPLEX_MODE_CHNG_INT_EN	0	Enable Duplex Mode Change Interrupt: 1 = Enable Duplex Mode Change interrupt. 0 = Disable Duplex Mode Change interrupt.	RW
12	PAGE_RECEIVED_INT_EN	0	Enable Page Received Interrupt: 1 = Enable Page Received Interrupt. 0 = Disable Page Received Interrupt.	RW
11	LINK_FAIL_INT_EN	0	Enable Link Fail Interrupt: 1 = Enable Link Fail Interrupt. 0 = Disable Link Fail Interrupt.	RW
10	LINK_COMP_INT_EN	0	Enable Link Complete Interrupt: 1 = Enable Link Complete Interrupt. 0 = Disable LINK Complete Interrupt.	RW
9:7	RSVD	0x0	Reserved.	RW
6	WOL_INT_EN	0	Enable Wake-on-LAN Interrupt: 1 = Enable Wake-on-LAN Interrupt. 0 = Disable Wake-on-LAN Interrupt	RW
5	WS_DG_INT_EN	0	Wirespeed downgraded Interrupt 1 = Enable Interrupt. 0 = Disable Interrupt	RW
4:2	RSVD	0x0	Reserved.	RW
1	PL_CH_INT_EN	0	Enable Polarity Change Interrupt: 1 = Enable Polarity Change interrupt.	RW

			0 = Disable Polarity Change interrupt.	
0	JB_INT_EN	0	Enable Jabber Interrupt: 1 = Enable Jabber interrupt. 0 = Disable Jabber interrupt	RW

4.1.18 INTSR (Interrupt Status Register, Address: Register 0x13)

Table27. **INTSR**

Bit	Name	Default	Description	Access
15:14	AN_ERR_INT	0x0	Auto-Negotiation Error Interrupt: 1 = Occur Auto-Negotiation Error interrupt 0 = No Auto-Negotiation Error interrupt.	RO RC
14	SPEED_CHNG_INT_EN	0	Speed Change Interrupt: 1 = Occur Speed Change interrupt. 0 = No Speed Change interrupt.	RO RC
13	DUPLEX_MODE_CHNG_INT_EN	0	Duplex Mode Change Interrupt: 1 = Occur Duplex Mode Change interrupt. 0 = No Duplex Mode Change interrupt.	RO RC
12	PAGE_RECEIVED_INT_EN	0	Page Received Interrupt: 1 = Occur Page Received Interrupt. 0 = No Page Received Interrupt.	RO RC
11	LINK_FAIL_INT_EN	0	Link Fail Interrupt: 1 = Occur Link Fail Interrupt. 0 = No Link Fail Interrupt.	RO RC
10	LINK_COMP_INT_EN	0	Link Complete Interrupt: 1 = Occur Link Complete Interrupt. 0 = No LINK Complete Interrupt.	RO RC
9:7	RSVD	0x0	Reserved.	RO RC
6	WOL_INT_EN	0	Wake-on-LAN Interrupt: 1 = Occur Wake-on-LAN Interrupt. 0 = No Wake-on-LAN Interrupt	RO RC
5	WS_DG_INT_EN	0	Wirespeed downgraded Interrupt 1 = Occur Interrupt. 0 = No Interrupt	RO RC
4:2	RSVD	0x0	Reserved.	RO RC
1	PL_CH_INT_EN	0	Polarity Change Interrupt: 1 = Occur Polarity Change interrupt. 0 = No Polarity Change interrupt.	RO RC
0	JB_INT_EN	0	Jabber Interrupt: 1 = Occur Jabber interrupt. 0 = No Jabber interrupt	RO RC

4.1.19 SPCR (Speed Configuration Register, Address: Register 0x14)

Table28. **SPCR**

Bit	Name	Default	Description	Access
15:12	RSVD	0x0	Reserved.	RO
11:6	RSVD	0x20	Reserved.	RW

5	SP_DG_EN	1	1: Enables auto speed downgrade function. Writing this bit requires a software reset to up 0: Disable auto speed downgrade function	RW POS
4:2	AN_AT_SPDG	0x3	Attempts times (set value + additional 2) before downgrading. Such as 11: Attempts five times (set value 3 + additional 2) before downgrading. The number of attempts can be changed by these bits. Only take effect after software rese	RW
1	RSVD	0	Reserved.	RW
0	RSVD	0	Reserved.	RO

4.1.20 RECR (Receiver Error Counter Register, Address: Register 0x15)

Table29. **RECR**

Bit	Name	Default	Description	Access
15:0	RXERCNT[15:0]	0x0	RX_ER Counter: Receive error counter. This register saturates at the maximum value of 0xFFFF and hold it, not roll over.	RO SWC

4.1.21 EXT_ADD (Extended Register Address Register, Address: Register 0x1E)

Table30. **EXT_ADD**

Bit	Name	Default	Description	Access
15:8	RSVD	0x0	Reserved.	RO
7:0	EXT_ADD	0x0	Extended Register Address	RW

4.1.22 EXT_DATA (Extended Register Data Register, Register 0x1F)

Table31. **EXT_DATA**

Bit	Name	Default	Description	Access
15:0	EXT_DATA	0x0	Extended Register data	RW

4.2 Package Generation Extended Register

4.2.1 PKGC1 (Package Generation Configure1, Address: Register 0x38)

Table32. **PKGC1**

Bit	Name	Default	Description	Access
15:13	RSVD	-	Reserved.	RO
12	EN_PKG_DA_SA	0	1: set the DA/SA of the packet generated by package generation to a programmed value; For DA, if 0x38 bit[11] is 1, the DA is set to broadcast address FF-FF-FF-FF-FF-FF; else, the DA is set to fix value, the highest 5 Bytes are 00-00-00-00-00, and the lowest 1 Byte is programmed by EXT 0x3A bit[15:8]. For SA, the highest 5 Bytes are 00-00-00-00-00, and the lowest 1 Byte is	RW

			programmed by EXT 0x3A bit[7:0]. 0: the DA/SA is not programmed	
11	PKG_BRD	0	1: set the DA to broadcast address FF-FF-FFFF-FF-FF 0: set the DA to a fixed programmed value. Valid when 0x38 bit[12] is 1.	RW
10	PKG_TXSCR	0	1: The package checker on TX side will check the transmit data generated by pkg_gen; 0: The package checker on TX side will check the transmit data of UTP GMII/MII.	RW
9	PKG_AZ_EN	0	1:Enable send LPI pattern during the IPG of the packages sent by pkg_gen. 0:Disable send LPI pattern during the IPG of the packages sent by pkg_gen	RW
8:0	PKG_IN_AZ_TIME	0x1FF	The time of LPI pattern is sent. Unit is us.	RW

4.2.2 PKGC2(Package Generation Configure2, Address: Register 0x39)

Table33. **PKGC2**

Bit	Name	Default	Description	Access
15:8	PKG_PRE_AZ_TIME	0x20	The time from the end of last package to the beginning of LPI pattern. Unit is us.	RW
7:0	PKG_AFT_AZ_TIME	0x19	The time from the end of LPI pattern to the beginning of next package. Unit is us.	RW

4.2.3 PKGC3(Package Generation Configure3, Address: Register 0x3A)

Table34. **PKGC3**

Bit	Name	Default	Description	Access
15:8	PKG_DA	0x0	Lowest 8 bits of DA, others are zero. Refer to EXT 0x38 bit[12] for detail.	RW
7:0	PKG_SA	0x0	Lowest 8 bits of SA, others are zero. Refer to EXT 0x38 bit[12] for detail	RW

4.2.4 PKGC4(Package Generation Configure4, Address: Register 0x3B)

Table35. **PKGC4**

Bit	Name	Default	Description	Access
15:8	RSVD	-	Reserved.	RO
7:0	PKG_DATA_FIX	0x0	The fixed GMII data pattern that will be sent. Valid when EXT 0xA0 bit[1:0] is 0x3.	RW

4.2.5 PKGC5 (Package Generation Configure5, Address: Register 0xA0)

Table36. **PKGC5**

Bit	Name	Default	Description	Access
15	PKG_CHK_EN	0	RX checker checks the UTP GMII/MII RX data; TX checker checks the UTP GMII/MII TX data. 1: Enable UTP RX/TX package checker. 0: Disable UTP RX/TX package checker	RW
14	PKG_GATE_EN	1	1: Enable gate all the clocks to package self test module when bit15 PKG_CHK_EN is 0, bit13 PKG_GEN_MODE is 1 and bit12 PKG_GEN_EN is 0; 0: Not gate the clocks.	RW
13	PKG_GEN_MODE	1	1: normal mode, to send GMII/MII TX data from RGMII; 0: test mode, to send out the GMII/MII data generated by UTP pkg_gen module.	RW
12	PKG_GEN_EN	0	1: to enable pkg_gen generating GMII/MII packages. But, the data will only be sent to transceiver when Bit13 PKG_GEN_MODE is 1'b0. If PKG_BUR_SIZE is 0, continuous packages will be generated and will be stopped only when PKG_GEN_EN is set to 0; Otherwise, after the expected packages are generated, pkg_gen will stop, PKG_GEN_EN will be self-cleared	RW SC
11:8	PKG_PRM_LENGTH	0x8	The preamble length of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.	RW
7:4	PKG_IPG_LENGTH	0xD	The IPG of the generated packages, in Byte unit for setting smaller than 12. For setting 13, ipg is 2ms; for setting 14, ipg is 20ms; for 15, ipg is 400ms; Pkg_gen function only support >=2Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.	RW
3	RESV	0	Resvered	RW
2	PKG_COR_CRC	0	1: to make pkg_gen to send out CRC error packages. 0: pkg_gen sends out CRC good packages.	RW
1:0	PKG_PL	0x0	Control the payload of the generated packages. 11: fix pattern set by EXT 0x3B bit7:0 10: fix pattern 0x5AA55AA5… 01: random payload; 00: increased Byte payload	RW

4.2.6 PKGC6(Package Generation Configure6, Address: Register 0xA1)

Table37. **PKGC6**

Bit	Name	Default	Description	Access
15:0	PKG_LENGTH	0x40	the length of the generated packages	RW

4.2.7 PKGC7(Package Generation Configure7, Address: Register 0xA2)

Table38. **PKGC7**

Bit	Name	Default	Description	Access
15:0	PKG_BUR_SIZE	0x0	the number of packages in a burst of package generation.	RW

4.2.8 PKG_RV_H(Package Receiver Valid High, Address: Register 0xA3)

Table39. **PKG_RVH**

Bit	Name	Default	Description	Access
15:0	PKG_RV_H	0x0	PKG_RV[31:16], PKG_RV is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.	RO RC

4.2.9 PKG_RV_L(Package Receiver Valid Low, Address: Register 0xA4)

Table40. **PKG_RVL**

Bit	Name	Default	Description	Access
15:0	PKG_RV_L	0x0	PKG_RV [15:0], PKG_RV is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.	RO RC

4.2.10 PKG_RX_OSH(Package Receiver OS High, Address: Register 0xA5)

Table41. **PKG_RX_OSH**

Bit	Name	Default	Description	Access
15:0	PKG_RX_OSH	0x0	PKG_RX_OS[31:16], PKG_RX_OS is the number of RX packages from wire whose CRC are good and length are >1518Byte.	RO RC

4.2.11 PKG_RX_OSL(Package Receiver OS Low, Address: Register 0xA6)

Table42. **PKG_RX_OSL**

Bit	Name	Default	Description	Access
15:0	PKG_RX_OSL	0x0	PKG_RX_OS [15:0], PKG_RX_OS is the number of RX packages from wire whose CRC are good and length are >1518Byte.	RO RC

4.2.12 PKG_RX_USH(Package Receiver US High, Address: Register 0xA7)

Table43. **PKG_RX_USH**

Bit	Name	Default	Description	Access
15:0	**PKG_RX_USH**	0x0	PKG_RX_USH [31:16], PKG_RX_USH is the number of RX packages from wire whose CRC are good and length are <64Byte.	RO RC

4.2.13 PKG_RX_USL(Package Receiver US Low, Address: Register 0xA8)

Table44. **PKG_RX_USL**

Bit	Name	Default	Description	Access
15:0	PKG_RX_USL	0x0	PKG_RX_USH [15:0], PKG_RX_USH is the number of RX	RO

			packages from wire whose CRC are good and length are <64Byte.	RC

4.2.14 PKG_RX_ERR(Package Receiver Error, Address: Register 0xA9)

Table45. **PKG_RX_ERR**

Bit	Name	Default	Description	Access
15:0	PKG_IB_ERR	0x0	PKG_IB_ERR is the number of RX packages from wire whose CRC are wrong and length are >=64Byte, <=1518By	RO RC

4.2.15 PKG_RX_OS_ERR(Package Receiver OS Error, Address: Register 0xAA)

Table46. **PKG_RX_OSBAD**

Bit	Name	Default	Description	Access
15:0	PKG_RX_OS_ERR	0x0	PKG_RX_OS_ERR is the number of RX packages from wire whose CRC are wrong and length are >1518Byte.	RO RC

4.2.16 PKG_RX_FRM（Package Receiver Fragment, Address: Register 0xAB)

Table47. **PKG_RX_FRM**

Bit	Name	Default	Description	Access
15:0	PKG_RX_FRM	0x0	PKG_RX_FRM is the number of RX packages from wire whose length are <64Byte.	RO RC

4.2.17 PKG_RX_NOSFD（Package Receiver NOSFD, Address: Register 0xAC)

Table48. **PKG_RX_FRM**

Bit	Name	Default	Description	Access
15:0	PKG_RX_NOSFD	0x0	PKG_RX_NOSFD is the number of RX packages from wire whose SFD is missed.	RO RC

4.2.18 PKG_TV_H(Package Transmit Valid High, Address: Register 0xAD)

Table49. **PKG_RVH**

Bit	Name	Default	Description	Access
15:0	PKG_TV_H	0x0	PKG_TV[31:16], PKG_TV is the number of TX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.	RO RC

4.2.19 PKG_TV_L(Package Transmit Valid Low, Address: Register 0xAE)

Table50. **PKG_TV_L**

Bit	Name	Default	Description	Access
15:0	PKG_TV_L	0x0	PKG_TV[15:0], PKG_TV is the number of TX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.	RO RC

4.2.20 PKG_TX_OSH(Package Transmit OS High, Address: Register 0xAF)

Table51. **PKG_TX_OSH**

Bit	Name	Default	Description	Access
15:0	PKG_TX_OSH	0x0	PKG_TX_OS [31:16], PKG_TX_OS is the number of TX packages from wire whose CRC are good and length are >1518Byte.	RO RC

4.2.21 PKG_TX_OSL(Package Transmit OS Low, Address: Register 0xB0)

Table52. **PKG_TX_OSL**

Bit	Name	Default	Description	Access
15:0	PKG_TX_OSL	0x0	PKG_TX_OS [15:0], PKG_TX_OS is the number of TX packages from wire whose CRC are good and length are >1518Byte.	RO RC

4.2.22 PKG_TX_USH(Package Transmit US High, Address: Register 0xB1)

Table53. **PKG_TX_USH**

Bit	Name	Default	Description	Access
15:0	PKG_TX_USH	0x0	PKG_TX_USH [31:16], PKG_TX_USH is the number of TX packages from wire whose CRC are good and length are <64Byte.	RO RC

4.2.23 PKG_TX_USL(Package Transmit US Low, Address: Register 0xB2)

Table54. **PKG_TX_USL**

Bit	Name	Default	Description	Access
15:0	PKG_TX_USL	0x0	PKG_TX_USH [15:0], PKG_TX_USH is the number of TX packages from wire whose CRC are good and length are <64Byte.	RO RC

4.2.24 PKG_TX_ERR(Package Transmit Error, Address: Register 0xB3)

Table55. **PKG_TX_ERR**

Bit	Name	Default	Description	Access
15:0	PKG_OB_ERR	0x0	pkg_ob_err is the number of TX packages from wire whose CRC are wrong and length are >=64Byte, <=1518By	RO RC

4.2.25 PKG_TX_OS_ERR(Package Transmit OS Error, Address: Register 0xB4)

Table56. **PKG_TX_OSBAD**

Bit	Name	Default	Description	Access
15:0	PKG_TX_OS_ERR	0x0	It is the number of TX packages from wire whose CRC are wrong and length are >1518Byte.	RO RC

4.2.26 PKG_TX_FRM（Package Transmit Fragment, Address: Register 0xB5)

Table57. **PKG_TX_FRM**

Bit	Name	Default	Description	Access
15:0	PKG_TX_FRM	0x0	PKG_TX_FRM is the number of TX packages from wire whose length are <64Byte.	RO RC

4.2.27 PKG_TX_NOSFD（Package Transmit NOSFD, Address: Register 0xB6)

Table58. **PKG_TX_FRM**

Bit	Name	Default	Description	Access
15:0	PKG_TX_NOSFD	0x0	PKG_TX_NOSFD is the number of TX packages from wire whose SFD is missed.	RO RC

4.3 General Extended Register

4.3.1 PHY_CON (PHY Device Control Register, Address: Register 0xA001)

Table59. **PHY_CON**

Bit	Name	Default	Description	Access
15	SW_RST_MODE	1	Device mode change Software reset. Low active, self clear	RW SC
14:12	RESV	0x0	Reserved	RW
11	IDDQ_MODE	0	1: Iddq test mode 0: Normal mode	RW
10	RESERVED	0	Reserved	RO
9	EN_GATE_RX_CLK_RGMI	0	1=to close RXC when PHY link down; 0=do not close RXC when PHY link down.	RW
8	RXC_DLY_EN	1	rgmii clk 2ns delay control, depend on strapping	RW POS
7	RESERVED	0	Reserved	RO
6	EN_LDO	1	rgmii ldo enable, default is 0 and will be set to 1 after power strapping is done	RW
5:4	CFG_LDO	0x0	Rgmii ldo voltage and RGMII/MDC/MDIO	RW

			PAD's level shifter control. Depends on strapping. 11: 1.8v 10: 1.8v 01: 2.5v 00: 3.3v	
3:0	RESV	0x0	Reserved	RO

4.3.2 RGMII_CON (RGMII Control Register, Address: Register 0xA003)

Table60. **RGMII_CON**

Bit	Name	Default	Description	Access
15	RESV	0	Reserved	RW
14	TX_CLK_SEL	0	1: use inverted RGMII TX_CLK to drive the RGMII TX_CLK delay train.Used for debug 0: use original RGMII TX_CLK to drive the RGMII TX_CLK delay train;	RW
13:10	RX_DELAY_SEL	0x0	RGMII RX_CLK delay train configuration,about 150ps per step	RW
9	EN_RGMII_FD_CRS	0	See EXT 0xA003 bit[8].	RW
8	EN_RGMII_CRS	0	0: to not encode GMII/MII CRS into RGMII OOB; 1: to encode GMII/MII CRS into RGMII OOB when it's half duplex mode or EXT 0xA003 bit[9] is 1.	RW
7:4	TX_DELAY_SEL_FE	0xF	RGMII TX_CLK delay train configuration when speed is 100Mbps or 10Mbps, it's 150ps per step typically.	RW
3:0	TX_DELAY_SEL	0x1	RGMII TX_CLK delay train configuration when speed is 1000Mbps, it's150ps per step typically.	RW

4.3.3 RGMII_STA (RGMII Status Register, Address: Register 0xA004)

Table61. **RGMII_STA**

Bit	Name	Default	Description	Access
15:14	SPEED_RGPHY	0x0	RGMII's speed information when it works as RGMII PHY. It's also the source of RGMII OOB.	RO
13	DUPLEX_RGPHY	0	RGMII's duplex information when it works as RGMII PHY. It's also the source of RGMII OOB.	RO
12	LINK_UP_RGPHY	0	RGMII's linkup information when it works as RGMII PHY. It's also the source of RGMII OOB.	RO
11:10	PAUSE_RGPHY	0x0	RGMII's pause information when it works as RGMII PHY.	RO
9	EEE_CAP_RGPHY	0	RGMII's EEE capability information when it works as RGMII PHY.	RO
8	EEE_CLKSTP_CAP_RGPHY	0	RGMII's EEE clock stopable capability information when it works as RGMII PHY.	RO

7:0	RESV	0x0	Reserved	RO

4.3.4 SMI_RGMII_CON (SMI & RGMII Control Register, Address: Register 0xA005)

Table62. **SMI_RGMII_CON**

Bit	Name	Default	Description	Access
15:11	RESV	0x0	Reserved	RO
10	BYPASS_MDIO_WATCHDOG	0	bypass mdio watch dog	RW
9:8	RESERVED	0x0	Reserved	RO
7	EN_MDC_LA	0x1	enable mdc latch for read data	RW
6	EN_PHYADDR0	1	1: to always respond to MDIO command whose PHYAD field is 0; 0: to only respond to MDIO command whose PHYAD filed equals to PHY address strapping.	RW
5	EN_BDCST_ADDR	0	enable broadcast address	RW
4:0	BDCST_ADDR	0x0	broadcast address	RW

4.3.5 MISC_CON (MISC Control Register, Address: Register 0xA006)

Table63. **MISC_CON**

Bit	Name	Default	Description	Access
15:8	RESV	0x0	Reserved	RW
7	JUMBO_ENABLE	0	enable jumbo frame	RW
6	RESERVED	0	Reserved	RW
5	REMOTE_LOOPBACK	0	set remote loopback for UTP	RW
4	ULDATA_RLOOPBACK	0	1=remain upload data when remote loopback is set for phy	RW
3	BP_GMII_FATAL_RST	1	bypass gmii fifo overflow and underflow rst	RW
2:0	RESV	0x5	Reserved	RW

4.3.6 WOL_MAC_ADDH(WOL MAC Highest Address Register, Address: Register 0xA007)

Table64. **WOL_MAC_ADDH**

Bit	Name	Default	Description	Access
15:0	WOL_MAC_ADDR_H	0x0	highest 16 bits of MAC address used for WOL 47:32	RW

4.3.7 WOL_MAC_ADDM(WOL MAC Middle Address Register, Address: Register 0xA008)

Table65. **WOL_MAC_ADDM**

Bit	Name	Default	Description	Access
15:0	WOL_MAC_ADDR_M	0x0	Middle 16 bits of MAC address used for WOL 31:16	RW

4.3.8 WOL_MAC_ADDL(WOL MAC Lowest Address Register, Address: Register 0xA009)

Table66. **WOL_MAC_ADDL**

Bit	Name	Default	Description	Access
15:0	WOL_MAC_ADDR_L	0x0	Lowest 16 bits of MAC address used for WOL 31:16	RW

4.3.9 WOL_CON (WOL Control Register, Address: Register 0xA00A)

Table67. **WOL_CON**

Bit	Name	Default	Description	Access
15:8	RESV	0x0	Reserved	RO
7	SW_CLOSE_RGMII	0	1.disable rgmii interface 0.enable rgmii interface	RW
6	nPME_nINT_SEL	0	1: Pin 31 functions as nPME. 0: Pin 31 functions as nINT.	RW
5:4	RESV	0x0	Reserved	RW
3	WOL_EN	0	enable WOL.	RW
2:1	WOL_LTH_SEL	0x1	11: 672ms 10: 336ms 01: 168ms 00: 84ms	RW
0	WOL_INT_TYPE	0x0	1: nPME is level triggerd and active LOW; When nPME is LOW, EXT 0xA00A bit3, wol_en should be set to 0 to clear the nPME. 0: nPME is pulse triggered and active LOW, the purple width is controlled by wol_lth_sel[1:0].	RW

4.3.10 LED_COMCON (LED Common Control Register, Address: Register 0xA00B)

Table68. **LED_COMCON**

Bit	Name	Default	Description	Access
15	COL_BLK_SE	1	1 = when collision happens, and related LEDn cfg (n is 0/1/2)	RW

	L		register's bit3 led_col_blk_en is 1, LED blink at Blink Mode2; 0 = when collision happens, and related LEDn cfg (n is 0/1/2) register's bit3 led_col_blk_en is 0, LED blink at Blink Mode1. LED could blinks at different frequency in Blink Mode1 and Blink Mode2. Refer to EXT A00F[3:0] for the Blink Mode2 and Blink Mode1.	
14	JABBER_LED_DIS	1	1 = when 10Mb/s Jabber happens, LED will not blink;	RW
13	LPBK_LED_DIS	1	1 = In internal loopback mode, LED will not blink;	RW
12	DIS_LED_AN_TRY	0	1: LED will be ON when auto-negotiation is at LINK_GOOD_CHECK status, in which status, the link is not up already.	RW
11:9	RESV	0x0	Reserved	RO
8	LED_2_FORCE_EN	0	1 = enable LED2 force mode.	RW
7:6	LED_2_FORCE_MODE	0x0	Valid when bit8 is set. 11: force LED Blink at Blink Mode2 10: force LED Blink at Blink Mode1 01: force LED ON 00: force LED OFF LED could blinks at different frequency in Blink Mode1 and Blink Mode2. Refer to EXT A00F[3:0] for the Blink Mode2 and Blink Mode1.	RW
5	LED_1_FORCE_EN	0	1 = enable LED1 force mode.	RW
4:3	LED_1_FORCE_MODE	0x0	Valid when bit5 is set. Refer EXT A00B[7:6] for the force mode description.	RW
2	LED_0_FORCE_EN	0	1 = enable LED0 force mode.	RW
1:0	LED_0_FORCE_MODE	0x0	Valid when bit2 is set. Refer EXT A00B[7:6] for the force mode description.	RW

4.3.11 LED0_CON (LED0 Control Register, Address: Register 0xA00C)

Table69. **LED0_CON**

Bit	Name	Default	Description	Access
15:14	RSVD	0x0	Reserved	RW
13	LED_ACT_BLK_IND_0	0	When traffic is present, make LED0 BLINK no matter the previous LED0 status is ON or OFF, or make LED0 blink only when the previous	RW

			LED0 is ON.	
12	LED_FDX_ON_EN_0	0	1: If BLINK status is not activated, when PHY link up and duplex mode is full duplex, LED0 will be ON.	RW
11	LED_HDX_ON_EN_0	0	1: If BLINK status is not activated, when PHY link up and duplex mode is half duplex, LED0 will be ON.	RW
10	LED_TXACT_BLK_EN_0	1	1: If bit[13] is 1, or bit[13] is 0 and ON at certain speed or duplex more is/are activated, when PHY link up and TX is active, make LED0 blink at mode2.	RW
9	LED_RXACT_BLK_EN_0	1	1: If bit[13] is 1, or bit[13] is 0 and ON at certain speed or duplex more is/are activated, when PHY link up and RX is active, make LED0 blink at mode2.	RW
8	LED_TXACT_ON_EN_0	0	1: if BLINK status is not activated, when PHY link up and TX is active, make LED0 ON at least 10ms.	RW
7	LED_RXACT_ON_EN_0	0	1: if BLINK status is not activated, when PHY link up and RX is active, make LED0 ON at least 10ms.	RW
6	LED_GT_ON_EN_0	0	1: if BLINK status is not activated, when PHY link up and speed mode is 1000Mbps, make LED0 ON.	RW
5	LED_HT_ON_EN_0	0	1: if BLINK status is not activated, when PHY link up and speed mode is 100Mbps, make LED0 ON;	RW
4	LED_BT_ON_EN_0	1	1: if BLINK status is not activated, when PHY link up and speed mode is 10Mbps, make LED0 ON;	RW
3	LED_COL_BLK_EN_0	0	1: if PHY link up and collision happen, make LED0 BLINK;	RW
2	LED_GT_BLK_EN_0	0	1: if PHY link up and speed mode is 1000Mbps, make LED0 BLINK;	RW
1	LED_HT_BLK_EN_0	0	1: if PHY link up and speed mode is 100Mbps, make LED0 BLINK;	RW
0	LED_BT_BLK_EN_0	0	1: if PHY link up and speed mode is 10Mbps, make LED0 BLINK;	RW

4.3.12 LED1_CON (LED1 Control Register, Address: Register 0xA00D)

Table70. **LED1_CON**

Bit	Name	Default	Description	Access
15:14	RSVD	0x0	Reserved	RW
13	LED_ACT_BLK_IND_1	0	When traffic is present, make LED1 BLINK no matter the previous LED1 status is ON or OFF, or make LED1 blink only when the previous LED1 is ON.	RW
12	LED_FDX_ON_EN_1	0	1: If BLINK status is not activated, when PHY link up and duplex mode is full duplex, LED1 will be ON.	RW

11	LED_HDX_ON_EN_1	0	1: If BLINK status is not activated, when PHY link up and duplex mode is half duplex, LED1 will be ON.	RW
10	LED_TXACT_BLK_EN_1	1	1: If bit[13] is 1, or bit[13] is 0 and ON at certain speed or duplex more is/are activated, when PHY link up and TX is active, make LED1 blink at mode2.	RW
9	LED_RXACT_BLK_EN_1	1	1: If bit[13] is 1, or bit[13] is 0 and ON at certain speed or duplex more is/are activated, when PHY link up and RX is active, make LED1 blink at mode2.	RW
8	LED_TXACT_ON_EN_1	0	1: if BLINK status is not activated, when PHY link up and TX is active, make LED1 ON at least 10ms.	RW
7	LED_RXACT_ON_EN_1	0	1: if BLINK status is not activated, when PHY link up and RX is active, make LED1 ON at least 10ms.	RW
6	LED_GT_ON_EN_1	0	1: if BLINK status is not activated, when PHY link up and speed mode is 1000Mbps, make LED1 ON.	RW
5	LED_HT_ON_EN_1	0	1: if BLINK status is not activated, when PHY link up and speed mode is 100Mbps, make LED1 ON;	RW
4	LED_BT_ON_EN_1	1	1: if BLINK status is not activated, when PHY link up and speed mode is 10Mbps, make LED1 ON;	RW
3	LED_COL_BLK_EN_1	0	1: if PHY link up and collision happen, make LED1 BLINK;	RW
2	LED_GT_BLK_EN_1	0	1: if PHY link up and speed mode is 1000Mbps, make LED1 BLINK;	RW
1	LED_HT_BLK_EN_1	0	1: if PHY link up and speed mode is 100Mbps, make LED1 BLINK;	RW
0	LED_BT_BLK_EN_1	0	1: if PHY link up and speed mode is 10Mbps, make LED1 BLINK;	RW

4.3.13 LED2_CON (LED2 Control Register, Address: Register 0xA00E)

Table71. **LED2_CON**

Bit	Name	Default	Description	Access
15:14	RSVD	0x0	Reserved	RW
13	LED_ACT_BLK_IND_2	0	When traffic is present, make LED2 BLINK no matter the previous LED2 status is ON or OFF, or make LED2 blink only when the previous LED2 is ON.	RW
12	LED_FDX_ON_EN_2	0	1: If BLINK status is not activated, when PHY link up and duplex mode is full duplex, LED2 will be ON.	RW
11	LED_HDX_ON_EN_2	0	1: If BLINK status is not activated, when PHY link up and duplex mode is half duplex, LED2 will be ON.	RW
10	LED_TXACT_BLK_EN_2	1	1: If bit[13] is 1, or bit[13] is 0 and ON at certain speed or duplex more is/are activated, when PHY link up and TX is active, make	RW

			LED2 blink at mode2.	
9	LED_RXACT_BLK_EN_2	1	1: If bit[13] is 1, or bit[13] is 0 and ON at certain speed or duplex more is/are activated, when PHY link up and RX is active, make LED2 blink at mode2.	RW
8	LED_TXACT_ON_EN_2	0	1: if BLINK status is not activated, when PHY link up and TX is active, make LED2 ON at least 10ms.	RW
7	LED_RXACT_ON_EN_2	0	1: if BLINK status is not activated, when PHY link up and RX is active, make LED2 ON at least 10ms.	RW
6	LED_GT_ON_EN_2	0	1: if BLINK status is not activated, when PHY link up and speed mode is 1000Mbps, make LED2 ON.	RW
5	LED_HT_ON_EN_2	0	1: if BLINK status is not activated, when PHY link up and speed mode is 100Mbps, make LED2 ON;	RW
4	LED_BT_ON_EN_2	1	1: if BLINK status is not activated, when PHY link up and speed mode is 10Mbps, make LED2 ON;	RW
3	LED_COL_BLK_EN_2	0	1: if PHY link up and collision happen, make LED2 BLINK;	RW
2	LED_GT_BLK_EN_2	0	1: if PHY link up and speed mode is 1000Mbps, make LED2 BLINK;	RW
1	LED_HT_BLK_EN_2	0	1: if PHY link up and speed mode is 100Mbps, make LED2 BLINK;	RW
0	LED_BT_BLK_EN_2	0	1: if PHY link up and speed mode is 10Mbps, make LED2 BLINK;	RW

4.3.14 LED_BLCON (LED Blink Control Register, Address: Register 0xA00F)

Table72. **LED_BLCON**

Bit	Name	Default	Description	Access
15:7	RSVD	0x0	Reserved	RO
6:4	LED_DUTY	0x0	Select duty cycle of Blink: 000: 50% ON and 50% OFF; 001: 67% ON and 33% OFF; 010: 75% ON and 25% OFF; 011: 83% ON and 17% OFF; 100: 50% ON and 50% OFF; 101: 33% ON and 67% OFF; 110: 25% ON and 75% OFF; 111: 17% ON and 83% OFF.	RW
3:2	FREQ_SEL_2	0x1	Select frequency of Blink Mode2: 00: 2Hz; 01: 4Hz; 10: 8Hz;	RW

			11: 16Hz.	
1:0	FREQ_SEL_1	0x2	Select frequency of Blink Mode1: 00: 2Hz; 01: 4Hz; 10: 8Hz; 11: 16Hz.	RW

4.3.15 DRV_STR (Driver Strength Control Register, Address: Register 0xA010)

Table73. **DRV_STR**

Bit	Name	Default	Description	Access
15:13	RGMII_SW_DR_RX	0x3	Drive strenght of rx_clk pad. 3'b111: strongest; 3'b000: weakest.	RW
12	RGMII_SW_DR[2]	0	Bit 2 of Rgmii_sw_dr[2:0], refer to ext A010 [5:4]	RW
11	INT_OD_EN	1	1'b1: Interupt pin acts as a open drain pad 1'b0: Interupt pin acts as a normal output pad	RW
10	INT_ACT_HI	0	1'b1: Interupt acts as high active 1'b0: interupt acts as low active	RW
9:8	DR_SYNC_E	0x3	Drive strenght of SyncE pad. 2'b11: strongest; 2'b00: weakest	RW
7:6	DR_MDIO	0x3	Drive strenght of mdio pad. 2'b11: strongest; 2'b00: weakest	RW
5:4	RGMII_SW_DR[1:0	0x3	Bit 1 and 0 of Rgmii_sw_dr, Drive strenght of rxd/rx_ctl rgmii pad. 3'b111: strongest; 3'b000: weakest	RW POS
3:2	DR_INT_IO	0x3	Drive strenght of interrupt pad. 2'b11: strongest; 2'b00: weakest	RW
1:0	DR_LED	0x3	Drive strenght of led pad. 2'b11: strongest; 2'b00: weakest	RW

4.3.16 SyncE_CON (SyncE Control Register, Address: Register 0xA012)

Table74. **SyncE_CON**

Bit	Name	Default	Description	Access
15:8	RSVD	0x0	Reserved	RO
7	RSVD	1	Reserved	RW
6	EN_SYNC_E	1	enable SyncE clock output	RW
5	EN_SYNC_E_DURING_LNKDN	0	always output sync e clock even when link is down	RW

4	CLK_FRE_SEL	0	1'b1: output 125m clock; 1'b0: output 25m clock. It can control the output clock of internal 125M PLL and UTP recovered clock (CLK_SRC_SEL=0x0 or 0x1).	RW
3:1	CLK_SRC_SEL	0x4	select clock source of output clock. 3'b000： internal 125MHz PLL output clock 3'b001： UTP recovered RX clock 3'b010： Reserved. 3'b011： clock from digital (RGMII TX delayed clock, or debug clock out) 3'b100: reference 25MHz clock (default) 3'b101: 25MHz SSC.	RW
0	RSVD	0	Reserved	RO

4.4 MMD Extended Register

MMD Register Mapping and Definition,

Item	Address		Function	
	MMD	Offset	Register Name	Description
1	3	0x00	PCS_CON	PCS Control Register
2	3	0x01	PCS_STA	PCS status
3	3	0x14	EEE_CON	EEE Contrl Register
4	3	0x16	EEE_WERR	EEE Wake Error Register
5	7	0x3C	EEE_LA	EEE Local Ability Advertisement Register
6	7	0x3D	EEE_PA	EEE Link Partner Ability Register

4.4.1 PCS_CON (PCS Control Register, Address: MMD3 Register 0x00)

Table75. **PCS_CON**

Bit	Name	Default	Description	Access
15	PCS_RST	0	Setting this bit will set all PCS registers to their default states. This action also initiate a software reset as setting MII 0x0 bit15 and a reset as setting MMD1 0x0 bit15 and MMD7 0x0 bit15.	RW SC
14:11	RSVD	0x0	Reserved	RO
10	CLOCK_STOP PABLE	0	Not used.	RW SWC
9:0	RESERVED	0x0	Reserved	RO

4.4.2 PCS_STA (PCS Status Register, Address: MMD3 Register 0x01)

Table76. **PCS_STA**

Bit	Name	Default	Description	Access
15:12	RSVD	0x0	Reserved	RO
11	TX LPI_RC	0	TX LPI Received 1: TX PCS has received LPI 0: LPI not received	RO, LH
10	RX LPI_RC	0	RX LPI Received 1: RX PCS has received LPI 0: LPI not received	RO, LH
9	TX LPI_IND	0	TX LPI Indication 1: TX PCS is currently receiving LPI 0: TX PCS is not currently receiving LPI	RO
8	RX LPI_IND	0	RX LPI Indication 1: RX PCS is currently receiving LPI 0: RX PCS is not currently receiving LPI	RO
7:3	RSVD	0x0	Reserved	RO
2	PCSRX_LNK_ST	0	PCS status, latch low.	RO LL
1:0	RSVD	0x0	Reserved	RO

4.4.3 EEE_CON (EEE Control Register, Address: MMD3 Register 0x14)

Table77. **EEE_CON**

Bit	Name	Default	Description	Access
15:3	RSVD	0x0	Reserved	RO
2	1000BASE-T EEE	1	Always 1. EEE is supported for 1000BASE-T	RO
1	100BASE-TX EEE	1	Always 1. EEE is supported for 100BASE-TX	RO
0	RSVD	0	Reserved	RO

4.4.4 EEE_WERR (EEE Wake Error Register, Address: MMD3 Register 0x16)

Table78. **EEE_WERR**

Bit	Name	Default	Description	Access
15:0	Wake_ERR_CN	0x0	Count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type.	RO

4.4.5 EEE_LA (EEE Local Ability Register, Address: MMD7 Register 0x3C)

Table79. **EEE_LA**

Bit	Name	Default	Description	Access
15:03	RSVD	0x0	Reserved	RO
2	L_1000Base-T EEE	1	1: supported: 1000Base-T EEE 0: not supported: 1000Base-T EEE	RW
1	L_100Base-TX EEE	1	1: supported: 100Base-TX EEE 0: not supported: 100Base-TX EEE	RW
0	RSVD	0	Reserved	RO

4.4.6 EEE_PA (EEE Partner Ability Register, Address: MMD7 Register 0x3D)

Table80. **EEE_PA**

Bit	Name	Default	Description	Access
15:03	RSVD	0x0	Reserved	RO
2	LP 1000Base-T EEE	0	Link Partner of 1000Base-T EEE Capability. 1: Link Partner is capable of 1000Base-T EEE 0: Link Partner is not capable of 1000Base-T EEE	RO
1	LP 100Base-TX EEE	0	Link Partner of 100Base-TX EEE Capability. 1: Link Partner is capable of 100Base-TX EEE 0: Link Partner is not capable of 100Base-TX EEE	RO
0	RSVD	0	Reserved	RO

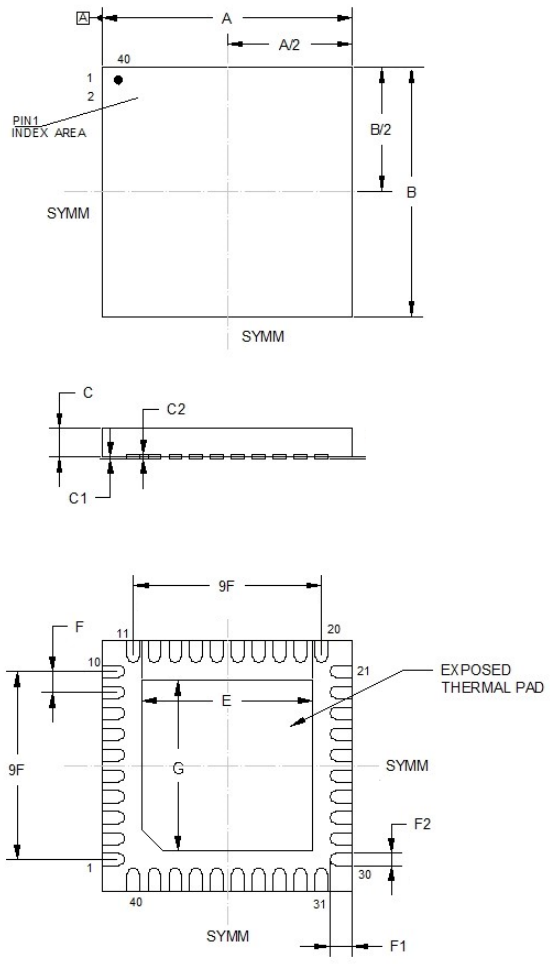
5 Environment

Table81. **Environment**

Attribute	Value
Moisture Sensitivity	Level 3
RoHS	RoHS2.0

6 Dimensions

6.1 QFN40 Dimensions



Dimension	Min.	Typ.	Max.
A	4.90	5.00	5.10
B	4.90	5.00	5.10
C	0.70	0.75	0.80
C1	--	--	0.05
C2	0.203REF		
E	3.30	3.40	3.50
G	3.30	3.40	3.50
F	0.40BSC		
F1	0.32	0.40	0.48
F2	0.15	0.20	0.25

(Unit: mm)

Figure 7. QFN-40 Dimension