



## DAP8201M(I) —A Fast Ethernet PHY Series



### Overview

The DAP8201M(I) is a single port Ethernet PHY, which has the characteristics of robustness, low power consumption and all physical layer functions. At the same time, it supports 10Base-Te, and 100Base TX, suitable for applications in security, communication and other electronic fields.

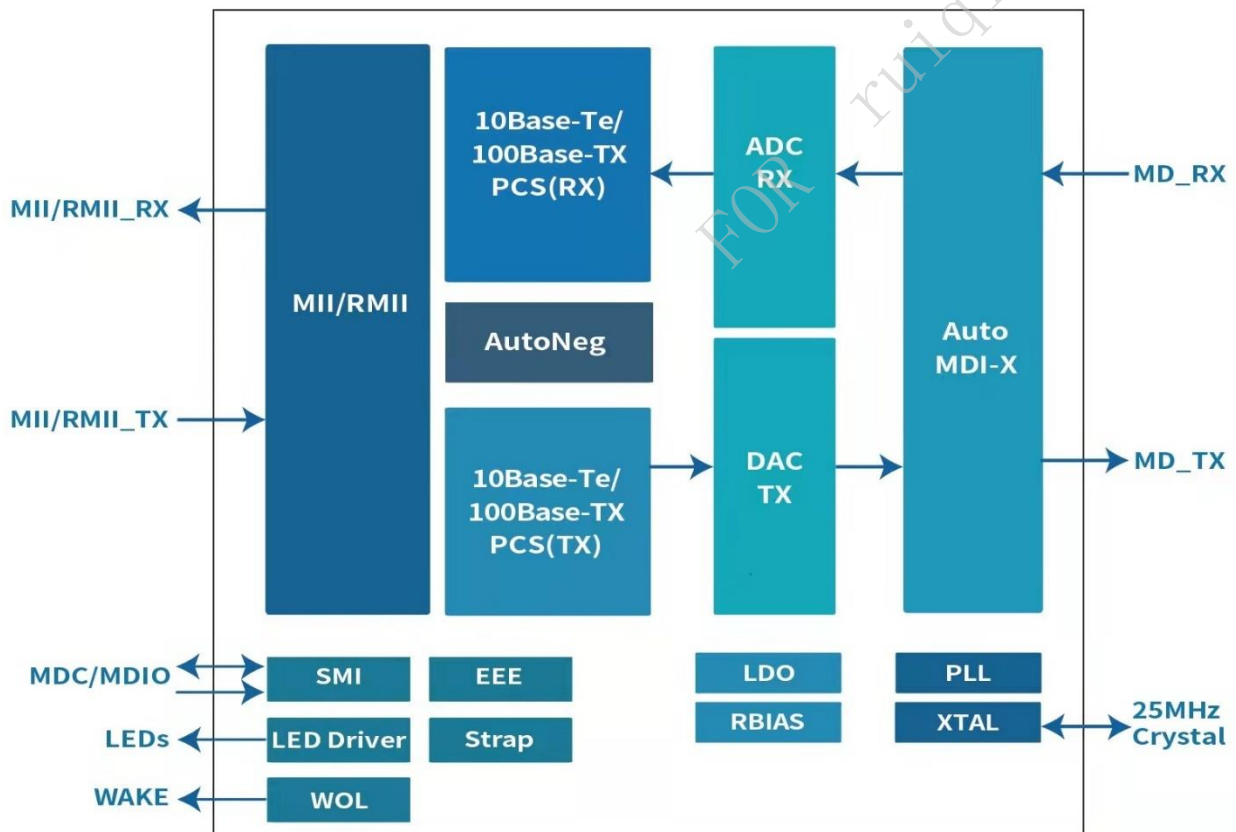
This device directly connects to the MAC layer through MII or RMI and supports MII/RMII to Copper.

The DAP8201M(I) is designed for easy implementation of 10/100Mbps Ethernet LANs. The MDI ports interfaces directly to CAT5 twisted pair media cable through the external transformer.

The DAP8201M(I) supports single 3.3V power supply.

Designed for low power, Wake-on-LAN can be used to lower system power consumption. The DAP8201M(I) is suitable for a wide range of applications.

### Block Diagram





### Key Features

- MII and RMII MAC Interface Options
- MII to Copper, RMII to Copper
- 100Base-TX/10Base-Te IEEE 802.3 Compliant
- IEEE 802.3az-2010 (EEE) Compliant
- WoL (Wake-on-LAN)
- Power Down Mode
- Auto-negotiation
- Auto-MDI-X
- Automatic Polarity Correction
- Supports Base Line Wander Correction
- Supports Interrupt Function
- 2 LEDs for Network Status
- Supports 25MHz External Crystal or 25M OSC Clock Input
- Output 50MHz Clock For MAC
- Integrate Linear Regulator 1.2V
- MAC I/O Voltage :3.3V
- 3.3V Single Power Supply
- Operation Temperature Range:
  - 0°C ~ +70°C
  - 40°C ~ +85°C
- Package: QFN 32-pin 5mm x 5mm

| Part Number | MI I to Copper | RMII to Copper | WoL | 100Base-TX | 10Base-Te | EEE | Integrated LDO | Temp.         | Package |
|-------------|----------------|----------------|-----|------------|-----------|-----|----------------|---------------|---------|
| DAP8201M    | •              | •              | •   | •          | •         | •   | •              | 0°C ~ +70°C   | QFN32   |
| DAP8201MI   | •              | •              | •   | •          | •         | •   | •              | -40°C ~ +85°C | QFN32   |

•: Support

### Applications

- Enterprise & SOHO
- LED Display
- Industrial Embedded Computing
- Wired and Wireless Communications Infrastructure
- Consumer Electronics





### Revision History

| Revision | Change Contents  | Prepared by | Revised Date |
|----------|--|-------------|--------------|
| 1.0      | First Issued   |             | 2022.03.05   |
| 1.1      | Correct some inexact description:<br>delete the internal power-on-reset; correct the absolute power supply voltage; correct pin name:V <sub>DD_1V</sub> ; etc.                             |             | 2022.04.16   |
| 1.2      | Add DAP8201MI<br>Correct description:<br>LED1, Link 100Mbps On;<br>LED_ACT_LEVEL_TH default value is 0xC<br>PKG_IPG_LENGTH default value is 0xC;<br>Table 15: bit 15 reset' s description; |             | 2022.05.31   |
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|          |  |             |              |



## Index

|  |           |
|--|-----------|
| OVERVIEW .....                             | 1         |
| BLOCK DIAGRAM.....                         | 1         |
| KEY FEATURES .....                         | 2         |
| REVISION HISTORY .....                     | 3         |
| INDEX .....                                | 4         |
| <b>1 PIN DEFINITION .....</b>              | <b>8</b>  |
| <b>2 ELECTRICAL CHARACTERISTICS .....</b>  | <b>11</b> |
| 2.1 ABSOLUTE MAXIMUM RATINGS .....         | 11        |
| 2.2 RECOMMENDED OPERATING CONDITIONS ..... | 11        |
| 2.3 POWER CONSUMPTION.....                 | 13        |
| 2.4 DC CHARACTERISTICS .....               | 13        |
| 2.5 TIMING CHARACTERISTICS .....           | 13        |
| 2.5.1 Reset Timing .....                   | 13        |
| 2.5.2 MII Interface Timing .....           | 14        |
| 2.5.3 RMII Interface Timing .....          | 16        |
| 2.6 REFERENCE CLOCK REQUIREMENTS .....     | 17        |
| <b>3 DETAIL DESCRIPTION .....</b>          | <b>18</b> |
| 3.1 BLOCK DIAGRAM .....                    | 18        |
| 3.2 FEATURE DESCRIPTION .....              | 18        |
| 3.2.1 WoL (Wake-on-LAN) .....              | 18        |
| 3.2.2 Auto-Negotiation.....                | 19        |
| 3.2.3 Auto-MDIX.....                       | 20        |
| 3.2.4 Automatic Polarity Correction .....  | 20        |
| 3.2.5 IEEE 802.3az-2010 EEE .....          | 20        |
| 3.2.6 UTP Ethernet .....                   | 20        |
| 3.2.7 MII Interface .....                  | 20        |



|          |   |           |
|----------|---|-----------|
| 3.2.8    | RMII Interface.....   | 21        |
| 3.2.9    | Reverse MII Interface.....  | 22        |
| 3.2.10   | Loopback Mode.....  | 22        |
| 3.2.11   | Hardware Bootstrap Configuration.....   | 23        |
| 3.2.12   | Reset.....  | 23        |
| 3.2.13   | Power Supply.....   | 23        |
| <b>4</b> | <b>REGISTERS.....</b>   | <b>25</b> |
| 4.1      | REGISTER MAPPING.....   | 25        |
| 4.2      | REGISTER ACCESS TYPES.....  | 25        |
| 4.3      | BASIC REGISTER.....   | 25        |
| 4.3.1    | BMCR(Basic Mode Control Register , Address: Register 0x0).....                  | 26        |
| 4.3.2    | BMSR (Basic Mode Status Register , Address: Register 0x1 ).....                 | 27        |
| 4.3.3    | PHYID1 (PHY Identifier Register #1 , Address: Register 0x2 ).....               | 28        |
| 4.3.4    | PHYID2 (PHY Identifier Register #2 , Address: Register 0x3 ).....               | 28        |
| 4.3.5    | ANAR (Auto-Negotiation Advertising , Address: Register 0x4 ).....               | 28        |
| 4.3.6    | ANLPA (Auto-Negotiation Link Partner Ability, Address: Register 0x5).....       | 29        |
| 4.3.7    | ANE (Auto-Negotiation Expansion Register Address: Register 0x6).....            | 30        |
| 4.3.8    | ANNPT (Auto-Negotiation Next Page Transmit Register Address: Register 7).....   | 30        |
| 4.3.9    | ANNPR (Auto-Negotiation Next Page Received Register Address: Register 0x8)..... | 31        |
| 4.3.10   | MSSR (Master-Slave Status Register Address: Register 0xA).....                  | 31        |
| 4.3.11   | MMD_AC (MMD Access Control; Address: Register 0xD).....                         | 32        |
| 4.3.12   | MMD_AADA (MMD Access Address Data, Address: Register 0xE).....                  | 32        |
| 4.3.13   | PHYCR (PHY Control Register, Address: Register 0x10).....                       | 32        |
| 4.3.14   | PHYSR (PHY Status Register, Address: Register 0x11).....                        | 33        |
| 4.3.15   | INTCR (Interrupt Control Register, Address: Register 0x12).....                 | 34        |
| 4.3.16   | INTSR (Interrupt Status Register, Address: Register 0x13).....                  | 35        |
| 4.3.17   | SPCR (Speed Configuration Register, Address: Register 0x14).....                | 35        |
| 4.3.18   | RECR (Receiver Error Counter Register, Address: Register 0x15).....             | 36        |



|            |   |           |
|------------|---|-----------|
| 4.3.19     | EXT_ADD (Extended Register Address Register, Address: Register 0x1E) .....      | 36        |
| 4.3.20     | EXT_DATA (Extended Register Data Register, Register 0x1F).....                  | 36        |
| <b>4.4</b> | <b>EXTENDED REGISTER .....</b>  | <b>36</b> |
| 4.4.1      | EXT_10M_PWRCON (10Mbps Power Control Register, Address: Register 0x200A) .....  | 36        |
| 4.4.2      | EXT_COMBO_CON (COMBO Control Register, Address: Register 0x4000) .....          | 36        |
| 4.4.3      | EXT_PIN_CON (PAD Control Register, Address: Register 0x4001).....               | 37        |
| 4.4.4      | EXT_COMBO2_CON (COMBO2 Control Register, Address: Register 0x4003) .....        | 37        |
| 4.4.5      | WoL_MAC_ADDH(WoL MAC Highest Address Register, Address: Register 0x4004).....   | 38        |
| 4.4.6      | WoL_MAC_ADDM(WoL MAC Middle Address Register, Address: Register 0x4005).....    | 38        |
| 4.4.7      | WoL_MAC_ADDL(WoL MAC Lowest Address Register, Address: Register 0x4006) .....   | 38        |
| 4.4.8      | PKG_ST_CON (Package Generation Selftest Control, Address: Register 0x40A0)..... | 38        |
| 4.4.9      | PKG_LEN(Package Generation Length, Address: Register 0x40A1) .....              | 39        |
| 4.4.10     | PKG_BS(Package Generation Burst Size, Address: Register 0x40A2).....            | 39        |
| 4.4.11     | PKG_RV_H(Package Receiver Valid High, Address: Register 0x40A3).....            | 39        |
| 4.4.12     | PKG_RV_L(Package Receiver Valid Low, Address: Register 0x40A4).....             | 40        |
| 4.4.13     | PKG_RX_OSH(Package Receiver OS High, Address: Register 0x40A5).....             | 40        |
| 4.4.14     | PKG_RX_OSL(Package Receiver OS Low, Address: Register 0x40A6).....              | 40        |
| 4.4.15     | PKG_RX_USH(Package Receiver US High, Address: Register 0x40A7) .....            | 40        |
| 4.4.16     | PKG_RX_USL(Package Receiver US Low, Address: Register 0x40A8).....              | 40        |
| 4.4.17     | PKG_RX_ERR(Package Receiver Error, Address: Register 0x40A9).....               | 40        |
| 4.4.18     | PKG_RX_OS_ERR(Package Receiver OS Error, Address: Register 0x40AA).....         | 41        |
| 4.4.19     | PKG_RX_FRM (Package Receiver Fragment, Address: Register 0x40AB).....           | 41        |
| 4.4.20     | PKG_RX_NOSFD (Package Receiver NOSFD, Address: Register 0x40AC).....            | 41        |
| 4.4.21     | PKG_TV_H(Package Transmit Valid High, Address: Register 0x40AD).....            | 41        |
| 4.4.22     | PKG_TV_L(Package Transmit Valid Low, Address: Register 0x40AE) .....            | 41        |
| 4.4.23     | PKG_TX_OSH(Package Transmit OS High, Address: Register 0x40AF).....             | 41        |
| 4.4.24     | PKG_TX_OSL(Package Transmit OS Low, Address: Register 0x40B0).....              | 42        |
| 4.4.25     | PKG_TX_USH(Package Transmit US High, Address: Register 0x40B1).....             | 42        |



|          |  |           |
|----------|--|-----------|
| 4.4.26   | PKG_TX_USL(Package Transmit US Low, Address: Register 0x40B2).....       | 42        |
| 4.4.27   | PKG_TX_ERR(Package Transmit Error, Address: Register 0x40B3) .....       | 42        |
| 4.4.28   | PKG_TX_OS_ERR(Package Transmit OS Error, Address: Register 0x40B4).....  | 42        |
| 4.4.29   | PKG_TX_FRM (Package Transmit Fragment, Address: Register 0x40B5) .....   | 42        |
| 4.4.30   | PKG_TX_NOSFD (Package Transmit NOSFD, Address: Register 0x40B6) .....    | 43        |
| 4.4.31   | PKG_CON2 (Package Generation Configure2, Address: Register 0x40B7).....  | 43        |
| 4.4.32   | PKG_CON3 (Package Generation Configure3, Address: Register 0x40B8).....  | 43        |
| 4.4.33   | PKG_CON4 (Package Generation Configure4, Address: Register 0x40B9).....  | 43        |
| 4.4.34   | PKG_CON5 (Package Generation Configure5, Address: Register 0x40BA) ..... | 43        |
| 4.4.35   | LED0_CON (LED0 Control Register, Address: Register 0x40C0).....          | 44        |
| 4.4.36   | LED_COMCON (LED Common Control Register, Address: Register 0x40C1) ..... | 44        |
| 4.4.37   | LED_BLCON (LED Blink Control Register, Address: Register 0x40C2) .....   | 45        |
| 4.4.38   | LED1_CON (LED1 Control Register, Address: Register 0x40C3).....          | 46        |
| <b>5</b> | <b>ENVIRONMENT .....</b>   | <b>47</b> |
| <b>6</b> | <b>DIMENSIONS .....</b>  | <b>48</b> |



# 1 Pin Definition

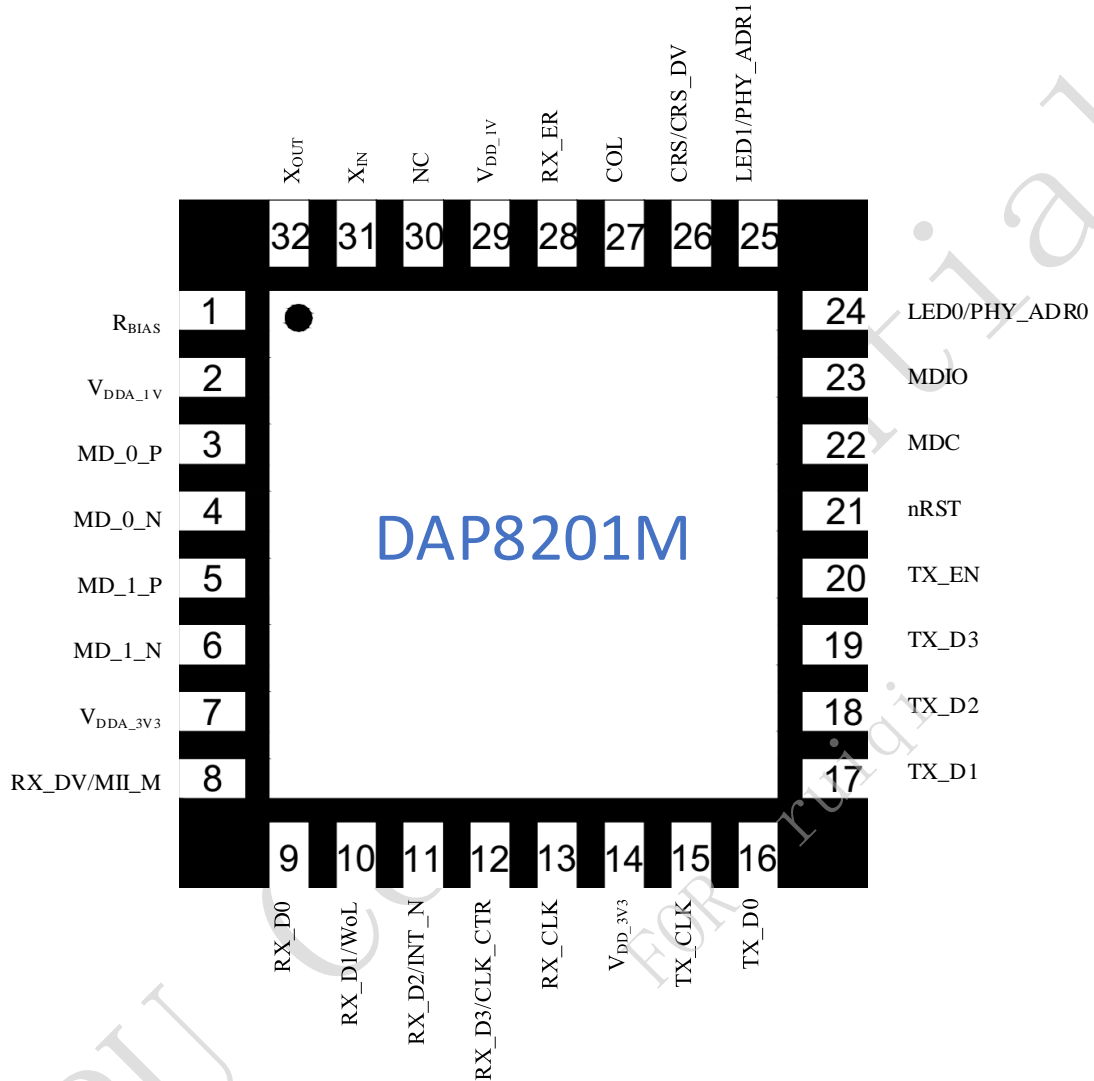


Figure 1 Package 32-Pin (Top View)

Table1. Pin Definition

| Pin Number              | Pin Name       | I/O   | Description  |
|-------------------------|----------------|-------|--|
| <b>POWER AND GROUND</b> |                |       |  |
| 2                       | $V_{DDA\_1V}$  | PWR/O | Power Output. Be sure to connect a 0.1 $\mu$ F and a 1.0uF ceramic capacitors for decoupling purposes. |
| 7                       | $V_{DDA\_3V3}$ | PWR   | 3.3V Analog Supply Input. A 1 $\mu$ F and 0.1 $\mu$ F capacitor are required to GND.                   |
| 14                      | $V_{DD\_3V3}$  | PWR   | 3.3V Digital Supply Input. Digital I/O power input for MII/RMII I/O, MDC/MDIO                          |





|                                  |                    |        |  |
|----------------------------------|--------------------|--------|--|
| 29                               | V <sub>DD_1V</sub> | PWR/O  | Power Output. Be sure to connect a 0.1μF and a 1.0uF ceramic capacitors for decoupling purposes.   |
| 33                               | EPAD               | GND    | Ground   |
| <b>REFERENCE CLOCK</b>           |                    |        |  |
| 31                               | X <sub>IN</sub>    | I      | Crystal/Oscillator Input: 25MHz oscillator or 25MHz crystal input  |
| 32                               | X <sub>OUT</sub>   | O      | Crystal Output: 25MHz crystal. Must be left floating if use oscillator.  |
| <b>MEDIA DEPENDENT INTERFACE</b> |                    |        |  |
| 3                                | MD_0_P             | I/O    | Differential Transmit/Receive. These differential IOs are automatically configured to either 10Base-Te or 100Base-TX signaling.<br>Auto-MDIX mode: it can be used as the Receive Input pair. There are 50Ω internal terminations on each pin, and due to this device incorporates voltage driven DAC, it does not require a center-tap power supply. |
| 4                                | MD_0_N             | I/O    |  |
| 5                                | MD_1_P             | I/O    | Differential Transmit/Receive. These differential IOs are automatically configured to either 10Base-Te or 100Base-TX signaling.<br>Auto-MDIX mode: it can be used as the Receive Input pair. There are 50Ω internal terminations on each pin, and due to this device incorporates voltage driven DAC, it does not require a center-tap power supply. |
| 6                                | MD_1_N             | I/O    |  |
| <b>MANAGEMENT INTERFACE</b>      |                    |        |  |
| 21                               | nRST               | I/HZ   | Reset: The active low RESET initializes or reinitializes the PHY, then all internal registers reinitialize to the default state.<br>Note: The reset signal must be held low at least 10ms.   |
| 22                               | MDC                | I/PU   | Management Data Clock  |
| 23                               | MDIO               | I/O/PU | Input/Output of Management Data.   |
| <b>MII/RMII Interface</b>        |                    |        |  |
| 15                               | TX_CLK             | I/O/PD | MII Mode: MII transmit clock, MII transmit clock provides a 25MHz reference clock for 100Mbps and a 2.5MHz reference clock for 10Mbps.<br>RMII Mode: RMII Reference Clock, 50MHz input or output for both transmit and receive.<br>The default direction is reference clock output mode if RX_D3/CLK_CTR pin floating.                               |
| 20                               | TX_EN              | I/PD   | Transmit enable: TX_EN is presented on the rising edge of the TX_CLK.<br>MII Mode: TX_EN indicates the presence of valid data inputs on TX_D[3:0]<br>RMII Mode: TX_EN indicates the presence of valid data inputs on TX_D[1:0]<br>TX_EN is an active high signal.  |
| 16                               | TX_D0              | I/PD   | Transmit Data.<br>The MAC will source TXD [0:3] synchronous with TXC when TX_EN is asserted.   |
| 17                               | TX_D1              | I/PD   |  |
| 18                               | TX_D2              | I/PD   |  |
| 19                               | TX_D3              | I/PD   |  |



| 13         | RX_CLK           | O/PD   | Receive clock: Receive Clock provides a 25MHz reference clock for 100Mbps speed and a 2.5MHz reference clock for 10Mbps speed, which is derived from the received data stream.  |       |            |            |   |   |     |   |   |             |   |   |  |   |   |  |
|------------|------------------|--|---|-------|------------|------------|---|---|-----|---|---|-------------|---|---|--|---|---|--|
| 8          | RX_DV/MII_M      | O/LI/PD  | Receive data valid: This pin indicates valid data is present on the RX_D[3:0] for MII mode.<br>Hardware Bootstrap for Media Mode Select with Pin13,<br>0: MII 1: RMII   |       |            |            |   |   |     |   |   |             |   |   |  |   |   |  |
|            |                  |  | <table border="1"> <thead> <tr> <th>Pin8</th> <th>Pin12</th> <th>Media Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>MII</td> </tr> <tr> <td>0</td> <td>1</td> <td>Reverse MII</td> </tr> <tr> <td>1</td> <td>0</td> <td>RMII2(TX_CLK outputs 50MHz Reference clock by default)</td> </tr> <tr> <td>1</td> <td>1</td> <td>RMII1(TX_CLK inputs 50MHz Reference clock)</td> </tr> </tbody> </table> | Pin8  | Pin12      | Media Mode | 0 | 0 | MII | 0 | 1 | Reverse MII | 1 | 0 | RMII2(TX_CLK outputs 50MHz Reference clock by default) | 1 | 1 | RMII1(TX_CLK inputs 50MHz Reference clock) |
|            |                  |  | Pin8  | Pin12 | Media Mode |            |   |   |     |   |   |             |   |   |  |   |   |  |
|            |                  |  | 0   | 0     | MII        |            |   |   |     |   |   |             |   |   |  |   |   |  |
| 0          | 1                | Reverse MII  |   |       |            |            |   |   |     |   |   |             |   |   |  |   |   |  |
| 1          | 0                | RMII2(TX_CLK outputs 50MHz Reference clock by default) |   |       |            |            |   |   |     |   |   |             |   |   |  |   |   |  |
| 1          | 1                | RMII1(TX_CLK inputs 50MHz Reference clock)             |   |       |            |            |   |   |     |   |   |             |   |   |  |   |   |  |
|            |                  |  |   |       |            |            |   |   |     |   |   |             |   |   |  |   |   |  |
|            |                  |  |   |       |            |            |   |   |     |   |   |             |   |   |  |   |   |  |
| 28         | RX_ER            | O/PD   | Receive error: This pin indicates that an error symbol has been detected within a received packet in both MII and RMII mode. In MII mode, RX_ER is asserted high synchronously to the rising edge of RX_CLK.  |       |            |            |   |   |     |   |   |             |   |   |  |   |   |  |
| 9          | RX_D0            | O/PD   | Receive data: Symbols received on the cable are decoded and presented on these pins synchronous to the rising edge of RX_CLK. When RX_DV is asserted, they contain valid data.  |       |            |            |   |   |     |   |   |             |   |   |  |   |   |  |
| 10         | RX_D1/WoL        | O/LI/PD  | Receive data: Symbols received on the cable are decoded and presented on these pins synchronous to the rising edge of RX_CLK. When RX_DV is asserted, they contain valid data.<br>Hardware Bootstrap:<br>0: Pin24 works as LED0<br>1: Pin24 works as WoL, must be pulled up.  |       |            |            |   |   |     |   |   |             |   |   |  |   |   |  |
| 11         | RX_D2/nINT       | O/OD/PD  | Receive data: Symbols received on the cable are decoded and presented on these pins synchronous to the rising edge of RX_CLK. When RX_DV is asserted, they contain valid data.<br>MII Mode: A RX_D[3:0] is received<br>RMII Mode:RX_D2 is used for interrupt pin.   |       |            |            |   |   |     |   |   |             |   |   |  |   |   |  |
| 12         | RX_D3/TX_CLK_CTR | O/LI/PD  | Receive data: Symbols received on the cable are decoded and presented on these pins synchronous to the rising edge of RX_CLK. When RX_DV is asserted, they contain valid data.<br>Hardware Bootstrap(RMII TX Clock control) :<br>0: RMII TX_CLK output,<br>1: RMII TX_CLK input   |       |            |            |   |   |     |   |   |             |   |   |  |   |   |  |
| 26         | CRS/CRS_DV       | O/PD   | MII Mode: Carrier Sense, asserted High to indicate the receive medium is non-idle.<br>RMII Mode: This signal combines the RMII Carrier Sense and Receive Data Valid indications.  |       |            |            |   |   |     |   |   |             |   |   |  |   |   |  |
| 27         | COL              | O/PD   | Collision detect:<br>In MII mode: For Full-Duplex mode, this pin is always low. In Half Duplex mode, this pin is asserted high only when both transmit and receive media are non-idle.  |       |            |            |   |   |     |   |   |             |   |   |  |   |   |  |
| <b>LED</b> |                  |  |   |       |            |            |   |   |     |   |   |             |   |   |  |   |   |  |
| 24         | LED0/PHY_ADR0    | O/LI/PD  | LED0, Link 10Mbps On, Active Blink.<br>Hardware Bootstrap: PHY Address [0]  |       |            |            |   |   |     |   |   |             |   |   |  |   |   |  |



|             |                   |         |   |
|-------------|-------------------|---------|---|
| 25          | LED1/PHY_ADR1     | O/LI/PD | LED1, Link 100Mbps On, Active Blink.<br>Hardware Bootstrap: PHY Address [1] |
| <b>MISC</b> |                   |         |   |
| 1           | R <sub>BIAS</sub> | I       | Bias Resistor Connection. External 2.49 kΩ 1% resistor connection to GND.   |
| 30          | NC                |         |   |

I: Input Signal

O: Output Signal

PWR: Power Supply

GND: Ground

EPAD: Exposed thermal PAD

PU: Pulled Up

PD: Pulled Down

LI: Latched Input during Power up or Reset

## 2 Electrical Characteristics

### 2.1 Absolute Maximum Ratings

Table2. Absolute Maximum Ratings

| Parameter                  | Symbol                          | Value |      |      | Unit | Notes                  |
|----------------------------|---------------------------------|-------|------|------|------|------------------------|
|                            |                                 | Min.  | Typ. | Max. |      |                        |
| Power Supply Voltage       | V <sub>D<sub>DA</sub>_1V</sub>  | -0.2  |      | 1.5  | V    | Analog supply voltage  |
|                            | V <sub>DD_1V</sub>              | -0.2  |      | 1.5  | V    | Digital supply voltage |
|                            | V <sub>D<sub>DA</sub>_3V3</sub> | -0.3  |      | 3.70 | V    | Analog supply voltage  |
|                            | V <sub>DD_3V3</sub>             | -0.3  |      | 3.70 | V    | Digital supply voltage |
| Storage temperature        | T <sub>STG</sub>                |       |      | 150  | °C   |                        |
| Lead Soldering Temperature | T <sub>Lead</sub>               |       |      | 260  | °C   | Soldering 10 seconds   |

### 2.2 Recommended Operating Conditions

Table3. Recommended Operating Conditions

| Parameter      | Symbol                          | Value |      |      | Unit | Notes |
|----------------|---------------------------------|-------|------|------|------|-------|
|                |                                 | Min.  | Typ. | Max. |      |       |
| Supply Voltage | V <sub>D<sub>DA</sub>_1V</sub>  | 1.10  | 1.20 | 1.30 | V    |       |
|                | V <sub>DD_1V</sub>              | 1.10  | 1.20 | 1.30 | V    |       |
|                | V <sub>D<sub>DA</sub>_3V3</sub> | 2.97  | 3.30 | 3.63 | V    |       |
|                | V <sub>DD_3V3</sub>             | 2.97  | 3.30 | 3.63 | V    |       |



| Parameter                                 | Symbol              | Value |      |      | Unit | Notes                          |
|---|---------------------|-------|------|------|------|--------------------------------|
|   |                     | Min.  | Typ. | Max. |      |                                |
| Operating Junction Temperature            | T <sub>JUNC</sub>   |       |      | 125  | °C   |                                |
| Operation temperature                     | T <sub>OPR</sub>    | 0     | 25   | 70   | °C   |                                |
| Max. Junction Temperature                 | T <sub>JUNC</sub>   | 0     |      | 125  | °C   |                                |
| Operation temperature                     | T <sub>OPR</sub>    | 0     | 25   | 70   | °C   | DAP8201M                       |
|   |                     | -40   | 25   | 85   | °C   | DAP8201MI                      |
| Thermal resistance - junction to ambient  | θ <sub>JA</sub>     |       | 37.8 |      | °C/W | JEDEC with no air flow TA=25°C |
| Thermal resistance - junction to board    | θ <sub>JB</sub>     |       | 16.1 |      | °C/W | JEDEC with no air flow         |
| Thermal resistance - junction to top case | θ <sub>JC-Top</sub> |       | 34.8 |      | °C/W | JEDEC with no air flow         |



### 2.3 Power Consumption

Table4. Power consumption

| Condition    | MII    | RMII   | Unit |
|--------------|--------|--------|------|
| Reset        | 16.5   | 16.5   | mW   |
| Power Down   | 18.48  | 18.48  | mW   |
| Sleep Mode   | 20.13  | 20.13  | mW   |
| Active       | 147.84 | 145.2  | mW   |
| Link 10M     | 79.53  | 77.88  | mW   |
| Link 100M    | 217.47 | 201.3  | mW   |
| Traffic 10M  | 135.3  | 133.65 | mW   |
| Traffic 100M | 212.52 | 189.35 | mW   |

The power consumption is measured under room temperature with typical process DUT.

### 2.4 DC Characteristics

Table5. DC Characteristics

| Parameter                      | Symbol          | Value |      |      | Unit | Notes                     |
|--------------------------------|-----------------|-------|------|------|------|---------------------------|
|                                |                 | Min.  | Typ. | Max. |      |                           |
| 3.3V High-level input voltage  | V <sub>IH</sub> | 2.0   |      |      | V    | V <sub>DD_3V3</sub> =3.3V |
| 3.3V Low-level input voltage   | V <sub>IL</sub> |       |      | 0.8  | V    | V <sub>DD_3V3</sub> =3.3V |
| 3.3V High-level output voltage | V <sub>OH</sub> | 2.4   |      |      | V    | V <sub>DD_3V3</sub> =3.3V |
| 3.3V Low-level output voltage  | V <sub>OL</sub> |       |      | 0.4  | V    | V <sub>DD_3V3</sub> =3.3V |

### 2.5 Timing Characteristics

#### 2.5.1 Reset Timing

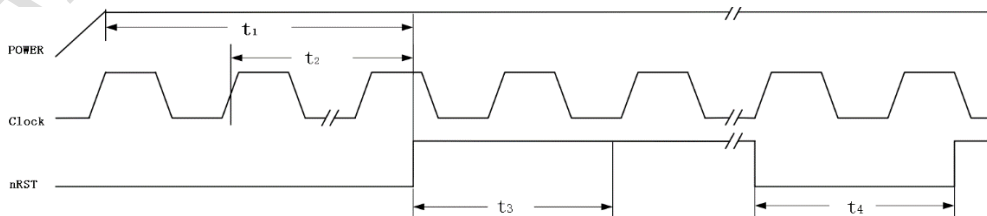


Figure 1. Reset Timing

Table6. Reset Timing



| Parameter                                   | Symbol | Value |      |      | Unit |
|---|--------|-------|------|------|------|
|   |        | Min.  | Typ. | Max. |      |
| Reset assert time after power on            | $t_1$  | 100   |      |      | ms   |
| Reset assert time after clock ready         | $t_2$  | 10    |      |      | ms   |
| Reset de-assert time after power on         | $t_3$  | 5     |      |      | ms   |
| Minimum reset pulse during normal operation | $t_4$  | 10    |      |      | ms   |

### 2.5.2 MII Interface Timing



Figure 2. 10Mbps/100Mbps MII Transmit Timing

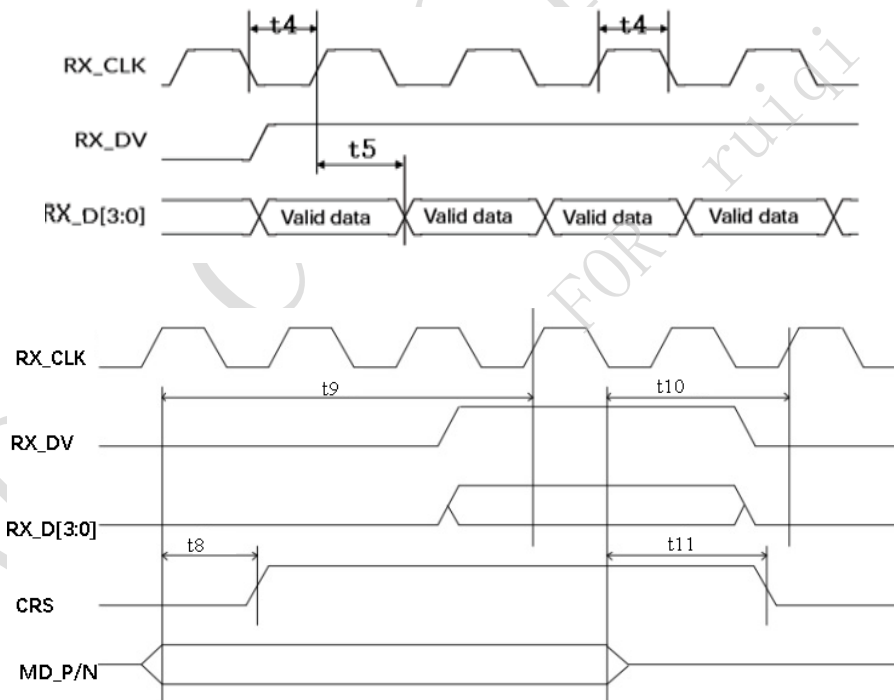


Figure 3. 10Mbps/100Mbps MII Receive Timing

Table7. 100Mbps MII Timing



| Parameter   | Symbol | Value |      |      | Unit | Notes            |
|---|--------|-------|------|------|------|------------------|
|   |        | Min.  | Typ. | Max. |      |                  |
| TX_CLK high/low time                                | t1     | 14    | 20   | 26   | ns   | 100Mbps MII mode |
| TX_D[3:0], TX_EN data setup to TX_CLK               | t2     | 10    |      |      | ns   |                  |
| TX_D[3:0], TX_EN data hold from TX_CLK              | t3     | 0     |      |      | ns   |                  |
| RX_CLK high/low time                                | t4     | 14    | 20   | 26   | ns   |                  |
| RX_CLK to RX_D[3:0], RX_DV, RX_ER delay             | t5     | 10    |      | 30   | ns   |                  |
| TX_EN Sampled to CRS High                           | t6     |       |      | 40   | ns   |                  |
| TX_EN Sampled to CRS Low                            | t7     |       |      | 160  | ns   |                  |
| Receive Frame to CRS High                           | t8     |       |      | 130  | ns   |                  |
| Receive Frame to sampled clock edge of RX_DV        | t9     |       |      | 150  | ns   |                  |
| End of Receive Frame to CRS Low                     | t10    |       |      | 240  | ns   |                  |
| End of Receive Frame to sampled clock edge of RX_DV | t11    | 10    |      | 120  | ns   |                  |

Table8. 10Mbps MII Timing

| Parameter   | Symbol | Value |      |      | Unit | Notes           |
|---|--------|-------|------|------|------|-----------------|
|   |        | Min.  | Typ. | Max. |      |                 |
| TX_CLK high/low time                                | t1     | 140   | 200  | 260  | ns   | 10Mbps MII mode |
| TX_D[3:0], TX_EN data setup to TX_CLK               | t2     | 5     |      |      | ns   |                 |
| TX_D[3:0], TX_EN data hold from TX_CLK              | t3     | 0     |      |      | ns   |                 |
| RX_CLK high/low time                                | t4     | 160   | 200  | 240  | ns   |                 |
| RX_CLK to RX_D[3:0], RX_DV, RX_ER delay             | t5     | 100   |      | 300  | ns   |                 |
| TX_EN Sampled to CRS High                           | t6     |       |      | 400  | ns   |                 |
| TX_EN Sampled to CRS Low                            | t7     |       |      | 2000 | ns   |                 |
| Receive Frame to CRS High                           | t8     |       |      | 2000 |      |                 |
| Receive Frame to sampled clock edge of RX_DV        | t9     |       |      | 3200 |      |                 |
| End of Receive Frame to CRS Low                     | t10    |       |      | 1000 |      |                 |
| End of Receive Frame to sampled clock edge of RX_DV | t11    | 10    |      | 1000 | ns   |                 |
| TX_EN Sampled to CRS Low                            | t7     |       |      | 2000 | ns   |                 |



### 2.5.3 RMII Interface Timing



Figure 4. RMII Transmit Timing

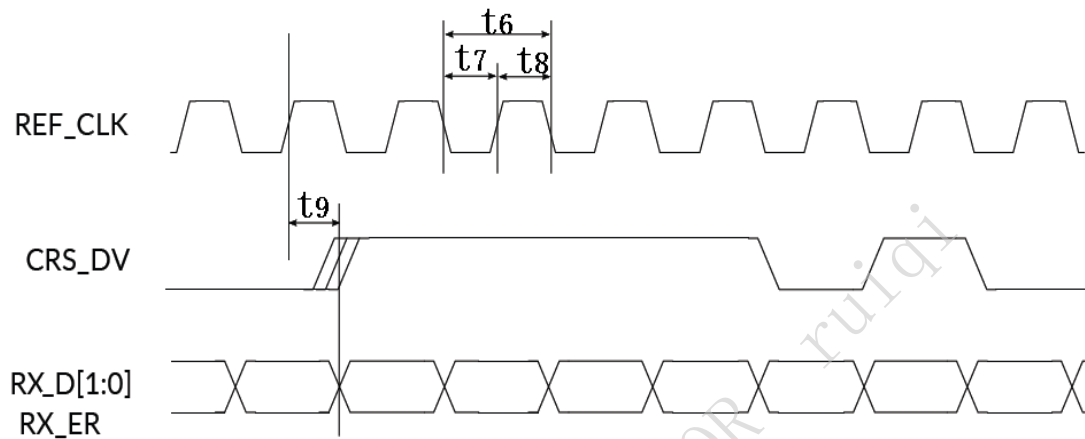


Figure 5. RMII Receive Timing

Table9. RMII Timing

| Parameter  | Symbol | Value |      |      | Unit | Notes |
|--|--------|-------|------|------|------|-------|
|  |        | Min.  | Typ. | Max. |      |       |
| REF_CLK(TX_CLK) clock period                               | t1, t6 |       | 20   |      | ns   |       |
| REFCLK(TX_CLK) clock duty cycle                            |        | 35    | 50   | 65   | %    |       |
| TX_D[1:0], TX_EN, data setup to REF_CLK(TX_CLK) rising     | t4     | 4     |      |      | ns   |       |
| TX_D[1:0], TX_EN, data hold from REF_CLK(TX_CLK) rising    | t5     | 2     |      |      | ns   |       |
| RX_D[1:0], CRS_DV output delay from REF_CLK(TX_CLK) rising | t9     | 2     |      |      | ns   |       |

Table10. 10Mbps RMII Timing

| Parameter            | Symbol | Value |      |      | Unit | Notes  |
|----------------------|--------|-------|------|------|------|--------|
|                      |        | Min.  | Typ. | Max. |      |        |
| TX_CLK high/low time | t1     | 140   | 200  | 260  | ns   | 10Mbps |





| Parameter                               | Symbol | Value |      |      | Unit | Notes    |
|---|--------|-------|------|------|------|----------|
|   |        | Min.  | Typ. | Max. |      |          |
| TX_D[3:0], TX_EN data setup to TX_CLK   | t2     | 10    |      |      | ns   | MII mode |
| TX_D[3:0], TX_EN data hold from TX_CLK  | t3     | 1     |      |      | ns   |          |
| RX_CLK high/low time                    | t4     | 160   | 200  | 240  | ns   |          |
| RX_CLK to RX_D[3:0], RX_DV, RX_ER delay | t5     | 100   |      | 300  | ns   |          |

## 2.6 Reference Clock Requirements

Table11. Crystal Specification

| Parameter           | Value |      |      | Unit     | Notes |
|---------------------|-------|------|------|----------|-------|
|                     | Min.  | Typ. | Max. |          |       |
| Frequency           |       | 25   |      | MHz      |       |
| Frequency Stability | -50   |      | 50   | ppm      |       |
| ESR                 |       |      | 50   | $\Omega$ |       |
| Drive Level         |       |      | 0.5  | mW       |       |

Table12. Oscillator Specification

| Parameter             | Value |      |      | Unit | Notes                           |
|-----------------------|-------|------|------|------|---------------------------------|
|                       | Min.  | Typ. | Max. |      |                                 |
| Frequency             |       | 25   |      | MHz  |                                 |
| Frequency Stability   | -50   |      | 50   | ppm  |                                 |
| Rise/Fall Time        |       |      | 6    | ns   | 10% - 90%                       |
| Cycle to Cycle Jitter |       |      | 200  | ps   | short term (peak to peak value) |
| Duty Cycle            | 40    |      | 60   | %    |                                 |
| V <sub>IH</sub>       | 1.4   |      | 3.6  | V    |                                 |
| V <sub>IL</sub>       |       |      | 0.4  | V    |                                 |



### 3 Detail Description

#### 3.1 Block Diagram

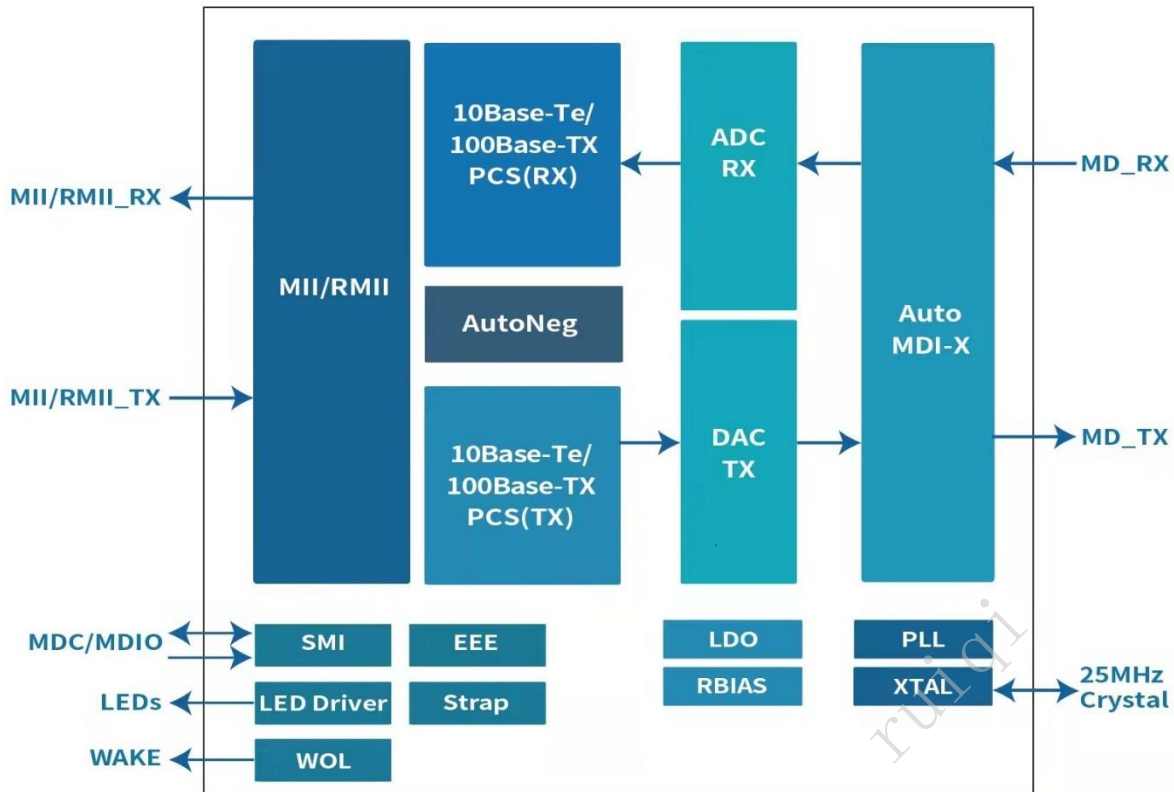


Figure 6. Functional Block Diagram

#### 3.2 Feature Description

##### 3.2.1 WoL (Wake-on-LAN)

Wake-on-LAN provides a mechanism to detect dedicated frames and inform the connected MAC through either a register status change, WoL indication, or an interrupt flag. The connected devices (MAC) placed above the Physical Layer to operate in a low power mode until special frames are detected. Supported WoL types include: Magic Packet.

When configured for Wake-on-LAN mode, the DAP8201M(I) will check all incoming frames to identify the Magic Packet frame.

A Magic Packet frame must also meet the basic requirements for the Ethernet Frame.



The specific Magic Packet sequence consists of 16 duplications of the IEEE address of this node, with no breaks or interruptions. This sequence can be located anywhere within the packet but must be preceded by a synchronization stream. The synchronization stream is defined as 6 bytes of 0xFF.

Table13. Magic Packet Structure

|                                       |
|---------------------------------------|
| <b>Destination</b><br>(6 bytes)       |
| <b>Source</b><br>(6 bytes)            |
| <b>MISC</b><br>(X bytes, X >= 0)      |
| <b>FFFFFFFFFFFF</b><br>(6 bytes)      |
| <b>Destination*16</b><br>(6*16 bytes) |
| <b>MISC</b><br>(X bytes, X >= 0)      |
| <b>CRC</b><br>(4 bytes)               |

EXT 0x4004, 0x4005 and 0x4006 are the 48-bit MAC address registers.

EXT 0x4000 bit2 controls the WoL mechanism.

RX\_D[1] just controls pin24 LED0 working as WoL interrupt. When the pad RX\_D1 is externally pulled up, pin24 will work as WoL interrupt.

If EXT 0x4003 bit7 is 0, the dedicated WoL interrupt is programmed to a level, otherwise, it's programmed to a pulse; either is active low. When it's programmed to a pulse, the pulse width can be programmed via EXT 0x4003 bit9:8.

WoL interrupt is also wire-and to general PHY interrupt RX\_D2\_INT when the bit6 INT\_WoL in Interrupt enable register (Basic Register 0x12) is set to 1. If the general PHY interrupt is triggered by WoL, it can be cleared by reading MII register 0x13 bit6.

NOTE:

When general PHY interrupt is used to monitor WoL interrupt, EXT 0x4003 bit7 should be 1, otherwise, the general PHY interrupt can't be read cleared.

Because PHY requires to receive packets from the line side, PHY cannot be powered down. If the link partner supports Energy Efficient Ethernet function, both ends can use EEE mode to save more power.

MII register 0x0 bit10 ISOLATE: When this bit is set to 1, the MII/RMII output pins are High Z. The MII/RMII inputs are ignored.

### 3.2.2 Auto-Negotiation

DAP8201M(I) supports Auto-Negotiation function which is defined in 802.3u. Auto-Negotiation function is to exchange information between two devices that share a link segment and to automatically configure both devices to take maximum advantage of their abilities.

The basic mechanism to achieve Auto-Negotiation is to pass information encapsulated within a burst of closely spaced



link integrity test pulses that individually meet the 10Base-Te Transmitter Waveform for Link Test Pulse. This burst of pulses is referred to as a Fast Link Pulse Burst.

The Auto-Negotiation function allows the devices to switch between the various operational modes in an ordered fashion, permits management to disable or enable the Auto-Negotiation function, and allows management to select a specific operational mode. The Auto-Negotiation function also provides a Parallel Detection function to allow 10Base-Te and 100Base-TX compatible devices to be recognized, even though they may not provide Auto-Negotiation.

### 3.2.3 Auto-MDIX

The function implements crossover detection automatically for MDI/MDIX cables which eases connection process. Auto-MDIX is enabled by default and can be configured via register (register 28, page 0), bits [2:1].

### 3.2.4 Automatic Polarity Correction

The DAP8201M(I) also implements polarity auto correction when cable happens to have wrong polarity connected when working at 10Base-Te mode. DAP8201M(I) will detect the polarity of Normal Link Pulse to determine the polarity of cable.

### 3.2.5 IEEE 802.3az-2010 EEE

The DAP8201M(I) supports IEEE 802.3az-2010(EEE: Energy Efficient Ethernet). EEE defines a negotiation method to enable link partners to decide whether EEE is supported.

Based on link utilization efficiency and EEE protocol, the transitions would work in different mode. When no packets are being transmitted, DAP8201M(I) would work in Low Power Idle mode to save power. As soon as packets to be transmitted, DAP8201M(I) returns to normal mode, and this doesn't impact the link status and dropping frames.

### 3.2.6 UTP Ethernet

DAP8201M(I) supports the 100Base-TX and 10Base-Te standard as defined by the IEEE 802.3 standard.

In 100M mode, the PHY will use two pairs MDI channels for communication. The communicated data are encoded/decoded in 4B/5B.

In 10M mode, the PHY will also use two pairs MDI channels for communication. The communicated data are encoded/decoded in Manchester.

### 3.2.7 MII Interface

The Media Independent Interface is a synchronous 4-bit wide nibble data interface that connects the PHY to the MAC in 100Base-TX and 10Base-Te modes. The MII is compliant with IEEE 802.3-2002 clause 22.

Additionally, the MII interface includes the carrier sense signal (CRS), as well as a collision detect signal (COL). The CRS signal asserts to indicate the reception or transmission of data. The COL signal asserts as an indication of a collision which can occur during Half-Duplex mode when both transmit and receive operations occur simultaneously.

Transmission: The MAC asserts the TX\_EN signal firstly, then changes byte data into 4-bit and transmits them to the



PHY via TX\_D[3:0]. The PHY will sample TX\_D[3:0] synchronously with TX\_CLK – the transmit clock signal supplied by the PHY.

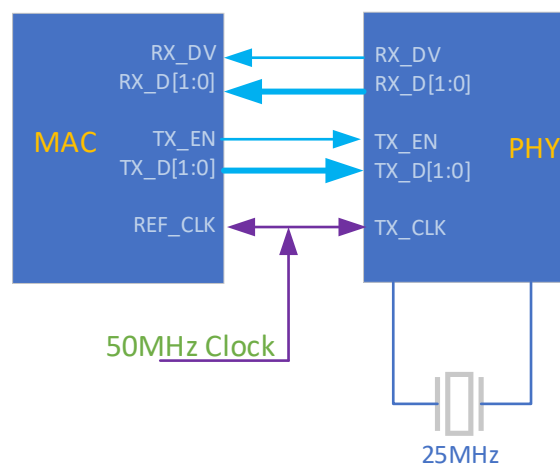
Reception: The PHY asserts the RXDV signal firstly. It transmits the received data RX\_D[3:0] clocked by RX\_CLK. CRS and COL signals are used for collision detection and handling.



### 3.2.8 RMII Interface

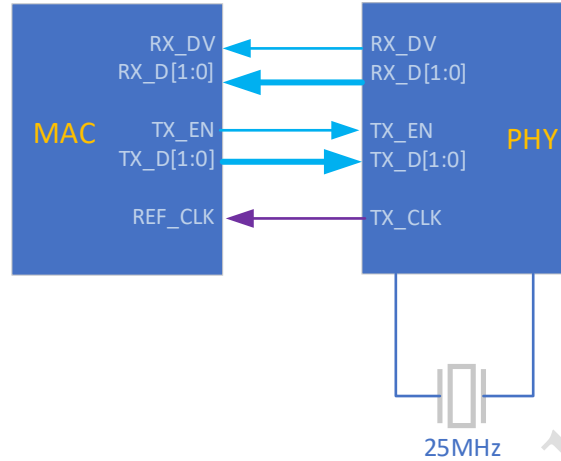
The DAP8201M(I) incorporates the Reduced Media Independent Interface (RMII) as specified in the RMII specification from the RMII consortium. The purpose of this interface is to provide a reduced pin count alternative to the IEEE 802.3u MII as specified in Clause 22. Architecturally, the RMII specification provides an additional reconciliation layer on either side of the MII, but it can be implemented in the absence of an MII.

1. RMII1 mode: This is fully conforming to RMII standard. DAP8201M(I) can use clock from TX\_CLK as reference clock for internal PLL. Configure bit 6 of extended register (address 0x50) to 1 to enable: not need 25MHz crystal at XI/XO.





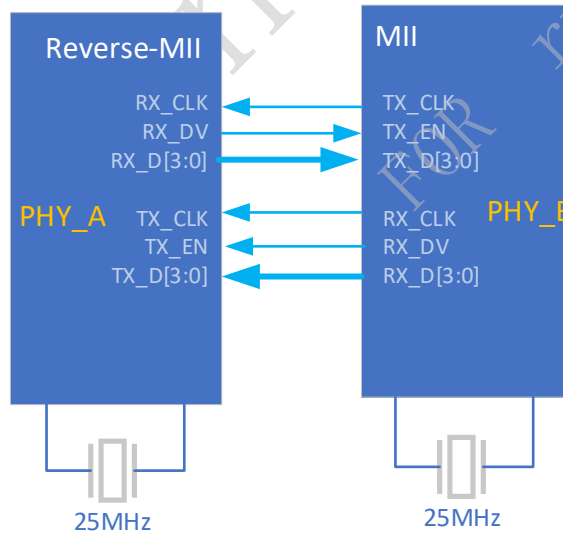
- 2. RMII2 mode: TX\_CLK will output 50MHz to MAC, this can save one 50MHz clock.



### 3.2.9 Reverse MII Interface

DAP8201M(I) supports reverse media independent interface. The only difference is the direction of TX\_CLK and RX\_CLK. For MII, TX\_CLK and RX\_CLK are output; for Reverse MII, TX\_CLK and RX\_CLK are input.

In Reverse MII mode, two PHYs are connected back-to-back via the MII interface to realize a repeater function on the physical layer.



### 3.2.10 Loopback Mode

There are several options for loopback mode that test and verify various functional blocks within the PHY. Enabling loopback mode allows in-circuit testing of the digital and analog data paths. Generally, the DAP8201M(I) may be configured to 3 loopback modes.



| Loopback Mode     | Description  |
|-------------------|--|
| Internal Loopback | When BMCR register field Loopback is set to “1”, data sent through DAC to ADC directly.  |
| External Loopback | An external loopback stub allows testing the complete data path without the need of a link partner. In this case it seems the data send through MII/RMII TX interface with be forwarded to MII/RMII RX interface through MDI interface |
| Remote Loopback   | When Remote_loopback bit of extended register(0x4000) is set to “1”, data transmitted from MII/RMII tx interface will route back to MII/RMII rx interface. This checks if MII/RMII works correctly for remote link.                    |

### 3.2.11 Hardware Bootstrap Configuration

The MII/RMII mode, and PHY address can be set by hardware. These configurations are setup through dedicated IO pin with external pullup/pulldown resistor. When power on reset is de-asserted, the hardware circuit will sample values on these dedicated IO pin.

Table14. Hardware Bootstrap

| Function                                 | Pin Number | Pin Name      | Description  |
|--|------------|---------------|--|
| Hardware Bootstrap for Media Mode Select | 8          | RX_DV/MII_M   | Pin8   Pin12   Media Mode                                      |
|  |            |               | 0   0   MII  |
|  |            |               | 0   1   Reverse MII  |
|  |            |               | 1   0   RMII2(TX_CLK outputs 50MHz Reference clock by default) |
|  |            |               | 1   1   RMII1(TX_CLK inputs 50MHz Reference clock)             |
| LED/WOL                                  | 10         | RX_D1/WoL     | 0: pin24 works as LED0<br>1: pin24 works as WoL                |
| PHY Address                              | 24         | LED0/PHY_ADR0 | Pin25   Pin24   PHY Address                                    |
|  |            |               | 0   0   00000  |
|  |            |               | 0   1   00001  |
|  |            |               | 1   0   00010  |
|  |            |               | 1   1   00011  |
|  | 25         | LED1/PHY_ADR1 |  |

### 3.2.12 Reset

There are two types of reset operation: Hardware Reset and Software Reset.

Hardware Reset: A hardware reset is implemented by asserting the nRST pin with low level: at least 10ms. All registers will be reset to default values and the hardware configuration will be re-latched.

Software Reset: A software reset is accomplished by writing BMC-C[15] Reset register to 1. All registers will be reset to default values and the hardware configuration will not be re-latched. Software need wait 100us to start other SMI operation.

### 3.2.13 Power Supply

DAP8201M(I) integrates the internal linear regulator and needs to supply a single 3.3V power source.



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## 4 Registers

### 4.1 Register mapping

The DAP8201M(I) includes 2 register groups.

|   | Register Group  | Description  |
|---|-----------------|--|
| 1 | Basic Register  | Basic Register based on IEEE802.3                  |
| 2 | Extend Register | Extend Register based on Extended Register Mapping |

Note: Basic Register is same to MII Register.

### 4.2 Register Access Types

| Type | Description  |
|------|--|
| RW   | Read and write   |
| RO   | Read only.   |
| SC   | Self-clear.<br>If default value is '0' ('1'), writing a '1' ('0') to this register field causes the function to be activated immediately, and then the field will be automatically cleared to '0' ('1'). |
| RC   | Read clear.  |
| SWC  | Software reset to 0.   |
| SWS  | Software reset to 1.   |
| PS   | Default value depends on power on strapping.   |
| LH   | Latch high.  |
| LL   | Latch Low.   |

### 4.3 Basic Register

| Item | Address | Function      |                                       |
|------|---------|---------------|---------------------------------------|
|      | Offset  | Register Name | Description                           |
| 1    | 0x0     | BMCR          | Basic Mode Control                    |
| 2    | 0x1     | BMSR          | Basic Mode Status                     |
| 3    | 0x2     | PHYID1        | PHY Identifier Register #1            |
| 4    | 0x3     | PHYID2        | PHY Identifier Register #2            |
| 5    | 0x4     | ANAR          | Auto-Negotiation Advertisement        |
| 6    | 0x5     | ANLPA         | Auto-Negotiation Link Partner Ability |
| 7    | 0x6     | ANE           | Auto-Negotiate Expansion              |
| 8    | 0x7     | ANNPT         | Auto-Negotiate Next Page Transmit     |
| 9    | 0x8     | ANNPR         | Auto-Negotiate Next Page Receive      |
| 10   | 0xA     | MSSR          | Master-Slave Status Register          |
| 11   | 0xD     | MMD_AC        | MMD Access Control                    |
| 12   | 0xE     | MMD_AADA      | MMD Access Address and Data           |



|    |      |          |                                    |
|----|------|----------|------------------------------------|
| 13 | 0x10 | PHYCR    | PHY Control Register               |
| 14 | 0x11 | PHYSR    | PHY Status Register                |
| 15 | 0x12 | INTCR    | Interrupt Control Register         |
| 16 | 0x13 | INTSR    | Interrupt Status Register          |
| 17 | 0x14 | SPCR     | Speed Configuration Register       |
| 18 | 0x15 | RECR     | Receiver Error Counter Register    |
| 19 | 0x1E | EXT_ADD  | Extended Register Address Register |
| 20 | 0x1F | EXT_DATA | Extended Register Data Register    |

#### 4.3.1 BMCR(Basic Mode Control Register, Address: Register 0x0)

Table15. BMCR

| Bit | Name     | Default | Description   | Access |
|-----|----------|---------|---|--------|
| 15  | Reset    | 0       | Reset.<br>1: PHY reset<br>0: Normal operation<br>Software Reset. Writing a '1' to this bit to reset the PHY states machine.<br>Register 0 (BMCR) and register 1 (BMSR) will return to default values once the reset operation is done.                                  | RW, SC |
| 14  | Loopback | 0       | Internal Loopback Mode.<br>1: Enable internal loopback mode<br>0: Disable internal loopback mode  | RW     |
| 13  | Speed[0] | 1       | Speed Select Bit<br>Speed [1:0]:<br>11: Reserved<br>10: Reserved<br>01:100Mbps<br>0: 10Mbps<br>After completing auto negotiation, this bit will reflect the speed status.<br>1:100Base-T<br>0:10Base-Te   | RW     |
| 12  | AN_E     | 1       | Auto-Negotiation Enable.<br>1: Enable Auto-Negotiation<br>0: Disable Auto-Negotiation   | RW     |
| 11  | PWD      | 0       | Power Down.<br>1: Power down (only Management Interface and logic are active; link is down)<br>0: Normal Operation  | RW     |
| 10  | Isolate  | 0       | Isolate.<br>1: Isolate<br>0: Normal Operation<br>MII interface is isolated; the serial management interface (MDC, MDIO) is still active. When this bit is asserted, the PHY ignores TX_D[3:0], and TXCTL inputs, and presents a high impedance on RXC, RXCTL, RX_D[3:0] | RW     |
| 9   | RS_AN    | 0       | Restart Auto-Negotiation.<br>1: Restart Auto-Negotiation<br>0: Normal operation   | RW/SC  |
| 8   | Duplex   | 1       | duplex mode set<br>if auto-negotiation is disabled (register0 bit 12=0).<br>1: Full duplex<br>0: Half duplex  | RW     |



|     |                |   |   |    |
|-----|----------------|---|---|----|
|     |                |   | After completing auto-negotiation, this bit will reflect the duplex status.<br>1: Full duplex<br>0: Half duplex |    |
| 7   | Collision Test | 0 | Collision Test.<br>1: Enable Collision Test<br>0: Normal Operation  | RW |
| 6   | Speed [1]      | 0 | Speed Select Bit 1<br>Refer to bit 0[13].   | RW |
| 5:0 | Reserved       | - | Reserved  | -  |

#### 4.3.2 BMSR (Basic Mode Status Register, Address: Register 0x1)

Table16. BMSR

| Bit  | Name         | Default | Description  | Access |
|------|--------------|---------|--|--------|
| 15   | 100Base-T4   | 0       | 100Base-T4 Capability.<br>1: Enable 100Base-T4 support<br>0: Suppress 100Base-T4 support   | RO     |
| 14   | 100Base-TX_F | 1       | 100Base-TX Full Duplex Capability.<br>1= full-duplex 100Base-TX can be performed by PHY.<br>0=full-duplex 100Base-TX cannot be performed by PHY.   | RO     |
| 13   | 100Base-TX_H | 1       | 100Base-TX Half Duplex Capability.<br>1= half-duplex 100Base-TX can be performed by PHY.<br>0= half-duplex 100Base-TX cannot be performed by PHY.  | RO     |
| 12   | 10Mbps_F     | 1       | 10Mbps Full Duplex Capability.<br>1= full-duplex 10Base-Te can be performed by PHY.<br>0=full-duplex 10Base-Te cannot be performed by PHY.   | RO     |
| 11   | 10Mbps_H     | 1       | 10Mbps half -duplex Capability.<br>1= half-duplex 10Base-Te can be performed by PHY.<br>0= half-duplex 10Base-Te cannot be performed by PHY.   | RO     |
| 10:9 | Reserved     | 00      | Reserved   | RO     |
| 8    | Ext_Status   | 1       | Extended status register in 0x0F<br>1: Supported extended status register<br>0: Not supported extended status register   | RO     |
| 7    | Transmit_MII | 0       | 1: PHY able to transmit from MII regardless of whether the PHY has detected that a valid link has been established.<br>0: PHY able to transmit from MII only when the PHY has detected that a valid link has been established.   | RO     |
| 6    | MF_PS        | 1       | 1: The PHY will accept management frames with preamble suppressed.<br>0: The PHY will not accept management frames with preamble suppressed.<br>A minimum of 32 preamble bits are required: the first management interface read/write transaction after reset. One idle bit is required between any two management transactions as per IEEE 802.3u specifications. | RO     |
| 5    | AN_C         | 0       | Auto-Negotiation Complete.<br>1=Auto-Negotiation process is complete.<br>0=Auto-Negotiation process is not complete.   | RO     |
| 4    | Remote Fault | 0       | Remote Fault.<br>1=Remote fault condition is detected (cleared on read or by reset).<br>0=Remote fault condition is not detected.  | RC     |
| 3    | AN_A         | 1       | Auto-Negotiation Ability.  | RO     |



|   |                |   |   |    |
|---|----------------|---|---|----|
|   |                |   | 1=Auto-Negotiation can be performed by PHY<br>0=Auto-Negotiation cannot be performed by PHY   |    |
| 2 | Link Status    | 0 | Link Status<br>1: Linked<br>0: Not Linked<br>This bit indicates whether the link was lost since the last read.:<br>the current link status, read this register twice.                 | RO |
| 1 | Jabber Detect  | 0 | Jabber Detect<br>1: Jabber condition detected<br>0: No Jabber detected  | RO |
| 0 | Ext_Capability | 1 | 1: Extended register capable (permanently=1)<br>0: Not extended register capable<br>To indicate whether support EXTs, to access from address register<br>0x1E and data register 0x1F. | RO |

#### 4.3.3 PHYID1 (PHY Identifier Register #1, Address: Register 0x2)

Table17. PHYID1

| Bit  | Name      | Default | Description               | Access |
|------|-----------|---------|---------------------------|--------|
| 15:0 | PHYID_LSB |         | PHY Identifier Bit [18:3] | RO     |

#### 4.3.4 PHYID2 (PHY Identifier Register #2, Address: Register 0x3)

Table18. PHYID2

| Bit   | Name            | Default | Description                | Access |
|-------|-----------------|---------|----------------------------|--------|
| 15:10 | PHYID_MSB       |         | PHY Identifier Bit [24:19] | RO     |
| 9:4   | Model Number    | 01 0010 | Manufacture's Model Number | RO     |
| 3:0   | Revision Number | 1000    | Revision Number            | RO     |

#### 4.3.5 ANAR (Auto-Negotiation Advertising, Address: Register 0x4)

This register contains the advertised abilities of this device as they will be transmitted to its link partner during auto-negotiation.

Table19. ANAR

| Bit | Name          | Default | Description   | Access |
|-----|---------------|---------|---|--------|
| 15  | Next Page*    | 0       | Next Page Bit.<br>1: Advertise<br>0: Not advertised   | RW     |
| 14  | Reserved      | 0       | Reserved  | RO     |
| 13  | Remote Fault  | 0       | Remote Fault<br>1: Set Remote Fault bit<br>0: No Remote Fault bit   | RW     |
| 12  | Ext_Next_Page | 1       | Extended next page enable control bit<br>1: Local device supports transmission of extended next pages<br>0: Local device does not support transmission of extended next | RW     |



|     |                   |       | pages.  |    |
|-----|-------------------|-------|---|----|
| 11  | Asymmetric PAUSE* | 1     | Asymmetric PAUSE<br>1: Advertise asymmetric pause support<br>0: No support of asymmetric pause                | RW |
| 10  | Pause*            | 1     | 1: MAC PAUSE implemented<br>0: MAC PAUSE not implemented  | RW |
| 9   | 100Base-T4        | 0     | 1: 100Base-T4 is supported by local node<br>0: 100Base-T4 not supported by local node                         | RO |
| 8   | 100Base-TX_F*     | 1     | 1: 100Base-TX full duplex is supported by local node<br>0: 100Base-TX full duplex not supported by local node | RW |
| 7   | 100Base-TX_H*     | 1     | 1: 100Base-TX half duplex is supported by local node<br>0: 100Base-TX half duplex not supported by local node | RW |
| 6   | 10Base-Te-F*      | 1     | 1: 10Base-Te full duplex supported by local node<br>0: 10Base-Te full duplex not supported by local node      | RW |
| 5   | 10Base-Te_H*      | 1     | 1: 10Base-Te half duplex is supported by local node<br>0: 10Base-Te half duplex not supported by local node   | RW |
| 4:0 | Selector Field    | 00001 | Selector Field mode.<br>00001: IEEE 802.3   | RO |

\*: This bit is updated immediately after the writing operation; However, the configuration does not take effect until any of the following occurs:

- Software reset is asserted by writing register 0x0 bit[15]
- Restart Auto-Negotiation is triggered by writing register 0x0 bit[9]
- The port is switched from power down to normal operation by writing register 0x0 bit[11]
- Link goes down

#### 4.3.6 ANLPA (Auto-Negotiation Link Partner Ability, Address: Register 0x5)

This register contains the advertised abilities of the Link Partner as received during auto-negotiation. The content changes after a successful auto-negotiation if Next-pages are supported.

Table20. ANLPA

| Bit | Name             | Default | Description  | Access |
|-----|------------------|---------|--|--------|
| 15  | Next Page        | 0       | Next Page Indication.<br>0: Transmitting the primary capability data page<br>1: Transmitting the protocol specific data page   | RO     |
| 14  | ACK              | 0       | Acknowledge<br>1: Link partner acknowledges reception of local node's capability data word<br>0: No acknowledgement  | RO     |
| 13  | Remote Fault     | 0       | Remote Fault<br>1: Link partner is indicating a remote fault<br>0: Link partner is not indicating a remote fault   | RO     |
| 12  | Reserved         | -       | Reserved.  | -      |
| 11  | Asymmetric Pause | 0       | Asymmetric Pause<br>1: Asymmetric pause control supported by Link Partner<br>0: No Asymmetric pause control supported by Link Partner<br>When auto-negotiation is enabled, this bit reflects Link Partner ability. | RO     |
| 10  | Pause            | 0       | 1: Link partner supports pause operation<br>0: Link partner does not support pause operation   | RO     |
| 9   | 100Base-T4       | 0       | 100Base-T4 supporting  | RO     |



|     |                |       |   |    |
|-----|----------------|-------|---|----|
|     |                |       | 1: 100Base-T4 is supported by link partner<br>0: 100Base-T4 not supported by link partner   |    |
| 8   | 100Base-TX-F   | 0     | 100Base-TX full duplex supporting<br>1: 100Base-TX full duplex is supported by link partner<br>0: 100Base-TX full duplex not supported by link partner  | RO |
| 7   | 100Base-TX     | 0     | 100Base-TX supporting<br>1: 100Base-TX is supported by link partner<br>0: 100Base-TX not supported by link partner<br>This bit will also be set if the link in 100Base-TX is established by parallel detection.                                 | RO |
| 6   | 10Base-Te-F    | 0     | 10Base-Te full duplex supporting<br>1: 10Base-Te full duplex is supported by link partner<br>0: 10Base-Te full duplex not supported by link partner   | RO |
| 5   | 10Base-Te_H    | 0     | 10Base-Te half duplex supporting<br>1: 10Base-Te half duplex is supported by link partner<br>0: 10Base-Te half duplex not supported by link partner<br>This bit will also be set if the link in 10Base-Te is established by parallel detection. | RO |
| 4:0 | Selector Field | 00000 | Link Partner's Binary Encoded Node Selector.  | RO |

#### 4.3.7 ANE (Auto-Negotiation Expansion Register Address: Register 0x6)

This register contains additional status: NWay auto-negotiation.

Table21. ANE

| Bit  | Name                           | Default | Description  | Access |
|------|--------------------------------|---------|--|--------|
| 15:5 | Reserved                       | -       | Reserved.  | -      |
| 4    | Parallel Detection Fault       | 0       | Parallel Detection Fault<br>1: A fault has been detected via the Parallel Detection function<br>0: No fault has been detected via the Parallel Detection function                    | RC     |
| 3    | Link Partner Next Page Ability | 0       | Link Partner Next Page Ability<br>1: Link Partner is Next Page able<br>0: Link Partner is not Next Page able   | RO     |
| 2    | Local Next Page Ability        | 1       | Local Next Page Ability<br>1: Next Page is able<br>0: Not Next Page able   | RO     |
| 1    | Page Received                  | 0       | 1: A New Page has been received<br>0: A New Page has not been received   | RC     |
| 0    | LP_AN_A                        | 0       | Link Partner Auto-Negotiation Ability<br>If Auto-Negotiation is Enabled, This Bit Means:<br>1: Link Partner is Auto-Negotiation able<br>0: Link Partner is not Auto-Negotiation able | RO     |

#### 4.3.8 ANNPT (Auto-Negotiation Next Page Transmit Register Address: Register 7)

Transmit the local auto-negotiation next page.

Table22. ANNPT

| Bit | Name      | Default | Description    | Access |
|-----|-----------|---------|----------------|--------|
| 15  | Next Page | 0       | Next Page Bit. | RW     |



|      |             |     |  |    |
|------|-------------|-----|--|----|
|      |             |     | 1: The page is not the last page<br>0: The page is the last page   |    |
| 14   | Reserved    | 0   | Reserved   | RO |
| 13   | MS_Page_M   | 0   | Message Page Mode<br>1: Message Page<br>0: Unformatted Page  | RW |
| 12   | ACK2        | 0   | Acknowledge<br>1: Comply with message<br>0: No Comply with message   | RW |
| 11   | Toggle      | 0   | 1: This bit in the previously exchanged Code Word is logic 0<br>0: The Toggle bit in the previously exchanged Code Word is logic 1 | RO |
| 10:0 | MS_UF_Field | 0x1 | These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0.      | RW |

#### 4.3.9 ANNPR (Auto-Negotiation Next Page Received Register Address: Register 0x8)

Received the Auto-Negotiation next page from Link Partner.

Table23. ANNPR

| Bit  | Name        | Default | Description  | Access |
|------|-------------|---------|--|--------|
| 15   | Next Page   | 0       | Next Page Bit.<br>1: The page is not the last page<br>0: The page is the last page   | RO     |
| 14   | Reserved    | 0       | Reserved   | RO     |
| 13   | MS_Page_M   | 0       | Message Page Mode<br>1: Message Page<br>0: Unformatted Page  | RO     |
| 12   | ACK2        | 0       | Acknowledge<br>1: Comply with message<br>0: No Comply with message   | RO     |
| 11   | Toggle      | 0       | 1: This bit in the previously exchanged Code Word is logic 0<br>0: The Toggle bit in the previously exchanged Code Word is logic 1 | RO     |
| 10:0 | MS_UF_Field | 0x0     | These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0.      | RO     |

#### 4.3.10 MSSR (Master-Slave Status Register Address: Register 0xA)

Table24. MSSR

| Bit | Name  | Default | Description  | Access |
|-----|---|---------|--|--------|
| 15  | MASTER/<br>SLAVE<br>CONFIGURATI<br>ON FAULT         | 0       | Master / Slave Manual Configuration Fault Detected:<br>1: Manual Master/Slave Configuration fault detected.<br>0: No Manual Master/Slave Configuration fault detected<br>This register bit will clear on read, | RO     |
| 14  | MASTER/<br>SLAVE<br>CONFIGURATI<br>ON<br>RESOLUTION | 0       | Master / Slave Configuration Results:<br>1: Configuration resolved to MASTER.<br>0: Configuration resolved to SLAVE.   | RO     |
| 13  | LOCAL<br>RECEIVER<br>STATUS                         | 0       | Local Receiver Status:<br>1: Local receiver is OK.<br>0: Local receiver is not OK.   | RO     |



|     |                        |     |   |    |
|-----|------------------------|-----|---|----|
| 12  | Remote Receiver        | 0   | 1: Remote Receiver OK<br>0: Remote Receiver not OK  | RO |
| 11  | 1000BASE-T Full Duplex | 0   | Advertise 1000BASE-T Full-Duplex Capability.<br>1: Advertise<br>0: Do not advertise   | RO |
| 10  | 1000BASE-T HALF DUPLEX | 0   | Link Partner 1000BASE-T Half Duplex Capable:<br>1: Link Partner capable of 1000Base-T Half Duplex.<br>0: Link partner not capable of 1000Base-T Half Duplex | RO |
| 9:8 | Reserved               | 0   | Reserved.   | RO |
| 7:0 | Idle Error Count       | 0x0 | Idle Error Counter. The register indicates the idle error count since the last read operation performed to this register.                                   | RO |

#### 4.3.11 MMD\_AC (MMD Access Control; Address: Register 0xD)

Table25. MMD\_AC

| Bit   | Name         | Default     | Description  | Access |
|-------|--------------|-------------|--|--------|
| 15:14 | MMD Function | 0           | MMD Function about Data and Address<br>00: Address<br>01: Data; no post increment<br>10: Data; post increment on reads and writes<br>11: Data; post increment on writes only | WO     |
| 13:5  | RSVD         | 0 0000 0000 | Reserved.  | RO     |
| 4:0   | DEVAD        | 0           | MMD Device Address.<br>00001: MMD1<br>00011: MMD3<br>00111: MMD7   | WO     |

Note 1: Used in conjunction with the MAADR (Register 14) to provide access to the MMD address space.

Note 2: If the access of MAADR is: address (Function=00) then it is directed to the address register within the MMD associated with the value in the DEVAD field.

Note 3: If the access of MAADR is: data (Function=01) then both the DEVAD field and the MMD address register direct the MAADR data accesses to the appropriate registers within the MMD.

#### 4.3.12 MMD\_AADA (MMD Access Address Data, Address: Register 0xE)

Table26. MMD\_AADR

| Bit  | Name         | Default | Description   | Access |
|------|--------------|---------|---|--------|
| 15:0 | Address Data | 0x0000  | [15:14]:00<br>It means MMD DEVAD's address register<br>[15:14]:01, 10, or 11<br>It means MMD DEVAD's data register as indicated by the contents of its address register | RW     |

#### 4.3.13 PHYCR (PHY Control Register, Address: Register 0x10)

Table27. PHYCR

| Bit  | Name          | Default | Description   | Access |
|------|---------------|---------|---|--------|
| 15:7 | RSVD          | 0x0     | Reserved.   | RO     |
| 6:5  | MDI_CROSSOVER | 0x3     | MDI Crossover Mode:<br>11: Enable automatic crossover | RW     |





|   |             |   |   |    |
|---|-------------|---|---|----|
|   |             |   | 10: Reserved<br>01: Manual MDI-X configuration<br>00: Manual MDI configuration  |    |
| 4 | RSVD        | 0 | Reserved.   | RW |
| 3 | CRS-TX      | 0 | This bit is effective in 10BASE-Te half-duplex mode and 100BASE-TX mode:<br>1: Assert CRS on transmitting or receiving<br>0: Never assert CRS on transmitting, only assert it on receiving. | RW |
| 2 | EN_SEQ_Test | 0 | 1: SQE test enabled,<br>0: SQE test disabled<br>Note: SQE Test is automatically disabled in full-duplex mode regardless the setting in this   | RW |
| 1 | POL_REV     | 1 | If polarity reversal is disabled, the polarity is forced to be normal in 10BASE-Te.<br>1: Polarity Reversal Enabled<br>0: Polarity Reversal Disabled  | RW |
| 0 | DIS_JAB     | 0 | 1: Disable 10BASE-Te jabber detection function<br>0: Enable 10BASE-Te jabber detection function   | RW |

#### 4.3.14 PHYSR (PHY Status Register, Address: Register 0x11)

Table28. PHYSR

| Bit   | Name                  | Default | Description  | Access |
|-------|-----------------------|---------|--|--------|
| 15:14 | SPEED SELECTION       | 0x0     | Speed Select Status:<br>11: Reserved<br>10: 1000 Mbps<br>01: 100 Mbps<br>00: 10 Mbps   | RO     |
| 13    | DUPLEX MODE           | 0       | Duplex Mode Status:<br>1: Full Duplex<br>0: Half Duplex.   | RO     |
| 12    | PAGE RECEIVED         | 0       | Page Received:<br>This bit is latched high and will be cleared upon a read.<br>1: Page received.<br>0: No page received.   | RO     |
| 11    | SPEED DUPLEX RESOLVED | 0       | Speed Duplex Resolution Status:<br>1: Auto-Negotiation has completed or is disabled.<br>0: Auto-Negotiation is enabled and has not completed   | RO     |
| 10    | LINK STATUS           | 0       | 1: Link up<br>0: Link down   | RO     |
| 9:7   | RSVD                  | 0x0     | Reserved.  | RO     |
| 6     | MDI Crossover Status  | 0       | 1: MDIX<br>0: MDI<br>This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed, or Auto-Negotiation is disabled.<br>The bit value depends on register 0x10 “PHY specific function control register” bits6~bit5 configurations. Register 0x10 configurations take effect after software reset. | RO     |
| 5     | Wirespeed downgrade   | 0       | 1: Downgrade<br>0: No Downgrade  | RO     |
| 4     | RSVD                  | 0       | Reserved.  | RO     |
| 3     | Transmit Pause        | 0       | This status bit is valid only when bit11 is 1.   | RO     |



|   |               |   |   |    |
|---|---------------|---|---|----|
|   |               |   | Bit11 is set when Auto-Negotiation is completed. This bit indicates MAC pause resolution. This bit is for information purposes only and is not used by the device. When in force mode, this bit is set to be 0.<br>1: Transmit pause enabled<br>0: Transmit pause disabled  |    |
| 2 | Receive Pause | 0 | This status bit is valid only when bit[11] is 1. Bit[11] is set when Auto-Negotiation is completed. This bit indicates MAC pause resolution. This bit is for information purposes only and is not used by the device. When in force mode, this bit is set to be 0.<br>1: Receive pause enabled<br>0: Receive pause disabled | RO |
| 1 | Polarity      | 0 | 1: Reverted polarity<br>0: Normal polarity  | RO |
| 0 | Jabber        | 0 | 1: Jabber<br>0: No jabber   | RO |

#### 4.3.15 INTCR (Interrupt Control Register, Address: Register 0x12)

Table29. INTCR

| Bit   | Name                    | Default | Description   | Access |
|-------|-------------------------|---------|---|--------|
| 15:14 | AN_ERR_INT_EN           | 0x0     | Enable Auto-Negotiation Error Interrupt:<br>1: Enable Auto-Negotiation Error interrupt.<br>0: Disable Auto-Negotiation Error interrupt. | RW     |
| 14    | SPEED_CHNG_INT_EN       | 0       | Enable Speed Change Interrupt:<br>1: Enable Speed Change interrupt.<br>0: Disable Speed Change interrupt.                               | RW     |
| 13    | DUPLEX_MODE_CHNG_INT_EN | 0       | Enable Duplex Mode Change Interrupt:<br>1: Enable Duplex Mode Change interrupt.<br>0: Disable Duplex Mode Change interrupt.             | RW     |
| 12    | PAGE_RECEIVED_INT_EN    | 0       | Enable Page Received Interrupt:<br>1: Enable Page Received Interrupt.<br>0: Disable Page Received Interrupt.                            | RW     |
| 11    | LINK_FAIL_INT_EN        | 0       | Enable Link Fail Interrupt:<br>1: Enable Link Fail Interrupt.<br>0: Disable Link Fail Interrupt.  | RW     |
| 10    | LINK_COMPLETE_INT_EN    | 0       | Enable Link Complete Interrupt:<br>1: Enable Link Complete Interrupt.<br>0: Disable LINK Complete Interrupt.                            | RW     |
| 9:7   | RSVD                    | 0x0     | Reserved.   | RW     |
| 6     | WoL_INT_EN              | 0       | Enable Wake-on-LAN Interrupt:<br>1: Enable Wake-on-LAN Interrupt.<br>0: Disable Wake-on-LAN Interrupt                                   | RW     |
| 5     | WS_DG_INT_EN            | 0       | Wirespeed downgraded Interrupt<br>1: Enable Interrupt.<br>0: Disable Interrupt  | RW     |
| 4:2   | RSVD                    | 0x0     | Reserved.   | RW     |
| 1     | PL_CH_INT_EN            | 0       | Enable Polarity Change Interrupt:<br>1: Enable Polarity Change interrupt.<br>0: Disable Polarity Change interrupt.                      | RW     |
| 0     | JB_INT_EN               | 0       | Enable Jabber Interrupt:<br>1: Enable Jabber interrupt.<br>0: Disable Jabber interrupt  | RW     |

**4.3.16 INTSR (Interrupt Status Register, Address: Register 0x13)**

Table30. INTSR

| Bit | Name                    | Default | Description   | Access   |
|-----|-------------------------|---------|---|----------|
| 15  | AN_ERR_INT              | 0x0     | Auto-Negotiation Error Interrupt:<br>1: Occur Auto-Negotiation Error interrupt<br>0: No Auto-Negotiation Error interrupt. | RO<br>RC |
| 14  | SPEED_CHNG_INT_EN       | 0       | Speed Change Interrupt:<br>1: Occur Speed Change interrupt.<br>0: No Speed Change interrupt.                              | RO<br>RC |
| 13  | DUPLEX_MODE_CHNG_INT_EN | 0       | Duplex Mode Change Interrupt:<br>1: Occur Duplex Mode Change interrupt.<br>0: No Duplex Mode Change interrupt.            | RO<br>RC |
| 12  | PAGE_RECEIVED_INT_EN    | 0       | Page Received Interrupt:<br>1: Occur Page Received Interrupt.<br>0: No Page Received Interrupt.                           | RO<br>RC |
| 11  | LINK_FAIL_INT_EN        | 0       | Link Fail Interrupt:<br>1: Occur Link Fail Interrupt.<br>0: No Link Fail Interrupt.                                       | RO<br>RC |
| 10  | LINK_COMPLETE_INT_EN    | 0       | Link Complete Interrupt:<br>1: Occur Link Complete Interrupt.<br>0: No LINK Complete Interrupt.                           | RO<br>RC |
| 9:7 | RSVD                    | 0x0     | Reserved.   | RO<br>RC |
| 6   | WoL_INT_EN              | 0       | Wake-on-LAN Interrupt:<br>1: Occur Wake-on-LAN Interrupt.<br>0: No Wake-on-LAN Interrupt                                  | RO<br>RC |
| 5   | WS_DG_INT_EN            | 0       | Wirespeed downgraded Interrupt<br>1: Occur Interrupt.<br>0: No Interrupt  | RO<br>RC |
| 4:2 | RSVD                    | 0x0     | Reserved.   | RO<br>RC |
| 1   | PL_CH_INT_EN            | 0       | Polarity Change Interrupt:<br>1: Occur Polarity Change interrupt.<br>0: No Polarity Change interrupt.                     | RO<br>RC |
| 0   | JB_INT_EN               | 0       | Jabber Interrupt:<br>1: Occur Jabber interrupt.<br>0: No Jabber interrupt   | RO<br>RC |

**4.3.17 SPCR (Speed Configuration Register, Address: Register 0x14)**

Table31. SPCR

| Bit   | Name      | Default | Description  | Access    |
|-------|-----------|---------|--|-----------|
| 15:12 | RSVD      | 0x0     | Reserved.  | RO        |
| 11    | EN_MDIO_L | 1       | 1: To latch MII/MMD register's read out value during MDIO read<br>0: Do not latch MII/MMD register's read out value during MDIO read   | RW        |
| 10:6  | RSVD      | 0x0     | Reserved.  | RW        |
| 5     | SP_DG_EN  | 1       | 1: Enables auto speed downgrade function. Writing this bit requires a software reset to up<br>0: Disable auto speed downgrade function | RW<br>POS |



|     |                  |     |  |    |
|-----|------------------|-----|--|----|
| 4:2 | AN_AT_SPDG       | 0x3 | Attempts times (set value + additional 2) before downgrading.<br>Such as 11: Attempts five times (set value 3 + additional 2) before downgrading. The number of attempts can be changed by these bits. Only take effect after software rese        | RW |
| 1   | BP_Timer_Auto_SP | 0   | 1:The wirespeed downgrade FSM will bypass the timer used for link stability check;<br>0: not bypass the timer, then links that established but hold for less than 2.5s would still be taken as failure, autoneg. retry counter will increase by 1. | RW |
| 0   | RSVD             | 0   | Reserved.  | RO |

#### 4.3.18 RECR (Receiver Error Counter Register, Address: Register 0x15)

Table32. RECR

| Bit  | Name          | Default | Description   | Access    |
|------|---------------|---------|---|-----------|
| 15:0 | RXERCNT[15:0] | 0x0     | RX_ER Counter:<br>Receive error counter. This register saturates at the maximum value of 0xFFFF and hold it, not roll over. | RO<br>SWC |

#### 4.3.19 EXT\_ADD (Extended Register Address Register, Address: Register 0x1E)

Table33. EXT\_ADD

| Bit  | Name    | Default | Description               | Access |
|------|---------|---------|---------------------------|--------|
| 15:0 | EXT_ADD | 0x0     | Extended Register Address | RW     |

#### 4.3.20 EXT\_DATA (Extended Register Data Register, Register 0x1F)

Table34. EXT\_DATA

| Bit  | Name     | Default | Description            | Access |
|------|----------|---------|------------------------|--------|
| 15:0 | EXT_DATA | 0x0     | Extended Register data | RW     |

### 4.4 Extended Register

#### 4.4.1 EXT\_10M\_PWRCON (10Mbps Power Control Register, Address: Register 0x200A)

Table35. EXT\_10M\_PWRCON

| Bit   | Name       | Default | Description  | Access |
|-------|------------|---------|--|--------|
| 15:11 | RESV       | 11001   | Reserved   | RW     |
| 10    | EN_10M_IDL |         | 1: In 10BT mode , if there's no data or NLP to transmit, shut off DAC; otherwise turn on the DAC;<br>0: In 10BT, DAC will not be turn off. | RW     |
| 9:0   | RESV       | 0x202   | Reserved   | RW     |

#### 4.4.2 EXT\_COMBO\_CON (COMBO Control Register, Address: Register 0x4000)

Table36. EXT\_COMBO\_CON



| Bit   | Name            | Default | Description   | Access |
|-------|-----------------|---------|---|--------|
| 15:12 | RESV            | 0x0     | Reserved  | RW     |
| 11    | REMOTE_LOOPBACK | 0       | set remote loopback<br>1: enable<br>0: disable  | RW     |
| 10:6  | RESV            | 0x0     | Reserved  | RW     |
| 5     | JUMBO_EN        | 0       | 1: enable jumbo frame reception<br>0: disable jumbo frame reception<br>Enable Jumbo frame reception up to 18KB frame, when disabled only up to 4.5KB frame supported  | RW     |
| 4     | RMII_RX_DV_SEL  | 0       | Drive PAD CRS_DV of RMII by CRS_DV or RX_DV.<br>1: by RX_DV<br>0: by CRS_DV   | RW     |
| 3     | RESV            | 0       | Reserved  | RW     |
| 2     | WoL_EN          | 0       | 1: enable WoL.<br>0: disable WoL  | RW     |
| 1     | RMII_EN         | 0       | 1: enable RMII mode<br>0: disable RMII mode   | RW     |
| 0     | CLK_SEL         | 0       | Its default value is determined by power on strapping.<br>1: input TXC/RXC;<br>0: output TXC/RXC.<br>[RMII_EN, CLK_SEL]:<br>2'b00: MII mode;<br>2'b01: RMII mode;<br>2'b10: RMII2 mode;<br>2'b11: RMII3 mode. | RW     |

#### 4.4.3 EXT\_PIN\_CON (PAD Control Register, Address: Register 0x4001)

Table37. EXT\_PIN\_CON

| Bit  | Name    | Default | Description   | Access |
|------|---------|---------|---|--------|
| 15   | INT_WoL | 1       | Control to output general interrupt or WoL interrupt to Pin24(LED0), when power on strapping value of RX_D1 is 1.<br>1: output general interrupt;<br>0: output WoL interrupt. | RW     |
| 14:6 | RESV    | 0x3     | Reserved  | RW     |
| 5:4  | XMII_DR | 0x2     | Xmii interface driver strength control in non-scan mode   | RW     |
| 3:2  | MDIO_DR | 0x3     | Mdio pin driver strength control in non-scan mode.  | RW     |
| 1:0  | RESV    | 0x3     | Reserved  | RW     |

#### 4.4.4 EXT\_COMBO2\_CON (COMBO2 Control Register, Address: Register 0x4003)

Table38. EXT\_COMBO2\_CON

| Bit   | Name           | Default | Description   | Access |
|-------|----------------|---------|---|--------|
| 15    | RESV           | 0       | Reserved  | RW     |
| 14    | Slave_Jitter_T | 0       | Mux clk_dac to rxc in slave jitter test mode<br>1: enable<br>0: disable       | RW     |
| 13:10 | RESV           | 0x0     | Reserved  | RW     |
| 9:7   | WoL_LTH_SEL    | 0x4     | WoL_lth_sel[0] control WoL interrupt to be a level or a pulse.<br>1: a pulse; | RW     |



|     |                   |     |  |    |
|-----|-------------------|-----|--|----|
|     |                   |     | 0: a level.<br>WoL_lth_sel[2:1] control WoL interrupt pulse width when WoL_lth_sel[0] is 1.<br>2'b00: 10us;<br>2'b01: 100us;<br>2'b10: 1ms;<br>2'b11: 10ms |    |
| 6   | EN_Isolate_TX_CLK | 1   | When isolate bit (BMCR register) is 1, control to make TX_CLK input or not.<br>1'b1: input;<br>1'b0: keep TX_CLK previous direction.                       | RW |
| 5   | EN_Isolate_RX_CLK | 1   | When isolate bit (BMCR register) is 1, control to make RX_CLK input or not.<br>1'b1: input;<br>1'b0: keep RX_CLK previous direction.                       | RW |
| 4:0 | RESV              | 0x0 | Reserved   | RW |

#### 4.4.5 WoL\_MAC\_ADDH(WoL MAC Highest Address Register, Address: Register 0x4004)

Table39. WoL\_MAC\_ADDH

| Bit  | Name           | Default | Description                                       | Access |
|------|----------------|---------|---|--------|
| 15:0 | WoL_MAC_ADDR_H | 0x0     | highest 16 bits of MAC address used for WoL 47:32 | RW     |

#### 4.4.6 WoL\_MAC\_ADDM(WoL MAC Middle Address Register, Address: Register 0x4005)

Table40. WoL\_MAC\_ADDM

| Bit  | Name           | Default | Description                                      | Access |
|------|----------------|---------|--|--------|
| 15:0 | WoL_MAC_ADDR_M | 0x0     | Middle 16 bits of MAC address used for WoL 31:16 | RW     |

#### 4.4.7 WoL\_MAC\_ADDL(WoL MAC Lowest Address Register, Address: Register 0x4006)

Table41. WoL\_MAC\_ADDL

| Bit  | Name           | Default | Description                                      | Access |
|------|----------------|---------|--|--------|
| 15:0 | WoL_MAC_ADDR_L | 0x0     | Lowest 16 bits of MAC address used for WoL 31:16 | RW     |

#### 4.4.8 PKG\_ST\_CON (Package Generation Selftest Control, Address: Register 0x40A0)

Table42. PKG\_ST\_CON

| Bit | Name        | Default | Description   | Access |
|-----|-------------|---------|---|--------|
| 15  | PKG_CHK_EN  | 0       | RX checker checks the UTP MII RX data; TX checker checks the UTP MII TX data.<br>1: Enable UTP RX/TX package checker.<br>0: Disable UTP RX/TX package checker | RW     |
| 14  | PKG_GATE_EN | 1       | 1: Enable gate all the clocks to package self test module when bit15 PKG_CHK_EN is 0, bit13 PKG_GEN_MODE is 1 and   | RW     |



|      |                   |     |   |    |
|------|-------------------|-----|---|----|
|      |                   |     | bit12 PKG_GEN_EN is 0;<br>0: Not gate the clocks.   |    |
| 13   | PKG_GEN_TEST      | 1   | 1: normal mode, to send xMII TX data from PAD;<br>0: test mode, to send out the MII data generated by pkg_gen module.   | RW |
| 12   | PKG_GEN_MODE      | 0   | 1: to enable pkg_gen generating MII packages. But, the data will only be sent to transceiver when Bit13 bp_pkg_gen is 1'b0. If pkg_burst_size is 0, continuous packages will be generated and will be stopped only when pkg_gen_en is set to 0; Otherwise, after the expected packages are generated, pkg_gen will stop, pkg_gen_en will be self-cleared. | RW |
| 11:8 | PKG_PREAM_LEN     | 0x8 | The preamble length of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.   | RW |
| 7:4  | PKG_IPG_LEN       | 0xC | The IPG of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.   | RW |
| 3    | PKG_GEN_FORCE_gen | 0   | 1: enable pkg_gen to send out the generated data even when the link is not established.<br>0: disable pkg_gen to send out the generated data even when the link is not established  | RW |
| 2    | PKG_COR_CRC       | 0   | 1: to make pkg_gen to send out CRC error packages.<br>0: pkg_gen sends out CRC good packages.   | RW |
| 1:0  | PKG_PL            | 0x0 | Control the payload of the generated packages.<br>11: reserved<br>10: fix pattern 0x5AA55AA5...<br>01: random payload;<br>00: increased Byte payload  | RW |

#### 4.4.9 PKG\_LEN(Package Generation Length, Address: Register 0x40A1)

Table43. PKG\_LEN

| Bit  | Name       | Default | Description                          | Access |
|------|------------|---------|--------------------------------------|--------|
| 15:0 | PKG_LENGTH | 0x40    | the length of the generated packages | RW     |

#### 4.4.10 PKG\_BS(Package Generation Burst Size, Address: Register 0x40A2)

Table44. PKG\_BS

| Bit  | Name         | Default | Description  | Access |
|------|--------------|---------|--|--------|
| 15:0 | PKG_BUR_SIZE | 0x0     | the number of packages in a burst of package generation. | RW     |

#### 4.4.11 PKG\_RV\_H(Package Receiver Valid High, Address: Register 0x40A3)

Table45. PKG\_RVH

| Bit  | Name     | Default | Description   | Access   |
|------|----------|---------|---|----------|
| 15:0 | PKG_RV_H | 0x0     | PKG_RV[31:16], PKG_RV is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte. | RO<br>RC |



#### 4.4.12 PKG\_RV\_L(Package Receiver Valid Low, Address: Register 0x40A4)

Table46. PKG\_RVL

| Bit  | Name     | Default | Description   | Access   |
|------|----------|---------|---|----------|
| 15:0 | PKG_RV_L | 0x0     | PKG_RV [15:0], PKG_RV is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte. | RO<br>RC |

#### 4.4.13 PKG\_RX\_OSH(Package Receiver OS High, Address: Register 0x40A5)

Table47. PKG\_RX\_OSH

| Bit  | Name       | Default | Description   | Access   |
|------|------------|---------|---|----------|
| 15:0 | PKG_RX_OSH | 0x0     | PKG_RX_OS[31:16], PKG_RX_OS is the number of RX packages from wire whose CRC are good and length are >1518Byte. | RO<br>RC |

#### 4.4.14 PKG\_RX\_OSL(Package Receiver OS Low, Address: Register 0x40A6)

Table48. PKG\_RX\_OSL

| Bit  | Name       | Default | Description   | Access   |
|------|------------|---------|---|----------|
| 15:0 | PKG_RX_OSL | 0x0     | PKG_RX_OS [15:0], PKG_RX_OS is the number of RX packages from wire whose CRC are good and length are >1518Byte. | RO<br>RC |

#### 4.4.15 PKG\_RX\_USH(Package Receiver US High, Address: Register 0x40A7)

Table49. PKG\_RX\_USH

| Bit  | Name       | Default | Description  | Access   |
|------|------------|---------|--|----------|
| 15:0 | PKG_RX_USH | 0x0     | PKG_RX_USH [31:16], PKG_RX_USH is the number of RX packages from wire whose CRC are good and length are <64Byte. | RO<br>RC |

#### 4.4.16 PKG\_RX\_USL(Package Receiver US Low, Address: Register 0x40A8)

Table50. PKG\_RX\_USL

| Bit  | Name       | Default | Description   | Access   |
|------|------------|---------|---|----------|
| 15:0 | PKG_RX_USL | 0x0     | PKG_RX_USH [15:0], PKG_RX_USH is the number of RX packages from wire whose CRC are good and length are <64Byte. | RO<br>RC |

#### 4.4.17 PKG\_RX\_ERR(Package Receiver Error, Address: Register 0x40A9)

Table51. PKG\_RX\_ERR

| Bit  | Name       | Default | Description   | Access   |
|------|------------|---------|---|----------|
| 15:0 | PKG_IB_ERR | 0x0     | PKG_IB_ERR is the number of RX packages from wire whose CRC are wrong and length are >=64Byte, <=1518By | RO<br>RC |





#### 4.4.18 PKG\_RX\_OS\_ERR(Package Receiver OS Error, Address: Register 0x40AA)

Table52. PKG\_RX\_OS\_BAD

| Bit  | Name          | Default | Description  | Access   |
|------|---------------|---------|--|----------|
| 15:0 | PKG_RX_OS_ERR | 0x0     | PKG_RX_OS_ERR is the number of RX packages from wire whose CRC are wrong and length are >1518Byte. | RO<br>RC |

#### 4.4.19 PKG\_RX\_FRM (Package Receiver Fragment, Address: Register 0x40AB)

Table53. PKG\_RX\_FRM

| Bit  | Name       | Default | Description   | Access   |
|------|------------|---------|---|----------|
| 15:0 | PKG_RX_FRM | 0x0     | PKG_RX_FRM is the number of RX packages from wire whose length are <64Byte. | RO<br>RC |

#### 4.4.20 PKG\_RX\_NOSFD (Package Receiver NOSFD, Address: Register 0x40AC)

Table54. PKG\_RX\_FRM

| Bit  | Name         | Default | Description  | Access   |
|------|--------------|---------|--|----------|
| 15:0 | PKG_RX_NOSFD | 0x0     | PKG_RX_NOSFD is the number of RX packages from wire whose SFD is missed. | RO<br>RC |

#### 4.4.21 PKG\_TV\_H(Package Transmit Valid High, Address: Register 0x40AD)

Table55. PKG\_RVH

| Bit  | Name     | Default | Description   | Access   |
|------|----------|---------|---|----------|
| 15:0 | PKG_TV_H | 0x0     | PKG_TV[31:16], PKG_TV is the number of TX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte. | RO<br>RC |

#### 4.4.22 PKG\_TV\_L(Package Transmit Valid Low, Address: Register 0x40AE)

Table56. PKG\_TV\_L

| Bit  | Name     | Default | Description  | Access   |
|------|----------|---------|--|----------|
| 15:0 | PKG_TV_L | 0x0     | PKG_TV[15:0], PKG_TV is the number of TX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte. | RO<br>RC |

#### 4.4.23 PKG\_TX\_OSH(Package Transmit OS High, Address: Register 0x40AF)

Table57. PKG\_TX\_OSH

| Bit  | Name       | Default | Description                                      | Access |
|------|------------|---------|--|--------|
| 15:0 | PKG_TX_OSH | 0x0     | PKG_TX_OS [31:16], PKG_TX_OS is the number of TX | RO     |



|  |  |  |   |    |
|--|--|--|---|----|
|  |  |  | packages from wire whose CRC are good and length are >1518Byte. | RC |
|--|--|--|---|----|

#### 4.4.24 PKG\_TX\_OSL(Package Transmit OS Low, Address: Register 0x40B0)

Table58. PKG\_TX\_OSL

| Bit  | Name       | Default | Description   | Access   |
|------|------------|---------|---|----------|
| 15:0 | PKG_TX_OSL | 0x0     | PKG_TX_OS [15:0], PKG_TX_OS is the number of TX packages from wire whose CRC are good and length are >1518Byte. | RO<br>RC |

#### 4.4.25 PKG\_TX\_USH(Package Transmit US High, Address: Register 0x40B1)

Table59. PKG\_TX\_USH

| Bit  | Name       | Default | Description  | Access   |
|------|------------|---------|--|----------|
| 15:0 | PKG_TX_USH | 0x0     | PKG_TX_USH [31:16], PKG_TX_USH is the number of TX packages from wire whose CRC are good and length are <64Byte. | RO<br>RC |

#### 4.4.26 PKG\_TX\_USL(Package Transmit US Low, Address: Register 0x40B2)

Table60. PKG\_TX\_USL

| Bit  | Name       | Default | Description   | Access   |
|------|------------|---------|---|----------|
| 15:0 | PKG_TX_USL | 0x0     | PKG_TX_USH [15:0], PKG_TX_USH is the number of TX packages from wire whose CRC are good and length are <64Byte. | RO<br>RC |

#### 4.4.27 PKG\_TX\_ERR(Package Transmit Error, Address: Register 0x40B3)

Table61. PKG\_TX\_ERR

| Bit  | Name       | Default | Description   | Access   |
|------|------------|---------|---|----------|
| 15:0 | PKG_OB_ERR | 0x0     | pkg_ob_err is the number of TX packages from wire whose CRC are wrong and length are >=64Byte, <=1518By | RO<br>RC |

#### 4.4.28 PKG\_TX\_OS\_ERR(Package Transmit OS Error, Address: Register 0x40B4)

Table62. PKG\_TX\_OSBAD

| Bit  | Name          | Default | Description   | Access   |
|------|---------------|---------|---|----------|
| 15:0 | PKG_TX_OS_ERR | 0x0     | It is the number of TX packages from wire whose CRC are wrong and length are >1518Byte. | RO<br>RC |

#### 4.4.29 PKG\_TX\_FRM (Package Transmit Fragment, Address: Register 0x40B5)

Table63. PKG\_TX\_FRM

| Bit  | Name       | Default | Description  | Access   |
|------|------------|---------|--|----------|
| 15:0 | PKG_TX_FRM | 0x0     | PKG_TX_FRM is the number of TX packages from MII whose length are <64Byte. | RO<br>RC |



#### 4.4.30 PKG\_TX\_NOSFD (Package Transmit NOSFD, Address: Register 0x40B6)

Table64. PKG\_TX\_FRM

| Bit  | Name         | Default | Description   | Access   |
|------|--------------|---------|---|----------|
| 15:0 | PKG_TX_NOSFD | 0x0     | PKG_TX_NOSFD is the number of TX packages from MII whose SFD is missed. | RO<br>RC |

#### 4.4.31 PKG\_CON2 (Package Generation Configure2, Address: Register 0x40B7)

Table65. PKG\_CON2

| Bit  | Name           | Default | Description   | Access |
|------|----------------|---------|---|--------|
| 15:2 | RSVD           | -       | Reserved.   | RO     |
| 1    | PKG_TXSCR      | 0       | 1: The package checker on TX side will check the transmit data generated by pkg_gen;<br>0: The package checker on TX side will check the transmit data of UTP GMII/MII. | RW     |
| 0    | PKG_AZ_EN      | 0       | 1: Enable send LPI pattern during the IPG of the packages sent by pkg_gen.<br>0: Disable send LPI pattern during the IPG of the packages sent by pkg_gen                | RW     |
| 8:0  | PKG_IN_AZ_TIME | 0x1FF   | The time of LPI pattern is sent.<br>Unit is us.   | RW     |

#### 4.4.32 PKG\_CON3 (Package Generation Configure3, Address: Register 0x40B8)

Table66. PKG\_CON3

| Bit   | Name            | Default | Description   | Access |
|-------|-----------------|---------|---|--------|
| 15:11 | RSVD            | -       | Reserved.   | RW     |
| 10:0  | PKG_PRE_AZ_TIME | 0x0     | The time from the end of last package to the beginning of LPI pattern.<br>Unit is us. | RW     |

#### 4.4.33 PKG\_CON4 (Package Generation Configure4, Address: Register 0x40B9)

Table67. PKG\_CON3

| Bit   | Name           | Default | Description                                     | Access |
|-------|----------------|---------|---|--------|
| 15:11 | RSVD           | -       | Reserved.                                       | RW     |
| 10:0  | PKG_IN_AZ_TIME | 0x0     | The time of LPI pattern is sent.<br>Unit is us. | RW     |

#### 4.4.34 PKG\_CON5 (Package Generation Configure5, Address: Register 0x40BA)

Table68. PKG\_CON3

| Bit   | Name            | Default | Description   | Access |
|-------|-----------------|---------|---|--------|
| 15:11 | RSVD            | -       | Reserved.   | RW     |
| 10:0  | PKG_AFT_AZ_TIME | 0x0     | The idle time from the end of LPI pattern to the beginning of next package. | RW     |



|  |  |  |             |  |
|--|--|--|-------------|--|
|  |  |  | Unit is us. |  |
|--|--|--|-------------|--|

#### 4.4.35 LED0\_CON (LED0 Control Register, Address: Register 0x40C0)

Table69. LED0\_CON

| Bit   | Name              | Default | Description  | Access |
|-------|-------------------|---------|--|--------|
| 15    | LED0_FORCE_EN     | 0       | 1 : enable LED0 force mode.  | RW     |
| 14:13 | LED0_FORCE_MODE   | 0x0     | Valid when bit8 is set.<br>11: force LED Blink at Blink Mode2<br>10: force LED Blink at Blink Mode1<br>01: force LED ON<br>00: force LED OFF<br>LED could blink at different frequency in Blink Mode1 and Blink Mode2. | RW     |
| 12    | LED0_ACT_BLK_IND  | 0       | When traffic is present, make LED BLINK no matter the previous LED0 status is ON or OFF, or make LED0 blink only when the previous LED0 is ON.   | RW     |
| 11    | LED0_FDX_ON_EN    | 0       | 1: If BLINK status is not activated, when PHY link up and duplex mode is full duplex, LED0 will be ON.   | RW     |
| 10    | LED0_HDX_ON_EN    | 0       | 1: If BLINK status is not activated, when PHY link up and duplex mode is half duplex, LED0 will be ON.   | RW     |
| 9     | LED0_TXACT_BLK_EN | 1       | 1: If bit[13] is 1, or bit[13] is 0 and ON at certain speed or duplex more is/are activated, when PHY link up and TX is active, make LED0 blink at mode2.  | RW     |
| 8     | LED0_RXACT_BLK_EN | 1       | 1: If bit[13] is 1, or bit[13] is 0 and ON at certain speed or duplex more is/are activated, when PHY link up and RX is active, make LED0 blink at mode2.  | RW     |
| 7     | LED0_TXACT_ON_EN  | 0       | 1: if BLINK status is not activated, when PHY link up and TX is active, make LED0 ON at least 10ms.  | RW     |
| 6     | LED0_RXACT_ON_EN  | 0       | 1: if BLINK status is not activated, when PHY link up and RX is active, make LED0 ON at least 10ms.  | RW     |
| 5     | LED0_HT_ON_EN     | 0       | 1: if BLINK status is not activated, when PHY link up and speed mode is 100Mbps, make LED0 ON;   | RW     |
| 4     | LED0_BT_ON_EN     | 1       | 1: if BLINK status is not activated, when PHY link up and speed mode is 10Mbps, make LED0 ON;  | RW     |
| 3     | LED0_COL_BLK_EN   | 0       | 1: if PHY link up and collision happen, make LED0 BLINK;   | RW     |
| 2     | LED0_HT_BLK_EN    | 0       | 1: if PHY link up and speed mode is 100Mbps, make LED0 BLINK;  | RW     |
| 1     | LED0_BT_BLK_EN    | 0       | 1: if PHY link up and speed mode is 10Mbps, make LED0 BLINK;   | RW     |
| 0     | DIS_LED0_TRY      | 1       | when PHY is active and auto-negotiation is at LINK_GOOD_CHECK status,<br>1: LED will be on;<br>0: LED will be off.   | RW     |

#### 4.4.36 LED\_COMCON (LED Common Control Register, Address: Register 0x40C1)

Table70. LED\_COMCON

| Bit | Name       | Default | Description   | Access |
|-----|------------|---------|---|--------|
| 15  | COL_BLK_SE | 1       | 1 = when collision happens, and related LEDn cfg (n is 0/1/2) | RW     |



|       |                  |     |  |    |
|-------|------------------|-----|--|----|
|       | L                |     | register's bit3 led_col_blk_en is 1, LED blink at Blink Mode2;<br>0 = when collision happens, and related LEDn cfg (n is 0/1/2)<br>register's bit3 led_col_blk_en is 0, LED blink at Blink Mode1.<br>LED could blinks at different frequency in Blink Mode1 and Blink Mode2. Refer to EXT A00F[3:0] for the Blink Mode2 and Blink Mode1. |    |
| 15:10 | RSVD             | -   | Reserved.  | RO |
| 9     | REVERSE_LED_DUTY | 0   | 1: to invert the duty cycle of ON and OFF, namely make LED ON time short and OFF time long.  | RW |
| 8     | LPBK_LED_DIS     | 0   | 1 = In internal loopback mode, LED will not blink;<br>0 = In internal loopback mode, LED will blink;   | RW |
| 7     | JABBER_LED_DIS   | 1   | 1 = when 10Mb/s Jabber happens, LED will not blink;<br>0 = when 10Mb/s Jabber happens, LED will still blink;   | RW |
| 6     | COL_BLK_SEL      | 1   | 1: when collision happens, LED blink at Blink Mode2 with higher frequency;<br>0: when collision happens, LED blink at Blink Mode1 with lower frequency   | RW |
| 5     | EN_LED_ACT_LEVEL | 0   | 1: to make LED blink at different frequency (Blink mode 0) when traffic weight is high.<br>0: to make LED blink always at Blink mode 1 no matter what the traffic weight is  | RW |
| 4:0   | LED_ACT_LEVEL_TH | 0xC | Traffic is heavy or not's threshold.<br>RX/TX traffic is monitored separately. In 1s interval, if RX or TX traffic active time > Led_act_level_th*42ms, then the traffic is heavy; otherwise, traffic is not heavy.  | RW |

#### 4.4.37 LED\_BLCON (LED Blink Control Register, Address: Register 0x40C2)

Table71. LED\_BLCON

| Bit   | Name       | Default | Description  | Access |
|-------|------------|---------|--|--------|
| 15:12 | FREQ_SEL_0 | 0xE     | Control the LED blink frequency in Blink mode 0.<br>ON/OFF duty cycle could be reverted by 40C1h bit9 reverse_led_duty. Below description is the default ON/OFF cycle, that is reverse_led_duty=0.<br>4'd0=LED blink once every 10s, 6% OFF;<br>4'd1=LED blink once every 9.4s, 7% OFF;<br>4'd2=LED blink once every 8s, 8% OFF;<br>4'd3=LED blink once every 7.4s, 9% OFF;<br>4'd4=LED blink once every 6s, 11% OFF;<br>4'd5=LED blink once every 5s, 6% OFF;<br>4'd6=LED blink once every 4s, 8% OFF;<br>4'd7=LED blink once every 3s, 11% OFF;<br>4'd8=LED blink once every 2s, 16% OFF;<br>4'd9=LED blink once every 1s, 16% OFF;<br>4'd10=LED blink at 2Hz, 50% OFF;<br>4'd11=LED blink at 3Hz, 50% OFF;<br>4'd12=LED blink at 4Hz, 50% OFF;<br>4'd13=LED blink at 6Hz, 50% OFF;<br>4'd14=LED blink at 8Hz, 50% OFF;<br>4'd15=LED blink at 10Hz, 50% OFF; | RW     |
| 11:8  | FREQ_SEL_1 | 0xC     | Control the LED blink frequency in Blink mode 1.<br>See description in bit15~12 Freq_sel_c0 for detail   | RW     |
| 7:4   | FREQ_SEL_2 | 0x7     | Control the LED blink frequency in Blink mode 2.<br>See description in bit15~12 Freq_sel_c0 for detail   | RW     |



|     |            |     |  |    |
|-----|------------|-----|--|----|
| 3:0 | FREQ_SEL_3 | 0x5 | Control the LED blink frequency in Blink mode 3.<br>See description in bit15~12 Freq_sel_c0 for detail | RW |
|-----|------------|-----|--|----|

#### 4.4.38 LED1\_CON (LED1 Control Register, Address: Register 0x40C3)

Table72. LED1\_CON

| Bit   | Name              | Default | Description  | Access |
|-------|-------------------|---------|--|--------|
| 15    | LED1_FORCE_EN     | 0       | 1 : enable LED1 force mode.  | RW     |
| 14:13 | LED1_FORCE_MODE   | 0x0     | Valid when bit8 is set.<br>11: force LED Blink at Blink Mode2<br>10: force LED Blink at Blink Mode1<br>01: force LED ON<br>00: force LED OFF<br>LED could blink at different frequency in Blink Mode1 and Blink Mode2. | RW     |
| 12    | LED1_ACT_BLK_IND  | 0       | When traffic is present, make LED BLINK no matter the previous LED1 status is ON or OFF, or make LED1 blink only when the previous LED1 is ON.   | RW     |
| 11    | LED1_FDX_ON_EN    | 0       | 1: If BLINK status is not activated, when PHY link up and duplex mode is full duplex, LED0 will be ON.   | RW     |
| 10    | LED1_HDX_ON_EN    | 0       | 1: If BLINK status is not activated, when PHY link up and duplex mode is half duplex, LED0 will be ON.   | RW     |
| 9     | LED1_TXACT_BLK_EN | 1       | 1: If bit[13] is 1, or bit[13] is 0 and ON at certain speed or duplex more is/are activated, when PHY link up and TX is active, make LED0 blink at mode2.  | RW     |
| 8     | LED1_RXACT_BLK_EN | 1       | 1: If bit[13] is 1, or bit[13] is 0 and ON at certain speed or duplex more is/are activated, when PHY link up and RX is active, make LED0 blink at mode2.  | RW     |
| 7     | LED1_TXACT_ON_EN  | 0       | 1: if BLINK status is not activated, when PHY link up and TX is active, make LED0 ON at least 10ms.  | RW     |
| 6     | LED1_RXACT_ON_EN  | 0       | 1: if BLINK status is not activated, when PHY link up and RX is active, make LED0 ON at least 10ms.  | RW     |
| 5     | LED1_HT_ON_EN     | 0       | 1: if BLINK status is not activated, when PHY link up and speed mode is 100Mbps, make LED0 ON;   | RW     |
| 4     | LED1_BT_ON_EN     | 1       | 1: if BLINK status is not activated, when PHY link up and speed mode is 10Mbps, make LED0 ON;  | RW     |
| 3     | LED1_COL_BLK_EN   | 0       | 1: if PHY link up and collision happen, make LED0 BLINK;   | RW     |
| 2     | LED1_HT_BLK_EN    | 0       | 1: if PHY link up and speed mode is 100Mbps, make LED0 BLINK;  | RW     |
| 1     | LED1_BT_BLK_EN    | 0       | 1: if PHY link up and speed mode is 10Mbps, make LED0 BLINK;   | RW     |
| 0     | RSVD              | 0       | Reserved.  | RO     |



## 5 Environment

Table73. Environment

| Attribute            | Value   |
|----------------------|---------|
| Moisture Sensitivity | Level 3 |
| RoHS                 | RoHS2.0 |

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## 6 Dimensions



| Dimension | Min.     | Typ.  | Max.  |
|-----------|----------|-------|-------|
| <b>A</b>  | 5BSC     |       |       |
| <b>B</b>  | 5BSC     |       |       |
| <b>C</b>  | 0.700    | 0.750 | 0.800 |
| <b>C1</b> | 0.203Ref |       |       |
| <b>C2</b> | 0        | /     | 0.050 |
| <b>D</b>  | 3.300    | 3.400 | 3.500 |
| <b>E</b>  | 3.300    | 3.400 | 3.500 |
| <b>F</b>  | 0.4Ref   |       |       |
| <b>G</b>  | 0.300    | 0.400 | 0.500 |
| <b>H</b>  | 0.5BSC   |       |       |
| <b>I</b>  | 0.200    | 0.250 | 0.300 |
| <b>J</b>  | 0.250    | 0.300 | 0.350 |

(Unit: mm)

Figure 7. QFN-32 Dimension

### Disclaimer

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