Guangdong Dapu Telecom Technology Co., Ltd

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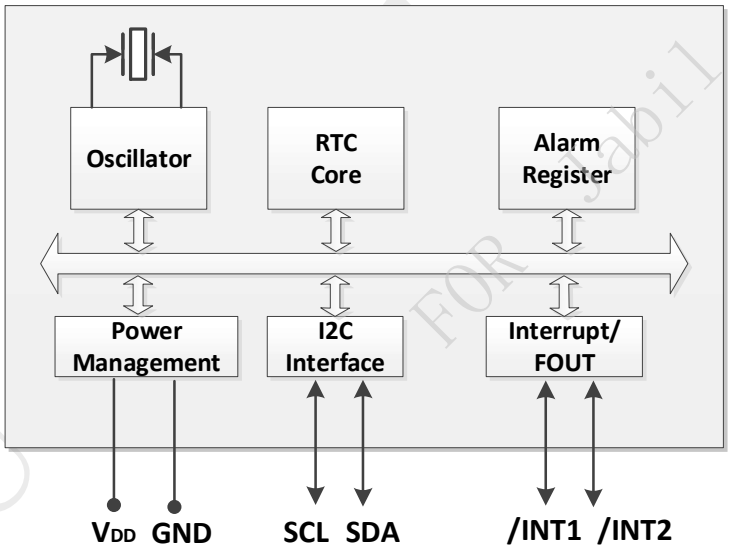
INS5710B —Low Power Consumption I²C RTC

Key Features

- Low current consumption: 0.5uA (Typ.)
- High stability: 5±23ppm @ +25℃
- Build-in XO: 32.768kHz
- Build-in Timer, Alarm, Interrupt and Frequency output
- Communication Interface: I²C bus
- Build-in 128bit RAM
- Power Supply Voltage: 1.6V~5.5V
- Operation Temperature Range: -40℃ ~ +85℃
- Leap years autocorrection
- Package: 4.9mm × 6.0mm × 1.6mm (SOP8)

Block Diagram



Overview

INS5710B is an I²C bus interface real-time clock with low power consumption. It embeds a 32.768kHz XO. It supports calendar (year, month, day, hour, minute, second), timer and alarm function. The SOP8 package makes it suitable to be used in portable electronic devices.

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Revision History

Version	Change Contents	Prepared by	Revised Date
V1.0	Released Version		2021.11.29

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2 Block Diagram

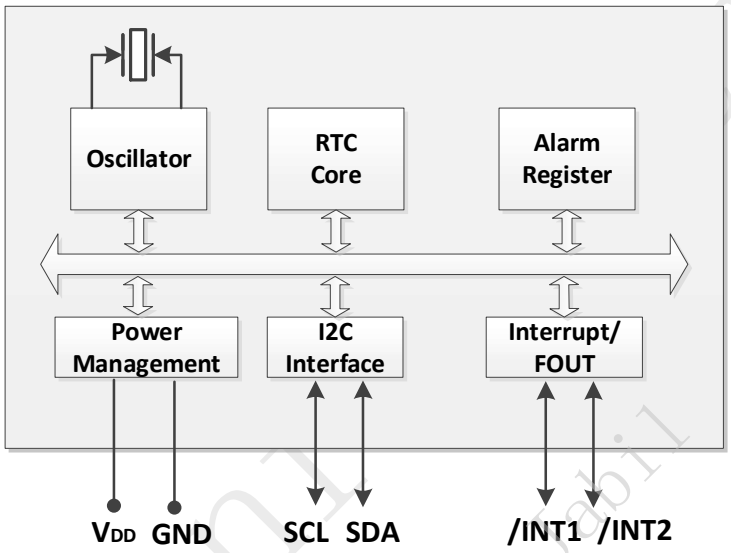

Figure 1. Block Diagram

3 Features

- Low current consumption: 0.5 uA (Typ.)
- High stability: 5±23ppm @ +25℃
- Build-in XO: 32.768kHz
- Communication Interface: I²C bus
- Power Supply Voltage: 1.6V ~ 5.5V
- Operation Temperature Range: -40℃ ~ +85℃
- Leap years autocorrection
- Timer, Interruption and FOUT
- Build-in 128bit RAM
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4 Pin Definition

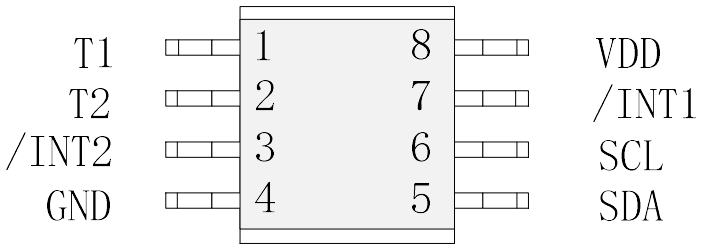

Table1. Pin Definition

Pin Number	Pin Name	I/O	Description
1	T1		Manufacturer test only. Ensure to be floating
2	T2		Manufacturer test only. Ensure to be floating
3	/INT2	Out	This pin can be configured as the output of timer or frequency, effective when Low Voltage (CMOS)
4	GND	-	Ground
5	SDA	In/Out	I2C data signal
6	SCL	In	I2C clock signal
7	/INT1	Out	This pin can be configured as output of Alarm, Timer. Time-update Interruption or Frequency, effective when Low Voltage (Open-Drain)
8	V_{DD}	-	Power in

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5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table2. Absolute Maximum Ratings

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage	V_{DD}	-0.3		6.5	V	
I/O Input Voltage	V_{IN}	GND-0.3		6.5	V	SCL, SDA Input
Clock Output Voltage1	V_{OUT1}	GND-0.3		V_{DD}+0.3	V	/INT2
Clock Output Voltage2	V_{OUT2}	GND-0.3		6.5	V	SDA，/INT1 Output
Storage temperature	T_{STG}	-55		125	℃	

5.2 Recommended Operating Conditions

Table3. Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage (normal mode)	V_{DD}	1.6	3.0	5.5	V	*
Power Supply Voltage (Time keeping)	V_{DD}	1.1	3.0	5.5	V	*
Low Voltage Detection	V_{LOW}			1.3	V	
Input Voltage on Pin	V_{PUP}			5.5	V	SDA ， /INT1
Operation temperature	T_{OPR}	-40	25	85	℃	

Note 1: V_{DD} need to be supplied with more than 1.6V at least for the oscillator to work until stabilization.

5.3 Frequency Characteristics

Table4. Frequency Characteristics

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Frequency stability	$\Delta f_1/f$	5±23			ppm	V_{DD}=3.0V; @+25℃
Temperature Stability	$\Delta f_2/f$	-120		+10	ppm	V_{DD}=3.0V; -20℃ ~ +70℃; Reference frequency @ +25℃
Oscillation start time	t_{STA}			1	s	@25℃
Year Aging	f_a			±5	ppm	First year
FOUT Duty cycle	t_w/t	40	50	60	%	/INT2

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5.4 DC Characteristics

Table5. DC Characteristics

Parameter	Symbol	Value			Unit	Notes	
		Min.	Typ.	Max.			
Average Current1	I_{DD1}		0.52		uA	V_{DD}=5.0V	Input pins are "L" f_{SCL} = 0 Hz, /INT1,2 = OFF, TSEL2="1"
Average Current2	I_{DD2}		0.5			V_{DD}=3.0V	
Average Current3	I_{DD3}		0.6			V_{DD}=5.0V	f_{SCL} = 0 Hz, /INT2 = OFF, /INT1: 32.768 kHz ON
Average Current4	I_{DD4}		0.57			V_{DD}=3.0V	
Average Current5	I_{DD5}		0.6			V_{DD}=5.0V	f_{SCL} = 0 Hz, /INT1 = OFF, /INT2 : 1024 Hz ON ,CL = 15 pF, @25℃
Average Current6	I_{DD6}		0.57			V_{DD}=3.0V	
Input High Voltage	V_{IH}	0.8*V_{DD}		5.5	V	SCL， SDA	
Input Low Voltage	V_{IL}	GND-0.3		0.2*V_{DD}	V		
Output High Voltage	V_{OH1}	4.5		5.0	V	VDD=5V, IOH=-1mA	/INT2
	V_{OH2}	2.7		3.0		VDD=3V, IOH=-0.5mA	
Output High Voltage	V_{OL1}	GND		GND+0.25	V	VDD =5V, IOL=1mA	/INT1
	V_{OL2}	GND		GND+0.4		VDD =3V, IOL=1mA	
	V_{OL3}	GND		GND+0.5		VDD =5V, IOL=1mA	/INT2
	V_{OL4}	GND		GND+0.3		VDD =3V, IOL=0.5mA	
Input Leak Current	I_{LK}	-0.1		0.1	uA	SDA, SCL， V_{IN} = V_{DD} or GND	
Output Leak Current	I_{OZ}	-0.1		0.1	uA	SDA, V_{IN} = V_{DD} or GND	

5.5 AC Characteristics

Table6. AC Characteristics

V_{DD}=1.6V ~ 5.5V; Ta=-40℃ ~ +85℃

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}			400	kHz
SCL Low Voltage Time	t_{LOW}	1.3			us
SCL How Voltage Time	t_{HIGH}	0.6			us
Start condition hold time	$t_{HD;\ STA}$	0.6			us
Start condition setup time	$t_{SU;\ STA}$	0.6			us
Stop condition setup time	$t_{SU;\ STO}$	0.6			us
Bus idle time between start condition and stop condition	t_{RCV}	1.3			us
Data setup time	$t_{SU;\ DAT}$	100			ns
Data hold time	$t_{HD;\ DAT}$	0			ns
SCL, SDA rising time	t_r			0.4	us
SCL, SDA falling time	t_f			0.4	us

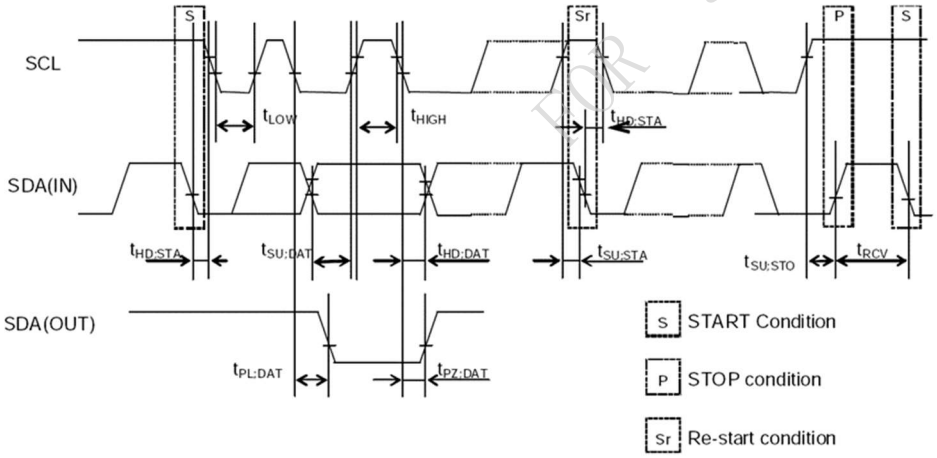

Figure 2. I^2C bus Timing Chart

Note：When the master device gets access to this slave device through I2C, the whole operation duration should be less than 1s, otherwise it will be reset by the I2C bus through the internal bus overtime function.

6 Registers

6.1 Register Lists

Address 0x10~0x1F: Basic Time and Calendar Registers

Address 0x20~0x2F: RAM Register Group

Address 0x30~32: Extended Register Group

Table7. Basic Time and Calendar Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x10	SEC	○	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				R/W
0x11	MIN	○	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R/W
0x12	HOUR	○	○	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0x13	WEEK	○	6	5	4	3	2	1	0	R/W
0x14	DAY	○	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x15	MONTH	○	○	○	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				R/W
0x16	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				R/W
0x17	RSV	Reserved								R/W
0x18	MIN Alarm	AE	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R/W
0x19	HOUR Alarm	AE	●	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0x1A	WEEK Alarm	AE	6	5	4	3	2	1	0	R/W
	DAY Alarm		●	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x1B	Timer Counter 0	128	64	32	16	8	4	2	1	R/W
0x1C	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256	R/W
0x1D	Extension Register	FSEL [1]	FSEL [0]	USEL	TE	WADA	TSEL [2]	TSEL [1]	TSEL [0]	R/W
0x1E	Flag Register	○	○	UF	TF	AF	Reserved	VLF	○	R/W
0x1F	Control Register	TEST	STOP	UIE	TIE	AIE	TSTP	Reserved	Reserved	R/W
0x20~| 0x2F	RAM	●	●	●	●	●	●	●	●	R/W
0x30	RSV	Reserved								R/W
0x31	RSV	Reserved								R/W
0x32	INT Control	○	Reserved	Reserved	Reserved	○	TMPIN	FOPIN1	FOPIN0	R/W

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Note:

1, After power-up reset or in case VLF bit returns "1", make sure to initialize all registers before using the RTC.

2. The default value of register after power on:

Initial 0: TEST、WADA、USEL、TE、FSEL[1:0]、TSEL[1:0]、UF、TF、AF、UIE、TIE、TSTP、TMPIN、FOPIN[1:0].

Initial 1: VLF、TSEL[2].

3.The bits marked with "○" can be read out "0" after initializing.

4.The bits marked with "●" are RAM bits which can be used to write or read any data.

5.Only 0 can be written to UF、TF、AF and VLF bits.

6.Make sure "0" to be written for TEST bits which are used for manufacturing testing only.

6.2 Details of Registers

6.2.1 Clock counter registers

Table8. Second、Minute and Hour Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x10	SEC	○	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				0x00
0x11	MIN	○	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x00
0x12	HOUR	○	○	BCD code, Hour tens place, 0-2		0x00				0x00

SEC: BCD format, Value: 0~59

MIN: BCD format, Value: 0~59

HOUR: BCD format, Value: 0~23

Table9. Week Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x13	WEEK	○	6	5	4	3	2	1	0	0x40

WEEK: Value 01h, 02h, 04h, 08h, 10h, 20h, 40h. Only one bit can be set to 1 each time, all others must be set to 0.

Table10. WEEK Register Value table

WEEK	Data	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sunday	01h	0	0	0	0	0	0	0	1
Monday	02h	0	0	0	0	0	0	1	0
Tuesday	04h	0	0	0	0	0	1	0	0
Wednesday	08h	0	0	0	0	1	0	0	0
Thursday	10h	0	0	0	1	0	0	0	0
Friday	20h	0	0	1	0	0	0	0	0
Saturday	40h	0	1	0	0	0	0	0	0

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Table11. Day Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x14	DAY	○	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				0x01

DAY: BCD format, the value range will be adjusted automatically according to the month setting and if a leap year or not.

Table12. DAY Register Value Range

Month	Day Value Range
1, 3, 5, 7, 8, 10, 12	1~31
4, 6, 9, 11	1~30
February in normal year	1~28
February in leap year	1~29

Table13. Month and Year Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x15	MONTH	○	○	○	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				0x01
0x16	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				0x00

MONTH: BCD format, Value1~12
YEAR: BCD format, Value0~99(2000~2099)
Example: 2020/01/01 Wednesday 21:18:36

Table14. Example of time setting

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x10	SEC	○	0	1	1	0	1	1	0
0x11	MIN	○	0	0	1	1	0	0	0
0x12	HOUR	○	○	1	0	0	0	0	1
0x13	WEEK	○	0	0	0	1	0	0	0
0x14	DAY	○	○	0	0	0	0	0	1
0x15	MONTH	○	○	○	0	0	0	0	1
0x16	YEAR	0	0	1	0	0	0	0	0

6.2.2 Alarm registers

Table15. Alarm Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x18	MIN Alarm	AE	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x00
0x19	HOUR Alarm	AE	●	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				0x00
0x1A	WEEK Alarm	AE	6	5	4	3	2	1	0	0x00
	DAY Alarm		●	BCD code, Day tens		BCD code, Day ones place, 0-9				

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Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
				place, 0-3						

Alarm interruption can be generated with the setting of these registers and the cooperation of AIE、AF and WADA.

WEEK Alarm/Day Alarm: WADA control bit 0x0A can choose week alarm or day alarm, details refer to 0x1D register bit3

AE（Alarm Enable）：Alarm Enable bit，0-Enable；1-Disable.

AF function refer to 0x1E register bit3.

AIE function refer to 0x1F register bit3.

6.2.3 Timer registers

Table16. Timer Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x1B	Timer Counter 0	128	64	32	16	8	4	2	1	0x00
0x1C	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256	0x00

Alarm interruption can be generated with the setting of these registers and the cooperation of TE、TF 、TIE and TSEL[1:0].

TE function refer to 0x1D register bit4.

TF function refer to 0x1E register bit4.

TIE function refer to 0x1F register bit4.

TSEL[1:0] function refer to 0x1D register bit2, bit1 and bit0.

6.2.4 Extension registers

Table17. Extension Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x1D	Extension Register	FSEL [1]	FSEL [0]	USEL	TE	WADA	TSEL [2]	TSEL [1]	TSEL [0]	0x04

Used for the specified functions, including Alarm、 Time Update Interruption、Setting and etc.

WADA（Week Alarm/Day Alarm）： 0-WEEK Alarm, 1-DAY Alarm。

USEL（Update Interrupt Select）：0-Interrupt per Second（Default），1-Interrupt per Minute。

TE（Timer Enable）：0- Disable Timer Interrupt function, 1-Enable Timer Interrupt function。

FSEL[1]，FSEL[0] and FOPIN[1],FOPIN[0] of register 0x32 work coordinately，to confirm the output pin and output frequency. Shown as below table：

Table18. FSEL&FOPIN Table

FOPIN1	FOPIN0	Output pin	FSEL[1]	FSEL[0]	FOUT Frequency
0	0	/INT2 （CMOS）	0	0	Disable
			0	1	1Hz output
			1	0	1024Hz output
			1	1	Reserved

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FOPIN1	FOPIN0	Output pin	FSEL[1]	FSEL[0]	FOUT Frequency
0	1	/INT1 （Open-Drain）	0	0	Disable
			0	1	1Hz output
			1	0	1024Hz output
			1	1	32768Hz Output

TSEL[2]，TSEL[1]，TSEL[0]：Timer/Counter Clock configuration bits, just as below table：

Table19. TSEL Table

TSEL[2]	TSEL[1]	TSEL[0]	Timer/Counter Clock	Interruption duration
0	0	0	4096Hz（244.14us）	122uS
0	0	1	64Hz（15.625ms）	7.813mS
0	1	0	1Hz（S）	7.813mS
0	1	1	1/60Hz（Min）	7.813mS
1	0	0	1/3600Hz（Hour）	7.813mS

6.2.5 Flag Register

Table20. Flag Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x1E	Flag Register	○	○	UF	TF	AF	Reserved	VLF	○	0x26

UF（Update Flag）：Time Update Flag, when time update interruption generates, this bit will change from “0”to “1”,and keep this value until written to “0” by software;

TF（Timer Flag）：Timer Flag, when timer interruption generates, this bit will change from “0”to “1”,and keep this value until written to “0” by software;

AF（Alarm Flag）：Alarm Flag, when Alarm Interruption generation, this bit will change from “0”to “1”,and keep this value until written to “0” by software;

VLF（Voltage Low Flag）：Voltage Low Flag, when voltage is lower than 1.3V ,this bit will be set to”1”, and keep this value until written to “0” by software。

6.2.6 Control Register

Table21. Control Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x1F	Control Register	TEST	STOP	UIE	TIE	AIE	TSTP	Reserved	Reserved	0x00

TEST：Test bit for manufacture，must always be“0” when used and cannot be changed by user;

UIE（Update Interrupt Enable)：When UF changes from“0”to“1”，this bit can control if the interruption generates or not。0-Did not generate（/INT maintain high resistance），1-generate the interruption（/INT changes from high resistance to low voltage）。

TIE（Timer Interrupt Enable）：When TF changes from“0”to“1”，this bit can control if the interruption generates or not。0-Did not generate（/INT maintain high resistance），1-generate the interruption（/INT changes from high resistance to low voltage）。

AIE（Alarm Interrupt Enable）：When AF changes from“0”to“1”，this bit can control if the interruption generates or not。0-Did not generate

（/INT maintain high resistance），1-generate the interruption（/INT changes from high resistance to low voltage）。

TSTP (Timer Stop):This bit is used to stop the count-down timer, always be used with STOP at the same time.

STOP: Used to stop the timer operation. When “STOP=1”, all timer update and calendar stop working. Fixed period timer stops the interruption partly; the output frequency can be 32768Hz, but 1Hz and 1024hz are disable .

Table22. STOP & TSTP Setting Table

STOP	TSTP	Description
0	0	When TSTP is written to“0”，Start timer
	1	When TSTP is written to“1”，Stop timer
1	X	At this moment, when frequency output is set to 64Hz，1Hz，1/60Hz or 1/3600Hz，the timer stop working。

6.2.7 Interruption Register

Table23. Interruption Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x32	INT Control	○	Reserved	Reserved	Reserved	○	TMPIN	FOPIN1	FOPIN0	0x00

1） FOPIN1，FOPIN0 bit

FOPIN[1:0] used to choose the output of FOUT,/INT1 or /INT2。

Table24. FOPIN Setting Table

FOPIN1	FOPIN0	Output Pin
0	0	/INT2(CMOS)
0	1	/INT1(OPEN-DRAIN)

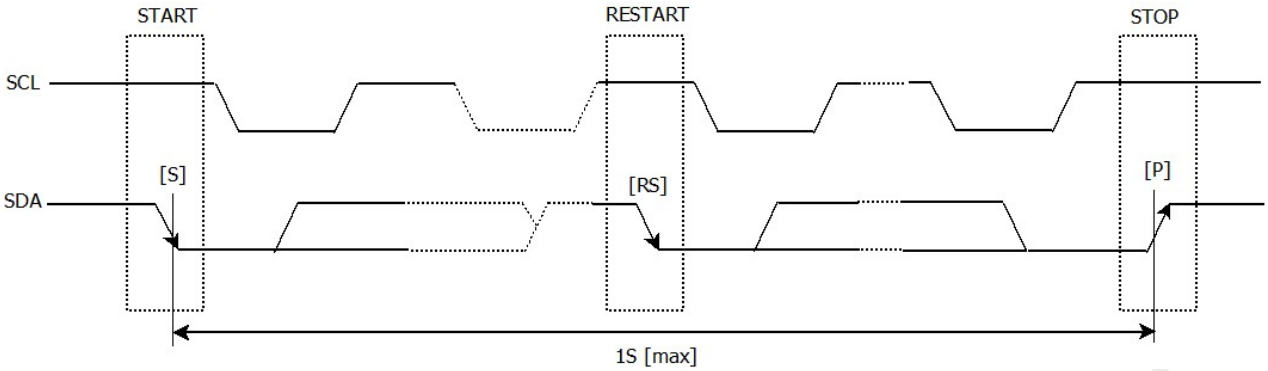
2） TMPIN bit

TMPIN used to choose the output of timer, /INT1 or /INT2.

Table25. TMPIN Setting Table

TMPIN	Output Pin
0	/INT2(CMOS)
1	/INT1(OPEN-DRAIN)

7 I²C Bus Interface



I²C bus supports bi-directional communications through a serial clock line SCL and a serial data line SDA. I²C bus device can be defined as "Master" and "Slave". INS5710B can only be used as Slave.

7.1 Cautions

I²C bus includes START, RESTART, STOP conditions, the duration between START and STOP must be less than 1 second just in case the bus to be set to standby mode automatically. If the time is more than 1S, INS5710B will reset I²C Interface.

INS5710B I²C bus interface supports single byte read/write operations as well as multiple bytes incremental access. After 0xFF address, the next one will be 0x00.

7.2 Slave Address

Table26. I²C Bus Slave Address

Transfer data	Slave address							R/W
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
65h (Read)	0	1	1	0	0	1	0	1 (Read)
64h (Write)								0 (Write)

INS5710B I²C bus Slave Address is [0110 010*].

7.3 I²C bus protocol

It is assumed CPU is master and INS5710B is slave in this section.

7.3.1 Write process

I²C bus includes an address auto-increment function, once the initial address has been specified, the

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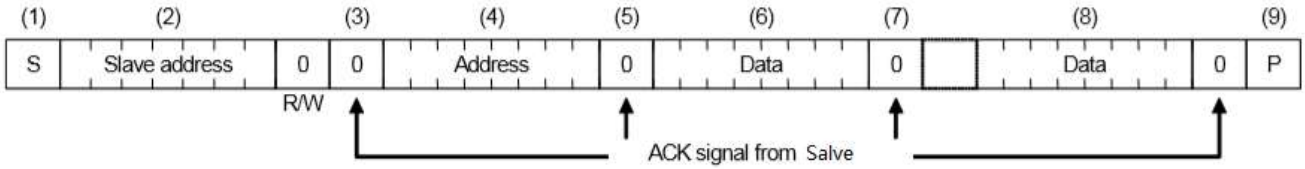
INS5710A increments (+1) the address automatically after each data is sent, then to write next data.

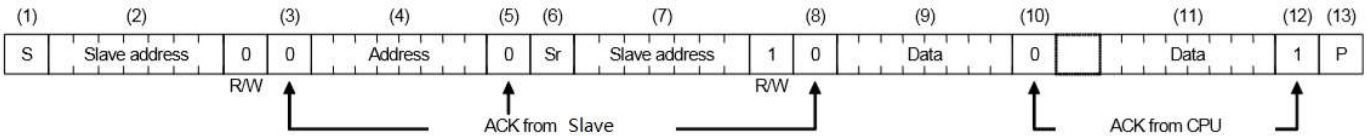
(1) CPU sends start condition[S]
(2) CPU sends INS5710B's slave address with R/W bit to set to write mode
(3) CPU verifies ACK signal from INS5710B
(4) CPU sends write address to INS5710B
(5) CPU verifies ACK signal from INS5710B
(6) CPU sends write data to the address specified at step (4)
(7) CPU verifies ACK signal from INS5710B
(8) Repeat (6) (7) if multiple bytes need to be written, address will be incremented automatically
(9) CPU ends stop condition[P]



7.3.2 Read process

Writing the address to be read with write mode firstly, then reading the data with read mode.

(1) CPU sends start condition[S]
(2) CPU sends INS5710B's slave address with R/W bit to set to write mode
(3) CPU verifies ACK signal from INS5710B
(4) CPU sends address for reading from INS5710B
(5) CPU verifies ACK signal from INS5710B
(6) CPU sends RESTART condition [Sr]
(7) CPU sends INS5710B's slave address with R/W bit to set to read mode
(8) CPU verifies ACK signal from INS5710B
(9) CPU reads data from the specified address in step (4)
(10) CPU verifies ACK signal from INS5710B
(11) Repeat (9) (10) if multiple bytes need to be read, address will be incremented automatically
(12) CPU sends ACK signal for "1"
(13) CPU sends stop condition[P]



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8 Reflow Soldering Curve

Standard: IPC/JEDEC J-STD-020

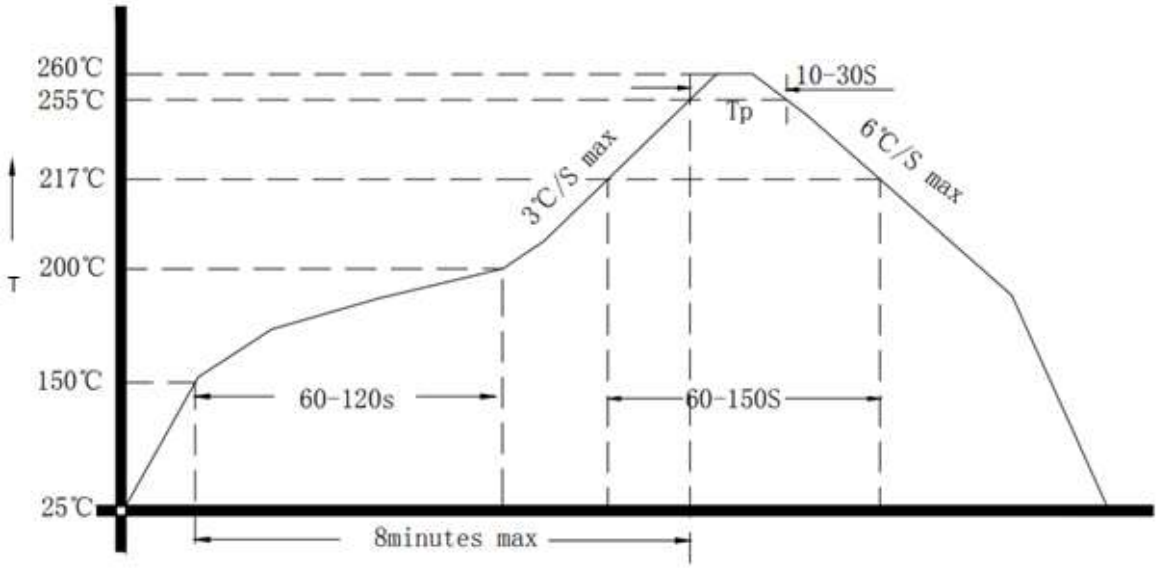
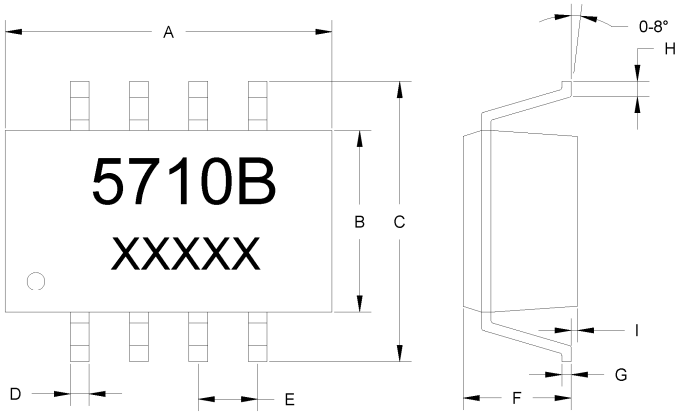


Figure 3. Reflow Soldering Curve

Note: It is suggested to solder IC under the condition shown in the curve above. Must pay attention to the temperature and time when manual soldering, if the temperature over +260℃, or you will make the xo performance bad, even damage it.

9 Dimensions

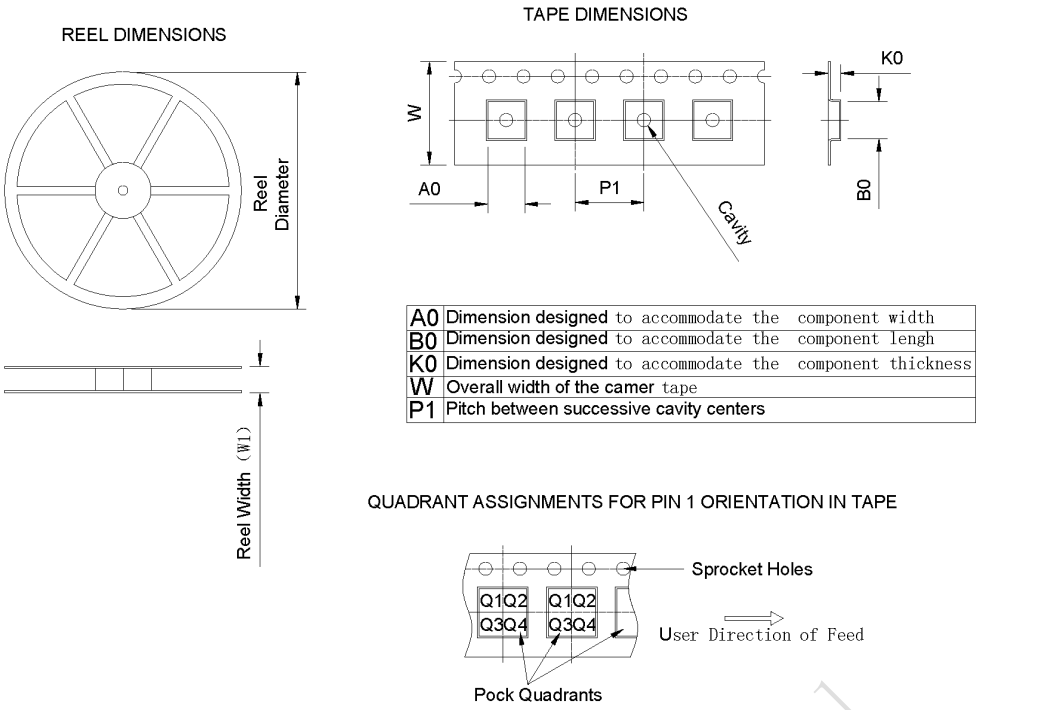


Dimension	Min.	Typ.	Max.
A	4.8	4.9	5.0
B	3.8	3.9	4.0
C	5.8	6.0	6.2
D	0.356	--	0.456
E	--	1.27	--
F	1.3	--	1.6
G	0.203	--	0.233
H	0.4	0.6	0.8

(Unit: mm)

Figure 4. Dimension

10 Package Information



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
			8		330±1	12.4±0.2	6.40	5.30	2.10	8.00±0.1	12.00±0.1

Figure 5. Package information