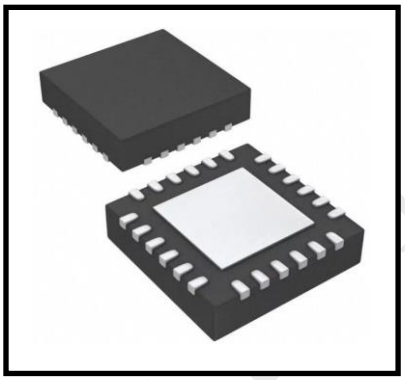
Guangdong Dapu Telecom Technology Co., Ltd

http：//www.dptel.com

Bldg. 5, SSL Modern Enterprise Accelerator Zone, Dongguan City, Guangdong Province, PRC China
TEL:0086-0769-88010888
FAX:0086-0769-81800098

INS6110 —1：10 Low-Jitter Clock Buffer

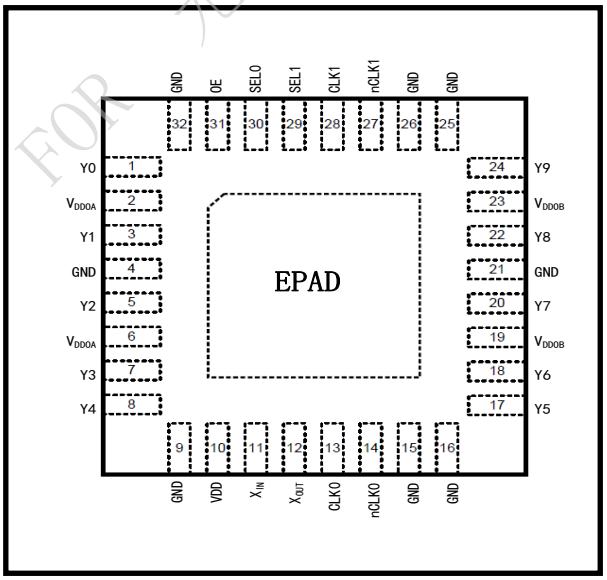


FEATURES

- 10 Single-Ended LVCMOS Outputs（DC~200MHz）
- 3 Clock Inputs
  - 2 Differential or Single-Ended Inputs（DC~200MHz）
  - 1 Crystal Input（8~50MHz）or Single-Ended（DC~50MHz）
- Additive Phase Noise/Jitter: 50fs RMS(Typ.)@25MHz（12KHz~20MHz）
- Output Power Supply：1.5V, 1.8V, 2.5V or 3.3V
- Core Power Supply：2.5V or 3.3V
- Temperature：-40℃~+85℃
- Package：QFN32（5.0mm x 5.0mm x 0.75mm）
- RoHS

APPLICATIONS

- High-Speed Clock Distribution
- Wireless and Wired Communications
- Medical Imaging
- Measurement



DESCRIPTION

The INS6110 is a low-jitter clock fan-out buffer. It can distribute to ten LVCMOS clock outputs from one clock input which is selected from two differential/single-ended clock inputs and a crystal input.

Bldg. 5, SSL Modern Enterprise Accelerator Zone, Dongguan City, Guangdong Province, PRC China
TEL:0086-0769-88010888
FAX:0086-0769-81800098

Revision History

Version	Change Contents	Prepared by	Revised Date
V1.0	First Version		2021.05.25
V1.1	1. Change the height from 0.9±0.1mm to 0.75±0.05mm 2. Change the size of thermal pad 3. Update the table 10.		2021.10.29

Bldg. 5, SSL Modern Enterprise Accelerator Zone, Dongguan City, Guangdong Province, PRC China
TEL:0086-0769-88010888
FAX:0086-0769-81800098

TABLE OF CONTENTS

Bldg. 5, SSL Modern Enterprise Accelerator Zone, Dongguan City, Guangdong Province, PRC China
TEL:0086-0769-88010888
FAX:0086-0769-81800098

1 Description

The INS6110 is a low-jitter clock fan-out buffer. It can distribute to ten LVCMOS clock outputs from one clock input which is selected from two differential/single-ended clock inputs and a crystal input.

Based on advanced CMOS technology and process, the INS6110 can output 10 LVCMOS clocks with low-jitter, low-skew and low propagation-delay. The input clock frequency range is from DC to 200MHz. The INS6110 could flexibly realize the clock signal level shifter with a 3.3V/2.5V core power and two flexible 3.3V/2.5V/1.8V/1.5V output powers.

Such a buffer is good for use in wireless and wired communications, medical imaging, measurement, etc.

The INS6110 package is QFN32(5.0mm x 5.0mm x 0.75mm).

2 Block Diagram & Pin Assignment

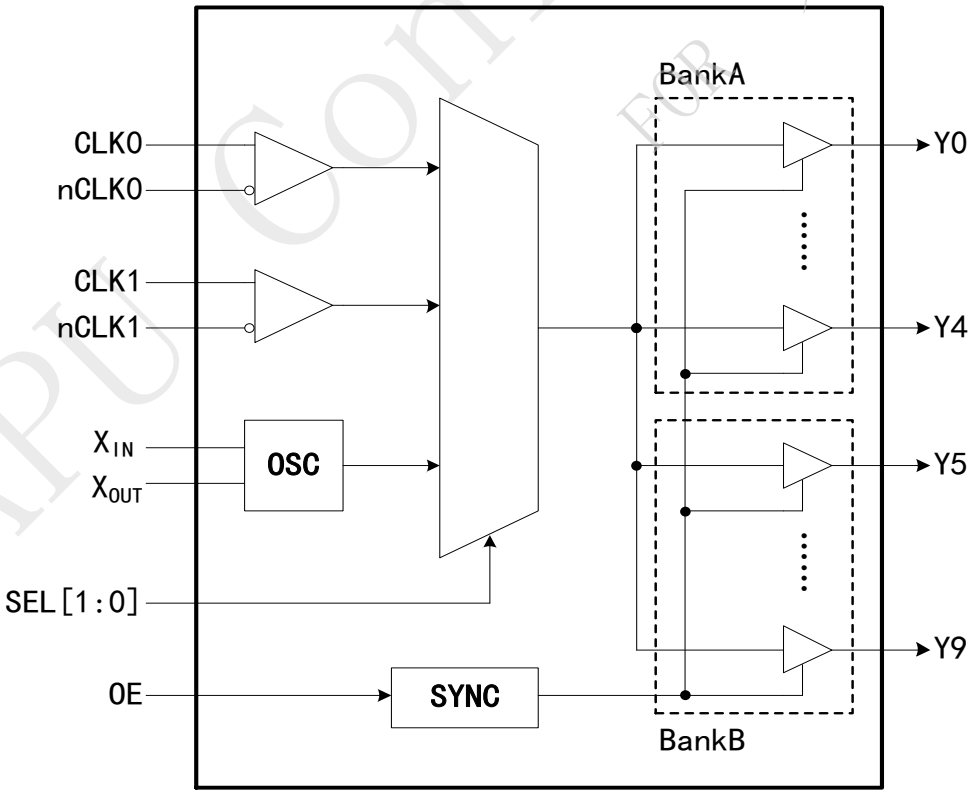


Figure 1. Block Diagram

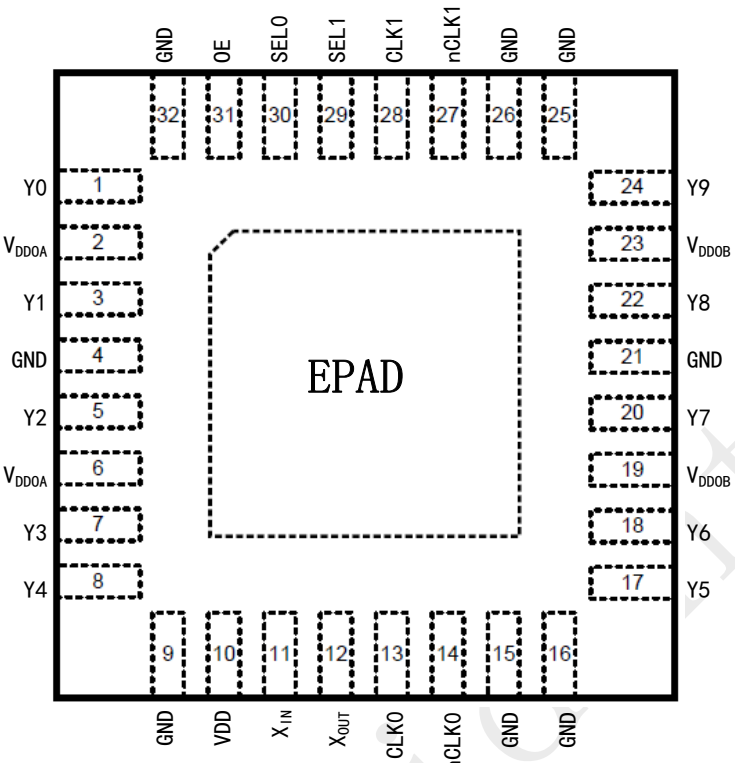


Figure 2. Pin Assignment

Table 1.Pin Descriptions

Number	Name	Type	Description
1	Y0	OUT	LVCMOS Clock Output0
2, 6	V_{DDOA}	PWR	BankA Output Supply
3	Y1	OUT	LVCMOS Clock Output 1
4, 9, 15, 16, 21, 25, 26, 32	GND	GND	GND
5	Y2	OUT	LVCMOS Clock Output 2
7	Y3	OUT	LVCMOS Clock Output 3
8	Y4	OUT	L LVCMOS Clock Output 4
10	V_{DD}	PWR	Core Power Supply
11	X_{IN}	IN	Crystal Input
12	X_{OUT}	OUT	Crystal Output
13	CLK0	IN	Non-inverting differential input clock0
14	nCLK0	IN	Inverting differential input clock0
17	Y5	OUT	LVCMOS Clock Output 5
18	Y6	OUT	LVCMOS Clock Output 6
19, 23	V_{DDOB}	PWR	BankB Output Supply

Bldg. 5, SSL Modern Enterprise Accelerator Zone, Dongguan City, Guangdong Province, PRC China
TEL:0086-0769-88010888
FAX:0086-0769-81800098

20	Y7	OUT	LVCMOS Clock Output 7
22	Y8	OUT	LVCMOS Clock Output 8
24	Y9	OUT	LVCMOS Clock Output 9
27	nCLK1	IN	Inverting differential input clock1
28	CLK1	IN	Non-inverting differential input clock1
29	SEL1	IN	Input clock selection 1, pull down
30	SEL0	IN	Input clock selection 0, pull down
31	OE	IN	Output enable, pull down 0：disable clock output, High-Impedance 1：enable clock output
	EPAD		The Exposed thermal Pad. Must be connected with GND.

* IN：Input Signal
OUT：Output Signal
PWR：Power Supply
GND：Ground
EPAD：Exposed thermal PAD

3 Electric Parameter

Table 2. Absolute Maximum Ratings

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Parameter	Symbol	Rating	Unit	Comments
Power Supply	V_{DD} V_{DDOA} V_{DDOB}	-0.5~4.6	V	
Input Voltage	V_{IN}	-0.5~V_{DD}+0.5	V	
Output Voltage	V_{OUT}	-0.5~V_{DDOA}/V_{DDOB}+0.5	V	
Storage Temperature Range	T_{STG}	-65~150	℃	
Maximum Junction Temperature	T_J	125	℃	
Thermal Impedance	θ_{JA}	50	℃/W	

Table3 Recommended Operating Conditions

Bldg. 5, SSL Modern Enterprise Accelerator Zone, Dongguan City, Guangdong Province, PRC China
TEL:0086-0769-88010888
FAX:0086-0769-81800098

Test Condition: -40℃≤T_A≤85℃; It is recommended that the chip operates with the rated electrical range indicated in the table below.

Parameter	Symbol	Value			Unit	Comments
		Min.	Typ.	Max.		
Core Power Supply	V_{DD}	3.135	3.3	3.465	V	
		2.375	2.5	2.625		
Output Supply	V_{DDOX} (1)	3.135	3.3	3.465	V	
		2.375	2.5	2.625		
		1.6	1.8	2		
		1.35	1.5	1.65		
Static Device Current	I_{VDD}		14		mA	V_{DD}/V_{DDOX}=3.3V
			8		mA	V_{DD}/V_{DDOX}=2.5V
			20		mA	Crystal input
Power dissipation capacitance per output	C_{PD} (1)		9		pF	V_{DDOX} =3.3V, F_{OUT}=100MHz
			8.5		pF	V_{DDOX} =2.5V, F_{OUT}=100MHz
			8		pF	V_{DDOX} =1.8V, F_{OUT}=100MHz
			7.5		pF	V_{DDOX} =1.5V, F_{OUT}=100MHz
Operating Temperature Range	T_A	-40		85	℃	

*（1）DDOX: DDOA/DDOB

Table 4.Control Signal Characteristics

Test Condition：-40℃≤T_A≤85℃, 2.375V≤V_{DD}≤3.465V, 1.35V≤V_{DDOX}≤V_{DD}, $F_{IN/OUT}$=100MHz; Unless otherwise noted.

Parameter	Symbol	Value			Unit	Comments
		Min.	Typ.	Max.		
Control Signals（OE, SEL0, SEL1）						
Input High Current	I_{IH}			40	uA	
Input Low Current	I_{IL}	-40			uA	
Input High Voltage	V_{IH}	0.7*V_{DD}			V	
Input Low Voltage	V_{IL}			0.3*V_{DD}	V	

Table 5.CLKx/nCLKx (2) Characteristics

Test Condition：-40℃≤T_A≤85℃, 2.375V≤V_{DD}≤3.465V, 1.35V≤V_{DDOX}≤V_{DD}, $F_{IN/OUT}$=100MHz; Unless otherwise noted.

Parameter	Symbol	Value			Unit	Comments
		Min.	Typ.	Max.		

Bldg. 5, SSL Modern Enterprise Accelerator Zone, Dongguan City, Guangdong Province, PRC China
TEL:0086-0769-88010888
FAX:0086-0769-81800098

CLKx/nCLKx DC Characteristic						
Input High Current	I_{IH}			40	uA	$V_{CLK}=V_{DD}$
Input Low Current	I_{IL}	-40			uA	V_{CLK}=0V
Single-Ended Input DC Characteristic（CLKx）(3)						
Input High Voltage	V_{IH}	$0.7*V_{DD}$		$V_{DD}+0.3$	V	
Input Low Voltage	V_{IL}	-0.3		$0.3*V_{DD}$	V	
Differential Input DC Characteristic（CLK/nCLK）						
Differential Input Voltage Swing	V_{ID}	0.15		1.3	V	
Input Common-mode Voltage	V_{CM}(4)	0.5		$V_{DD}-0.85$	V	
AC Characteristic（CLK/nCLK）						
Input frequency	F_{IN}	0		200	MHz	
Input duty cycle	Duty Cycle	40	50	60	%	

*（2）CLKx/nCLKx: CLK0/nCLK0 和 CLK1/nCLK1

（3）When Differential Input with Single-Ended Interconnect, nCLK must be AC coupled to GND or reference bias voltage to meet V_{CM}.

（4）When input signal's common-mode voltage is bigger than V_{CM}'s Max., must be AC coupled.

Table 6. X_{IN}/X_{OUT} Characteristics

Test Condition: -40℃≤T_A≤85℃, 2.375V≤V_{DD}≤3.465V, 1.35V≤V_{DDOX}≤V_{DD}; Unless otherwise noted.

Parameter	Symbol	Value			Unit	Comments
		Min.	Typ.	Max.		
Crystal						
Mode of Crystal			Fundamental			
Frequency	$F_{XIN/XOUT}$	8		50	MHz	
Equivalent Series Resistance	ESR		50		Ω	
Maximum Shunt Capacitance	C_{XO}		7		pF	
Drive Level	P_{XIN}		100		uW	
XIN/XOUT Characteristics						
Chip Capacitance	C_{ONCHIP}		12		pF	
Single-Ended Characteristics(Overdrive Mode)						

Frequency	F_{XIN}			50	MHz	X_{OUT} float
Input signal swing	V_{SWING}			2	V	
Single-Ended Characteristics(Bypass Mode)						
Frequency	F_{XIN}			50	MHz	X_{OUT} float
Input High Voltage	V_{XINH}	$0.7*V_{DD}$		$V_{DD}+0.3$	V	
Input Low Voltage	V_{XINL}	-0.3		$0.3*V_{DD}$	V	

Table 7. LVCMOS Characteristics (5)

Test Condition：-40℃≤T_A≤85℃, 2.375V≤V_{DD}≤3.465V, 1.35V≤V_{DDOX}≤V_{DD}, $F_{IN/OUT}$=100MHz, C_L=5pF//50Ω；Unless otherwise noted.

Parameter	Symbol	Value			Unit	Comments
		Min.	Typ.	Max.		
Output High Voltage	V_{OH}	$0.8*V_{DDOX}$			V	V_{DDOX}=2.375～3.465V
		$0.7*V_{DDOX}$			V	V_{DDOX}=1.35～2V
Output High Voltage	V_{OL}			$0.2*V_{DDOX}$	V	V_{DDOX}=2.375～3.465V
				$0.3*V_{DDOX}$		V_{DDOX}=1.35～2V
Output impedance	R_O		15		Ω	V_{DDOX}=3.3V
			20		Ω	V_{DDOX}=2.5V
			25		Ω	V_{DDOX}=1.8V
			30		Ω	V_{DDOX}=1.5V
Output Frequency	F_{OUT}	0		200	MHz	
Duty Cycle	Duty Cycle	45	50	55	%	
Output Skew	t_{Skew} (6)		30	50	ps	
Part-to-part skew	t_{PDP} (6)			2	ns	
Output Delay	t_{Delay}	1.5	1.95	4.0	ns	V_{DD}=3.3V V_{DDOX}=1.35V～ V_{DD}
		1.8	2.4	4.4	ns	V_{DD}=2.5V V_{DDOX}=1.35V～ V_{DD}
Rise/Fall Time	t_{Rise} /t_{Fall}		250		ps	V_{DD}=3.3V V_{DDOX}=1.8V C_L=10pF
			275		ps	V_{DD}=2.5V V_{DDOX}=2.5V C_L=10pF
			315		ps	VDD=3.3V VDDOX=3.3V CL=10pF

Additive RMS Phase Jitter（RMS）	t_J		50		fs	F_{OUT}=25MH Input skew rate ≥ 2V/ns C_L=5pF 12kHzto20MHz
Output enable or disable time	t_{EN}			2	Cycle	
MUX isolation	Isolation	55			dBc	125MHz

* （5）LVCMOS AC Parameters are dependent upon output capacitive loading

（6）Parameter is specified by design, not tested in production

4 Function Description

Control Signals

The INS6110 has 3 control signals: SEL0, SEL1 and OE.

SEL0, SEL1: Clock input selection is controlled using the SEL0 and SEL1 as shown in Table 8.

Table 8. Input Selection

SEL1	SEL0	Input Clock
0	0	CLK0/nCLK0
0	1	CLK1/nCLK1
1	0	X_{IN}/X_{OUT} or Overdrive Mode
1	1	Bypass Mode

Overdrive Mode: LVCMOS drives X_{IN} with AC couple

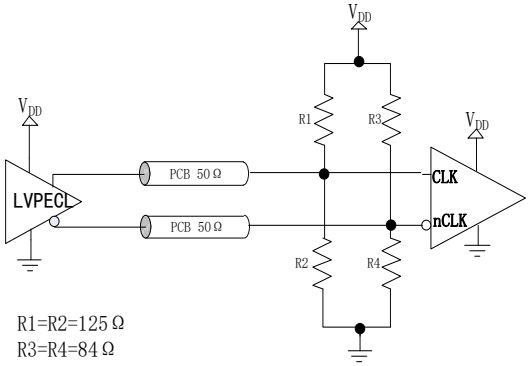
Bypass Mode: LVCMOS drives X_{IN} with DC couple

OE: Output Enable. When OE is held high, the output clocks are enabled. When it is held low, the output clocks are held in a high-impedance state as shown in Table 10.

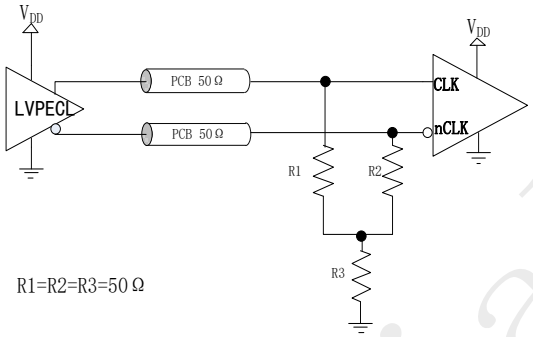
Input Clock

Differential Input(CLK/nCLK)： The CLK/nCLK accepts LVDS, LVPECL, SSTL, HCSL differential signals. Signals must meet the characteristics in Table 5. Figures 3 show interface examples for the CLK/nCLK input with built-in 50Ω terminations driven by the most common driver types.

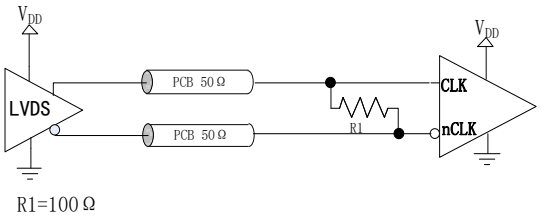
Bldg. 5, SSL Modern Enterprise Accelerator Zone, Dongguan City, Guangdong Province, PRC China
TEL:0086-0769-88010888
FAX:0086-0769-81800098



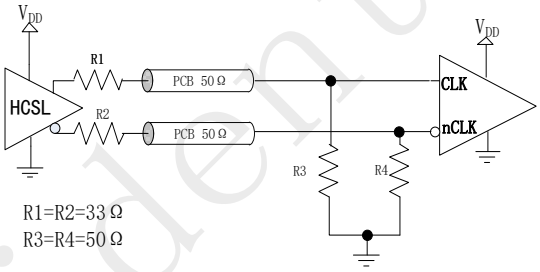
(a)LVPECL Input(Thevenin Parallel Termination)



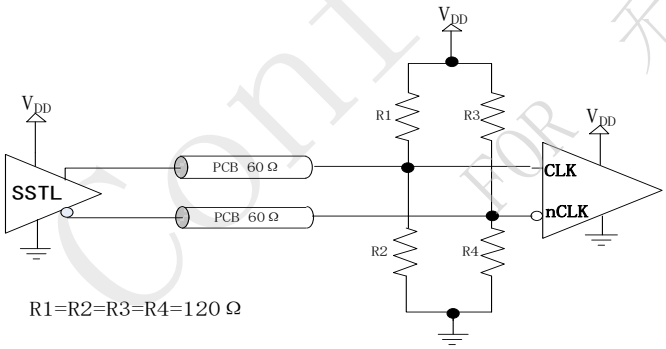
(b)LVPECL Input（“Y” Parallel Termination）



(c)LVDS Input



(d)HCSL Input



(e)SSTL Input

Figure 3. Differential Input Drives CLK/nCLK

Note

- A differential input signal is recommended over single-ended because it typically provides higher slew rate and common-mode noise rejection. It supports wider frequency range and brings better phase noise and jitter performance;
- When input signal's common-mode voltage is bigger than VCM's Max., must be AC coupled to meet characteristics in Table 5;
- For applications not requiring the use of the differential input, both CLK and CLK can be left floating.

Single-Ended Input (CLK/nCLK)：CLK/nCLK also supports LVCMOS input through couple circuit to meet characteristics in Table 5.

Refer to Figure 4, R1 is impedance matching of driver and is placed near the driver; When LVCMOS is 3.3V/2.5V, R2/R3(100Ω) is terminal impedance matching and is placed near the CLK pin; Because of half of the single-ended swing of the driver (V_{DD}/2) drives CLK, nCLK should be externally biased to the midpoint voltage of the attenuated (V_{DD}/2).

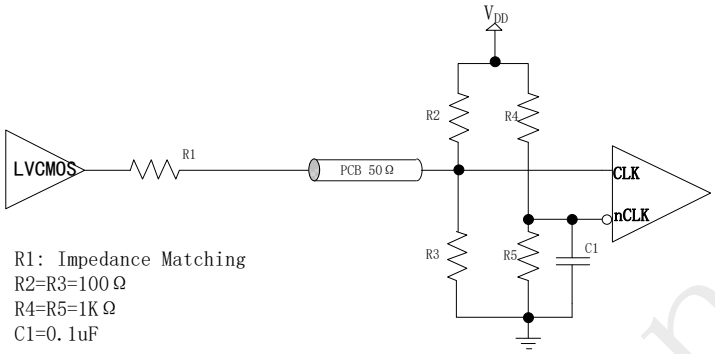


Figure 4. LVCMOS Drives CLK/nCLK

X_{IN}/X_{OUT}: Accept both crystal input and single-ended LVCMOS signals in overdrive and bypass modes. In overdrive mode, it is necessary to ac-couple the input with a capacitor (see Figure 5). Otherwise, in bypass mode, there is no requirement for a coupling capacitor.

When SEL1 is low level, XIN/XOUT could be left floating; When SEL1 is high level, X_{IN} must not be left floating.

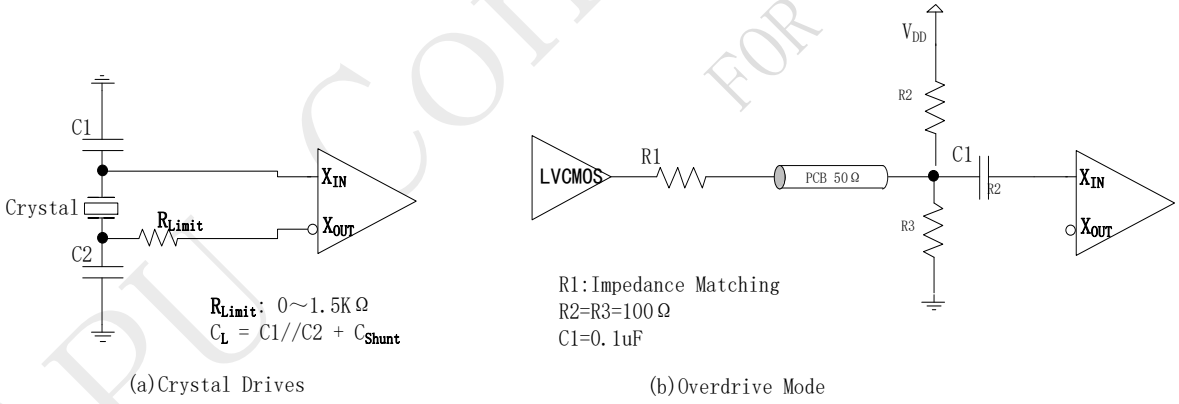


Figure 5. X_{IN}/X_{OUT}

Output Clock

The INS6110 has two separated banks of clock output (Table 9).

Table 9.Bank of Clock Output

Bank	Output Clock
BankA	Y0, Y1, Y2, Y3, Y4
BankB	Y5, Y6, Y7, Y8, Y9

Output impedance is listed in Table 7.

Bldg. 5, SSL Modern Enterprise Accelerator Zone, Dongguan City, Guangdong Province, PRC China
TEL:0086-0769-88010888
FAX:0086-0769-81800098

Table 10.Clock Output States

OE	SEL[1]	Input Clock	Output Clock
H(7)	0	CLKx=Open nCLKx=Open	L
		CLKx=H nCLKx=L	H
		CLKx=L nCLK=H	L
	1	X_{IN}/X_{OUT}	Active(10)
L(8)	X(9)	X	High Impedance

* (7) H: High Level
(8) L: Low Level
(9) X: Do Not Care
(10) Output Clock is depended on X_{IN}/X_{OUT}.

Note

- Unused outputs should be left floating

Power Supply

The INS6110 separates the core and the output power supplies which allow the output buffers to operate at the same supply as the core supply or at a lower supply voltage. Independent supplies could enable lower power consumption and output-level compatibility.

BankA (Y0-Y4) and BankB (Y5-Y9) may also be operated at different V_{DDOA} and V_{DDOB} voltages.

The core supply (V_{DD}) supports 2.5V and 3.3V, and the output supplies (V_{DDOA} and V_{DDOB}) supports 3.3V, 2.5V, 1.8V, and 1.5V.

Note

- V_{DDOA} and V_{DDOB} must not exceed V_{DD}.
- Don't connect V_{DDOA}/V_{DDOB} to ground.

Bldg. 5, SSL Modern Enterprise Accelerator Zone, Dongguan City, Guangdong Province, PRC China
TEL:0086-0769-88010888
FAX:0086-0769-81800098

5 Environment

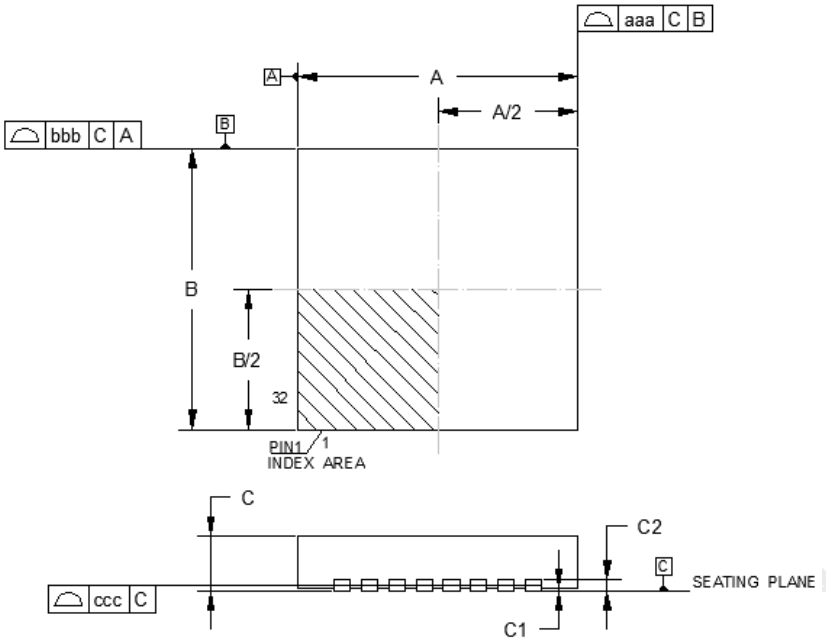
Table 11. Environment

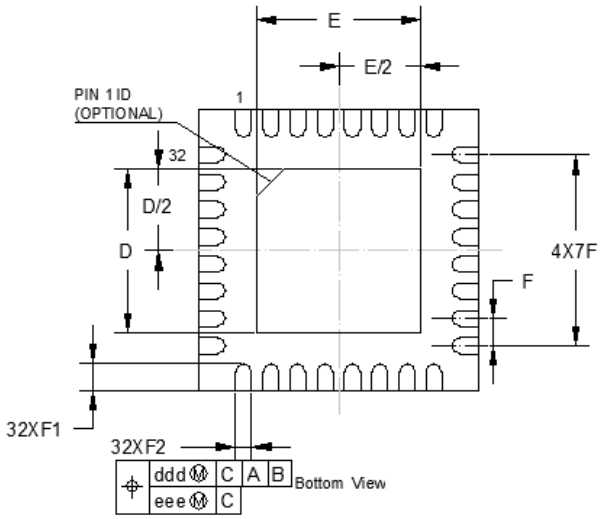
Attribute	Value	Unit	Comments
ESD Level	±2500V	V	HBM, refer to ANSI/ESDA/JEDEC JS-001
	±1000V	V	CDM, refer to JEDEC specification JESD22-C101
Moisture Sensitivity	Level 3		
RoHS	RoHS2.0		

* HBM: Human body model

CDM: Charged-device model

6 Package Dimensions

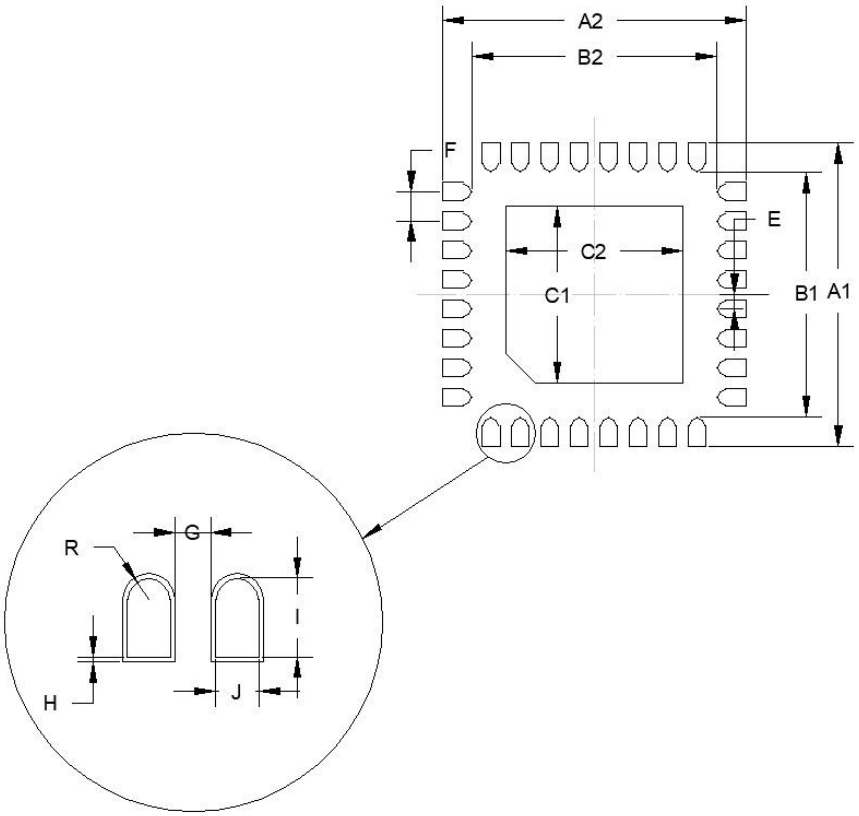




Dimensions	Min.	Typ.	Max.
A	4.85	5.00	5.15
B	4.85	5.00	5.15
C	0.70	0.75	0.80
C1	--	--	0.05
C2	--	--	0.20
D	3.30	3.40	3.50
E	3.30	3.40	3.50
F	--	0.50	--
F1	0.30	0.40	0.50
F2	0.18	--	0.30
aaa	--	--	0.15
bbb	--	--	0.10
ccc	--	--	0.08
ddd	--	--	0.10
eee	--	--	0.10

Figure 6. Package Outline（QFN32）

Bldg. 5, SSL Modern Enterprise Accelerator Zone, Dongguan City, Guangdong Province, PRC China
TEL:0086-0769-88010888
FAX:0086-0769-81800098



Dimensions (mm)	
A1	5.15
A2	5.15
B1	4.15
B2	4.15
C1	3.00
C2	3.00
E	0.25
F	0.5
G	0.08
H	0.07
I	0.50
J	0.30
R	0.15

Figure 7. SOLDERING FOOTPRINT RECOMMENDED（QFN32）

Note:

1. All linear dimensions are in millimeters.
2. EPAD must be soldered to PCB