ABOUT THE ACS9522

This is the datasheet for the DPSync ASSP ACS9522 variant. The datasheet should be read in conjunction with the ACS9522 user guide, API documentation and other information available at the DPSync Resource Center[1].

There are many applications in which it is necessary to lock a remote clock signal to a central frequency source, and there are other applications which require the alignment of a clock to a central source of time. The ACS9522 combines DAPU's synchronous equipment timing source (SETS) functionality and DPSync packet timing technology and can therefore be used for both applications.

In this datasheet, the words SETS and TDM Block are synonymous, and both terms are used.

SETS functionality is used for frequency-locking applications in SDH/SONET and Ethernet equipment. DPSync technology combines the IEEE 1588 v2 protocol with DAPU's patented packet delay filtering algorithms, which allow a reference clock to be transported across a packet switched network without special adaptations of switches or routers in the network. It is ideal for carrying timing across a legacy packet switched network. IEEE 1588 is often known as precision time protocol (PTP), the acronym that is generally used in this document.

The ACS9522 supports:

Timebase derived from:
PTP slave, SONET/SDH recovered clock, BITS/SSU input, SyncE recovered clock, GPS, 1PPS, precision holdover.
Physical layer clock sources are jitter and wander attenuated according to G.812, G.813, G.8261, G.8262, GR-1244-CORE, GR253 etc.

Technology bridging:
Derive timing from one input technology (SONET, SDH, SyncE, PTP) and provide timing to all output technologies simultaneously.

PTP Grandmaster:
PTP Grandmaster function supports multiple PTP slaves using multicast or unicast messaging. Timebase may be PTP or ARB.

PTP Slave:
Acting as a PTP Ordinary Clock in Slave mode, the ACS9522 can lock to BCs or TCs, or it can use sophisticated packet delay filters and adaptation algorithms to lock to a remote PTP Grandmaster over a multi-hop legacy network which has no PTP support.

TDM/clocks:
Includes all DAPU SETS family functions for physical layer input and output synchronization.

SyncE:
Integrates DAPU eSETS technology for the physical layer input and output synchronization of Ethernet PHY devices.

Self test - the device self-checks for consistency and makes rudimentary checks of the external Ethernet PHYs.

FEATURES

PTP timing features

- PTP Grandmaster selection - automatic or manual PTP master/slave mode selection.
- Powerful network delay analysis - full time-alignment in the slave over hostile networks (Layer 2 or Layer 3 networks).
- Dynamic adaptation - to network delay variations. Network loading change tolerant (e.g., ramps and steps).
- Time alignment - better than ±1 µs on a managed 10-switch GbE network under G.8261[20] test conditions.*
- Frequency alignment - better than ±10 ppb on a managed 10-switch GbE network under G.8261[20] test conditions.*

TDM timing features

- Programmable TDM timing bandwidth - for wander and jitter tracking/attenuation, 0.1 Hz to 70 Hz in 10 steps.
- Automatic hit-less source switchover - on loss of input.
- Output clock phase adjustment - in 6 ps steps to ±200 ns.

Device features

- Fully integrated - integrates hardware precision timestamping with on-the-fly insertion. Powerful integrated processor and clock recovery algorithm for PTP.
- Timing synchronization on a chip - supporting transitions from legacy circuit networks to new packet technology.
- Suitable applications - Stratum 3, 3E, 4E, 4, SONET Minimum Clock (SMC) or SONET/SDH Equipment Clock (SEC) or Ethernet, IEEE1588[13] PTP, Synchronous Ethernet, Ethernet Equipment Clock.
- Clocks - 18 clock inputs and 11 clock outputs.
- Precision holdover - in all modes.
- Ports - 2 x SGMII, serial interface and JTAG.
- Time-of-day - PPnS top-of-second signal plus current-time-since-epoch message on a UART.
- Output characteristics:
  Time-aligned output pair:
  1 PPS and 125 MHz divided by n (n = 4 to 125000).
  Frequency-aligned outputs:
  1 Hz and programmable frequency 1 kHz to 62.5 MHz.
  Low jitter frequency-aligned outputs:
  SONET and SDH OC-n rates: 3.84 MHz to 155.52 MHz.
  SyncE rates: 25 MHz, 50 MHz, 62.5 MHz and 125 MHz.
- Local oscillator: ±20 ppm or better.
- LBGA package: 324 pin, 19 mm x 19 mm.
  Lead-free - RoHS[26] and WEEE[27] compliant.
- External RAM not required.

A simplified system diagram is shown in Figure 1.

* This is an indication of DAPU tested performance and is not guaranteed across all types of switches and network conditions. Please contact DAPU DPSync support for further details.

System diagram

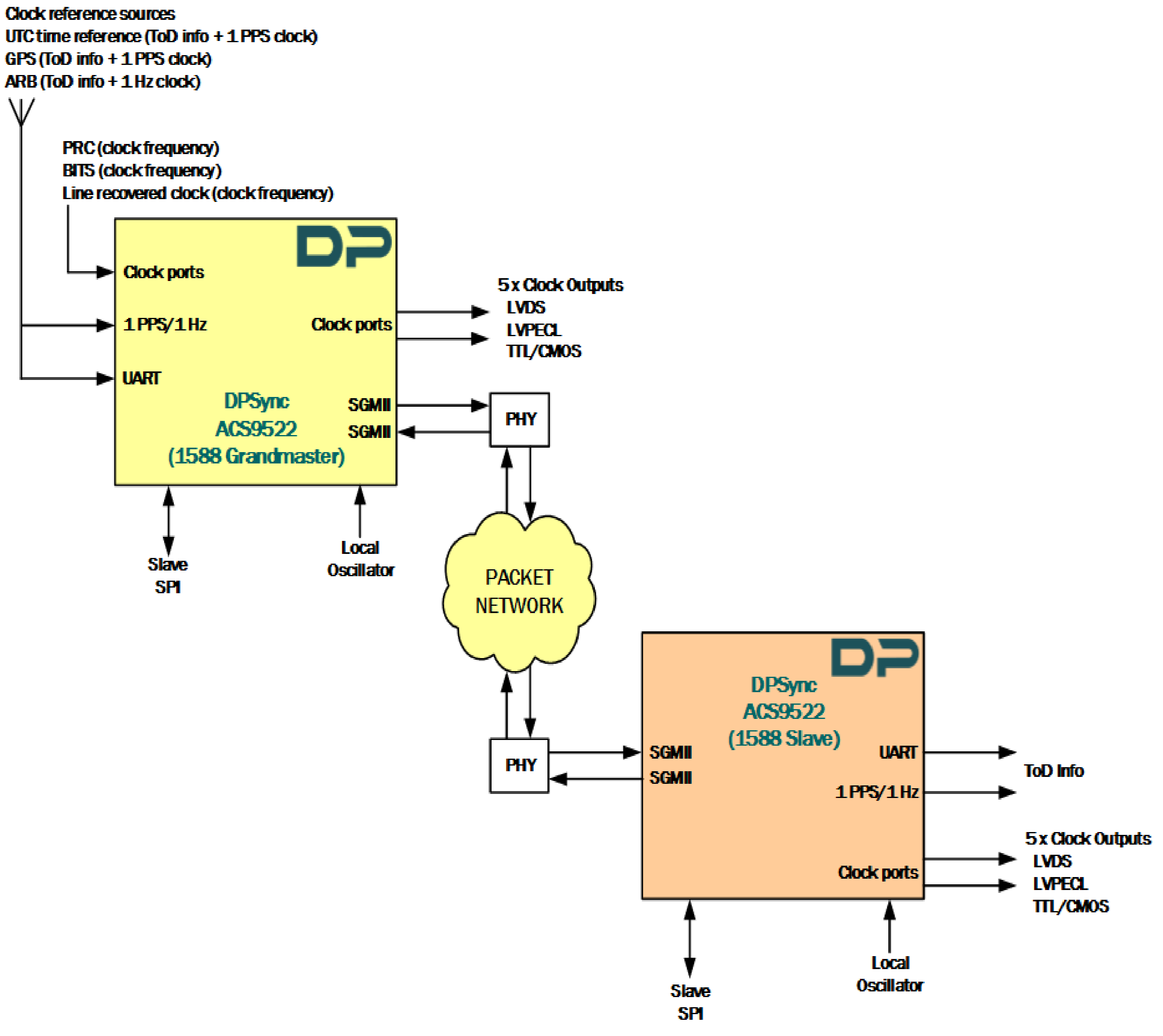

Figure 1 - Simplified system diagram - ACS9522 DPSync in PTP Grandmaster and Slave modes

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OVERVIEW

Figure 2 is a block diagram of the ACS9522 device, showing that it contains both TDM and PTP blocks. These blocks can be used separately or in conjunction with each other to provide a highly-flexible, multi-role device that can provide clock timing in traditional TDM equipment, or packet-timing in next-generation packet switching equipment. For packet-timing, the device supports packet-based timing transfer using Precision Time Protocol, and physical-layer-based timing transfer using Synchronous Ethernet.

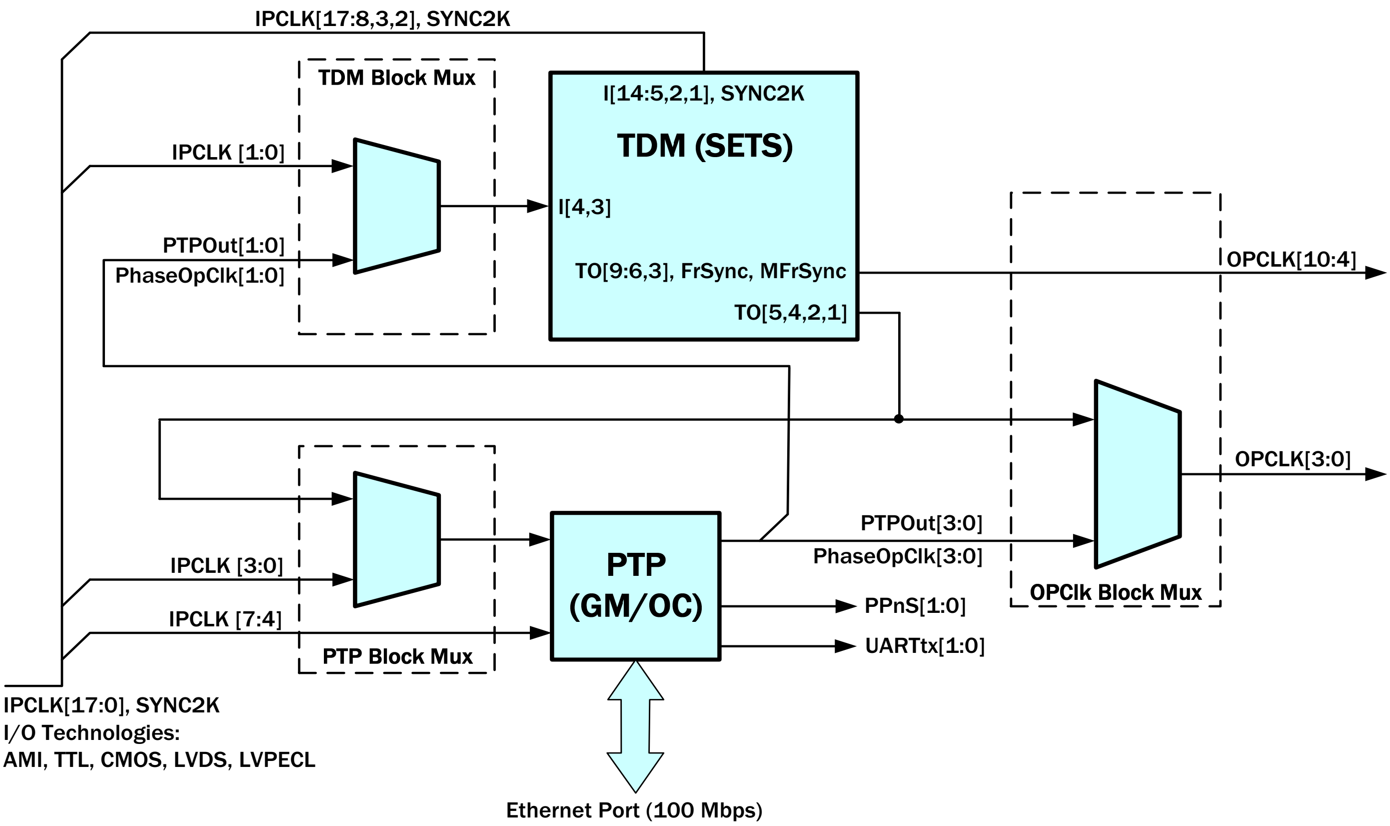

Figure 2 - Overall block diagram of the ACS9522

Physical layer timing

The TDM Block can be used to provide a dedicated SETS function independent of PTP operation. In SDH/SONET equipment, the TDM Block can produce the SEC: in Synchronous Ethernet equipment, it can produce the EEC.

The TDM Block is controlled using direct accesses to the control and status registers (see TDM Block register map).

The TDM Block may be hardwired to the IPCLK input and OPCLK output pins via the TDM Block Multiplexer and the OPCLK Block Multiplexer. Performance of noise-transfer, phase-transient-generation, holdover etc. is well within standardized requirements. See Figure 20 for sample wander and jitter transfer functions.

Interaction of TDM and PTP blocks

Clock generation in a combined PTP/TDM application

The TDM and PTP blocks are independent units that discretely provide appropriate functionality for their basic roles. Indeed, the TDM Block provides full SETS functionality with no assistance from the PTP Block, and the PTP Block provides PTP Grandmaster Clock and Slave Clock functionality without help from the TDM Block. However, by making the blocks work together, the range of applications is expanded and performance can be enhanced.

This section describes how to make the TDM Block and the PTP Block interact to enhance the basic performance of PTP Grandmaster, PTP Slave and SETS functions. The configuration involves the use of the TDM Block Multiplexer, the PTP Block Multiplexer and the OPCLK Block Multiplexer, which interconnect the TDM and PTP blocks. The multiplexers are controlled by dedicated API calls (see the ACS9522 Application Note [32]).

An ACS9522 can support both PTP and traditional TDM applications at the same time, either as a GM clock or as an OC. As a GM, an ACS9522 is capable of simultaneously generating PTP packets as well as output clocks, irrespective of the type of reference signal supplied to it. The output clocks may be referenced to the same reference source as the PTP packets or to some other reference source. For example, the device may generate PTP packets and T0 TDM clocks referenced to one reference source, whilst it also generates a T4 output clock referenced to another reference source. For a definition of the T0 and T4 clock signals, please refer to ITU-T Recommendation G.783[11].

The capability to generate multiple output clocks from separate references also embraces situations when the ACS9522 acts as an OC (where the T0 clock would be referenced to the PTP GM reference), and it allows the device to be used as a comprehensive timing device to suit a multitude of applications.

Figure 3 shows an example of a PTP-recovered clock being added to the possible references from which a SETS function may select a source.

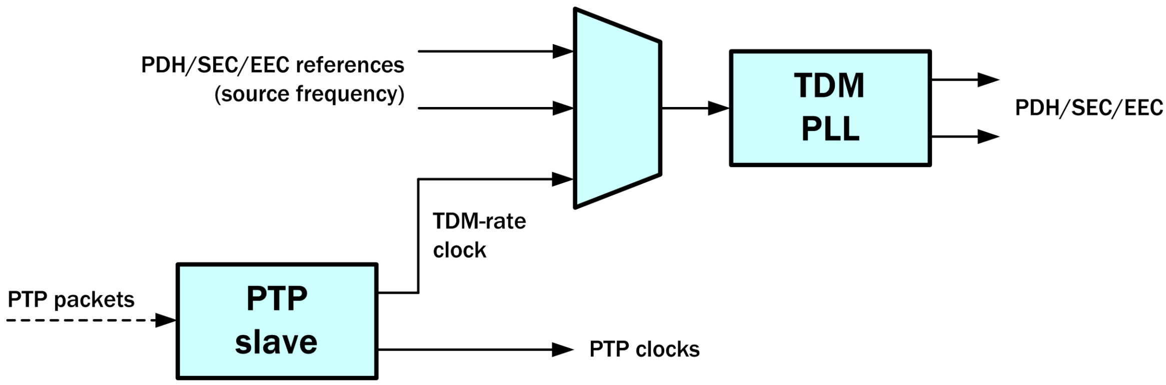

Figure 3 - PTP Block enhancing TDM Block

Enhancement of PTP Grandmaster clock

The PTP Block can accept up to 8 wired clocks. These can come from the first 8 of the 18 possible IPCLK clocks: 4 of the 8 clocks can also be routed from the TDM module. One of the 8 clock inputs can be selected as a reference for the PTP block (see ACS9522 Application Note [32]).

Using the TDM Block to enhance the PTP Block increases the range of clock signal frequencies that can be supported, improves the monitoring, and adds noise-reduction on the selected reference, along with phase build-out on switches between clock references. Conversely, without the use of the TDM Block, the PTP Block requires quieter clocks to achieve the same timebase stability. The PTP Block also has limited activity monitoring and no phase build-out capabilities, so it expects references to be phase-aligned. For 1PPS signals this is a reasonable expectation, but not for line-recovered clocks or even BITS clocks. So using the TDM Block to add the features described above is worthwhile.

The TDM Block can be brought into play by routing the input references to it via the TDM Block Multiplexer and setting up the TDM Block to suit the requirements. The output of the TDM Block can then be routed to the PTP Block, via the PTP Block Multiplexer, to act as a reference frequency source. If more than one reference source is available to the TDM Block, then the TDM Block can be configured to use them in a predefined order. It will apply phase build-out when necessary to maintain a tight output phase. It will apply the noise filter, with the selected bandwidth, and will generate the selected output frequency on the selected output.

This output signal should then be routed into the PTP Block by selecting the appropriate bit of the PTP Block Multiplexer and setting it to route the signal through. An example configuration is shown in Figure 4, although many other configurations are possible.

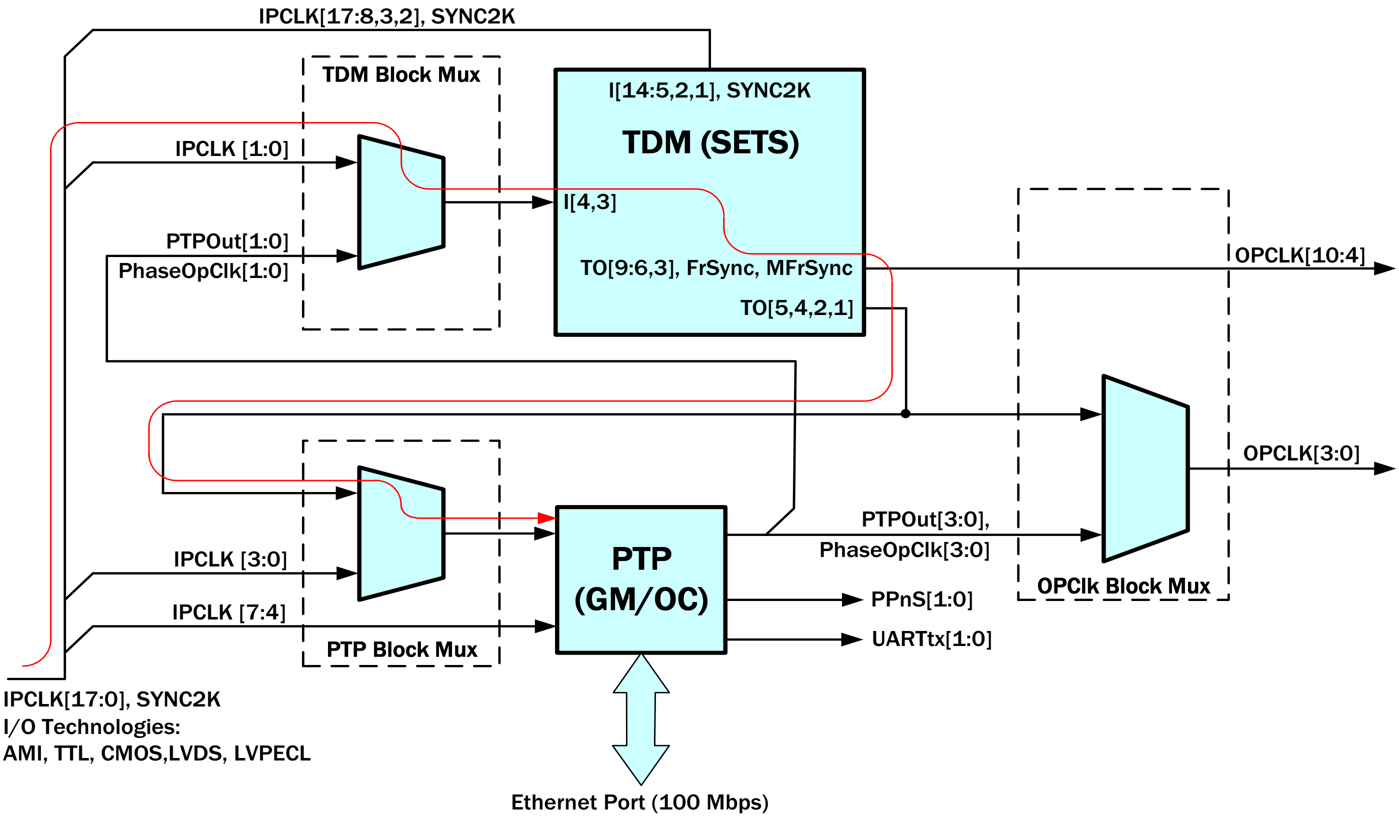

Figure 4 - Example of GM configuration for frequency transfer via PTP

The PTP Block can be supplied with references directly, without going through the TDM Block first. This would be the case when a reference supplies ToD, when the signal fed to the PTP Block would be a 1PPS signal, but other frequencies could be supplied also. These signals must not have significant levels of jitter or wander or they will disturb the stability of the GM timebase.

Enhancement of ordinary clock

All output signals of the PTP Block are driven by digital circuitry. Clock outputs change state on the nearest edge of a high-frequency internal oscillator. These edges rarely occur at exactly the right time for the output clock and so all output clocks which are generated by the PTP Block will contain jitter. For low-frequency output clocks, this jitter will be a small fraction of the unit interval and so should be suitable for direct use without needing additional jitter reduction measures. Higher-frequency signals may not meet the jitter requirements directly and may need additional jitter reduction measures.

When the output clock operates at a frequency used by telecom networks, the TDM Block may be able to perform this jitter reduction since it contains analog phase locked loops designed for low jitter at frequencies up to 155.52 MHz. If required, the TDM Block can be used to so enhance the PTP Block by routing the output signal(s) of the PTP Block to the TDM Block input(s) using the TDM Block Multiplexer (see ACS9522 Application Note [32]).

In addition to reducing jitter, the TDM Block can adapt the frequency of the clock signal if required. The TDM Block also provides a pair of differential outputs (LVPECL or LVDS) which can be used for frequencies up to 155.52 MHz. Figure 5 shows an example configuration.

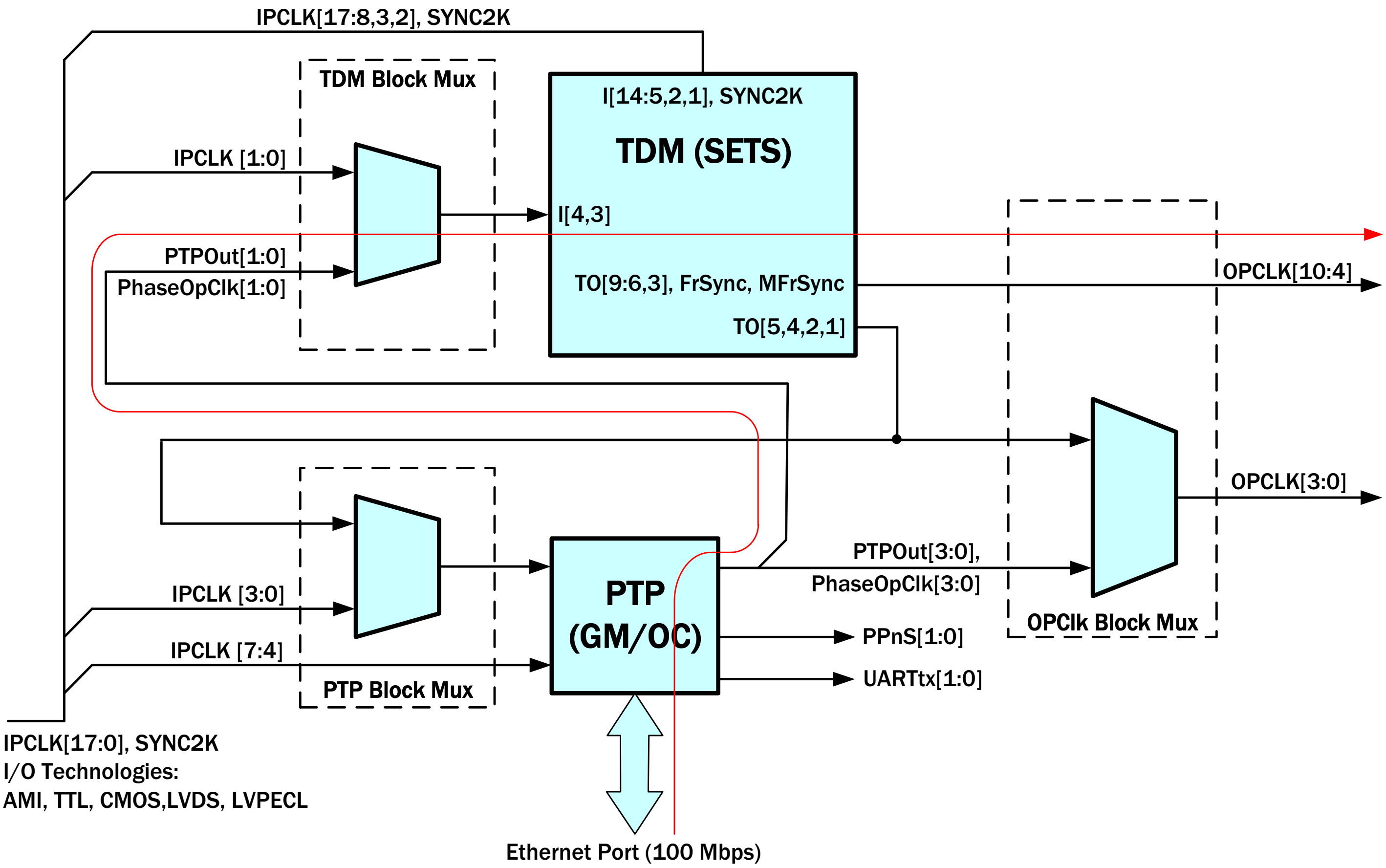

Figure 5 - TDM Block enhancing the PTP Block

Enhancement of the TDM Block

The TDM Block provides SETS functionality for use in traditional TDM applications. But by using the PTP Block as well, the functionality is enhanced by adding a PTP OC. Figure 6 shows an example in which the SETS function of the TDM Block is supplied conventionally with a number of BITS and/or line clocks and, in addition, is supplied with a clock recovered by the PTP Block (acting as an OC). The PTP-recovered clock must be operating at a frequency acceptable to the TDM Block (for example n x 8 kHz).

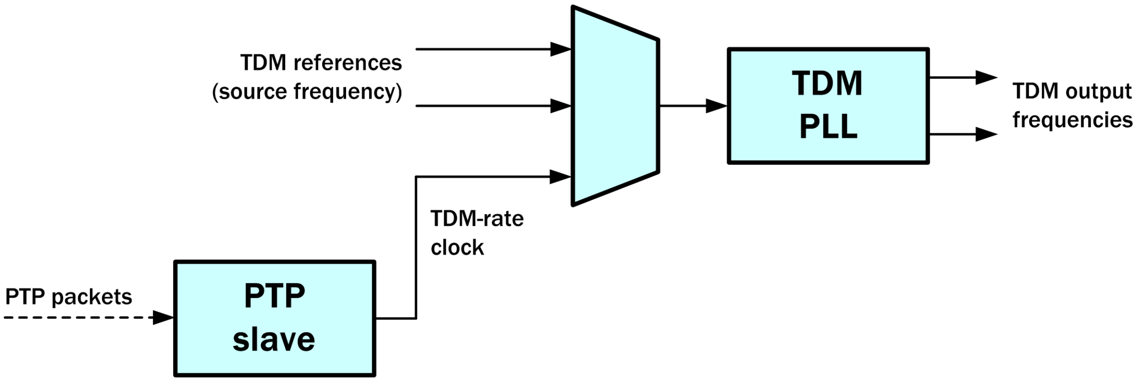

Figure 6 - PTP Block enhancing the TDM Block

All of the clocks supplied to the TDM Block are routed through the TDM Block Multiplexer. The TDM Block can select any of the supplied clocks as the reference source for the T0 channel, in accordance with a priority held in either the SETS T0 priority table or host software. The TDM Block can also select an input for the T4 channel if that is required. The input will be selected according to a priority held in either the SETS T4 priority table or host software.

The final output clock is produced by the TDM Block.

The TDM Block can also perform the new EEC function required by ITU Recommendation G.8262[29] for Synchronous Ethernet applications.

PIN DIAGRAMS

ACS9522

Figure 7 shows the pinout arrangement of the ACS9522. Click on a pad for more detailed information.

Pins of the same colour in Figure 7 may be grouped into buses in the Boundary Scan Description Language (BSDL) file.

	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	VSS	IC 04	NC	NC	NC	IC 03	NC	NC	NC	NC	NC	NC	NC	IC 02	IC 01	VSS	VSS	VSS
B	VSS	VDDIO	VDDIO	VDDIO	VDDIO	VDDIO	VDDIO	NC	NC	NC	NC	NC	VSS	VSS	VSS	VSS	VDDIO	VSS
C	VSS	VSS	VSS	VSS	VSS	VSS	VDDIO	IC 05	REFCLK	NC	NC	NC	VSS	VSS	VSS	VSS	VDDIO	SGMIICLKP
D	VDDIO	VSS	VSS	VSS	VSS	VSS	VDDIO	IPCLK1	IPCLK5s	IPCLK7	IC 06	NC	VSS	VSS	VSS	VSS	VDDIO	SGMIICLKN
E	VDDIO	VSS	VSS	VSS	VSS	VSS	VDDIO	IPCLK0	IPCLK2	IPCLK3	IC 09	OPCLK1	VSS	VSS	VSS	IC 08	IC 07	SGMIICLK
F	VDDIO	VSS	VSS	VSS	VSS	VSS	VDDIO	IPCLK6	IPCLK4	LOCKED	SGMIICLKSEL	PPNS1	VDDIO	VDDIO	IC 11	NC	IC 10	VSS
G	SYNC2K	IPCLK16	IPCLK15	VDDIO	VDDIO	IC 15	VDDIO	SYSMODE0	IC 14	IC 13	SYSMODE1	PWM0	VDDIO	VDDIO	VDDIO	IC 12	VDDASGMIITX1	VSS
H	IPCLK11POS	IPCLK13	IPCLK14	IC 20	IC 19	IC 18	OPCLK7	VDDIO	PORB	ALARM	SLVINT	TRST	VDDIO	VDDIO	IC 17	IC 16	VDDHASGMIITX1	TX1POS
J	IPCLK11NEG	IPCLK12	IPCLK17	IC 22	VDDIO	IC 21	TDI	VSS	VSS	SLVCSB	VDDCORE	OSCFSEL1	VDDCORE	VDDCORE	VDDCORE	VSSSGMII1	VDDHASGMIIRX1	TX1NEG
K	IPCLK8NEG	VDD_SETS	VDD_SETS	VDD_SETS	VDD_SETS	IC 23	SCL	VDDIO	VDDIO	SLVMISO	SDA	VDDIO	VDDIO	VDDIO	VSSSGMII1	VDDSGMII1	VDDASGMIIRX1	RX1POS
L	IPCLK8POS	OPCLK10	VSS	VSS	VSS	VSS	VDD_SETS	VSS	SLVCFGSPI	VDDCORE	VSS	VSS	VSS	VSS	VSS	VSSSGMII0	VDDASGMIIRX0	RX1NEG
M	OPCLK5POS	OPCLK9	VDD_SETS	VSS	VSS	VSS	OSCFSEL0	VSS	SLVCFGCLKE	SLVSCLK	VSS	VSS	VSS	VSS	VSS	VDDSGMII0	VDDHASGMIIRX0	RX0NEG
N	OPCLK5NEG	IPCLK10	VDD_SETS	VSS	VSS	VSS	IC 25	IC 24	VDDIO	VSS	VSS	VSS	VSS	VSS	VSS	VSSSGMII0	VDDHASGMIITX0	RX0POS
P	OPCLK4NEG	IPCLK9	VDD_SETS	VSS	VSS	ESVA3	OPCLK8	PPNS0	VDDIO	IC 26	VDDIO	VDDCORE	VDDIO	VDDCORE	VDDIO	GNDCMU	VDDASGMIITX0	TX0NEG
R	OPCLK4POS	IC 30	VDD_SETS	VSS	VSS	ESGNDA	IC 29	OPCLK0	PWM1	IC 28	IC 27	VDDCORE	MDC	VDDCORE	UARTRX0	VDDIO	UARTTX1	TX0POS
T	OPCLK6POS	IC 37	VSS	VSS	VSS	VSS	IC 36	OPCLK2	DACOUT	IC 35	SLVMOSI	IC 34	IC 33	IC 32	UARTRX1	IC 31	VDDCMUD	VDDCMUD
U	OPCLK6NEG	ESGNDA	TDO	IC 44	ESVA1	VDD_SETS	SONSDHB	OPCLK3	IC 43	DACPOS	IC 42	IC 41	IC 40	IC 39	VDDIO	IC 38	VDDCMU	VDDCMU
V	VSS	ESVA2	TCK	INTREQ	TMS	ESGNDA	IC 51	VDDIO	DACNEG	IC 50	IC 49	IC 48	IC 47	IC 46	MDIO	IC 45	UARTTX0	VSS

JTAG Control/alarms SGMII ToD I2C Input clocks

Output clocks SPI Power Ground Internally connected

Not connected

Figure 7 - ACS9522 pin diagram

Pin descriptions

This section contains tables of descriptions in which the details of every pin of the ACS9522 are declared.

In the pin description tables, the following acronyms appear in the I/O column:

I = input.
O = output.
I/O = bi-directional.

The following acronyms appear in the Signal Type column:

P = power.
G = ground.

TTL^U = TTL input with internal pull-up resistor greater than 20 kΩ.

TTL_D = TTL input with internal pull-down resistor greater than 20 kΩ.

NOTE: All pins are 5 V tolerant except where stated otherwise.

Table 1 JTAG interface

Pin	Symbol	I/O	Signal type	Description
J12	TDI	I	TTL^U	Boundary scan serial test data input Sampled on rising edge of TCK.
V14	TMS	I	TTL^U	Boundary scan test mode select. Sampled on rising edge of TCK. If not used, connect to V_{DD} or leave floating.
V16	TCK	I	TTL_D	Boundary scan test clock input.
U16	TDO	O	TTL^U	Boundary scan serial test data output. Sampled on rising edge of TCK.
H7	TRST	I	TTL_D	Test reset input. 0 = boundary scan standby mode, allowing correct device operation. 1 = enable JTAG boundary scan mode. If not used, connect to GND or leave floating.

Table 2 Control and alarm pins

Pin	Symbol	I/O	Signal type	Description
H10	PORB	I	TTL^{U}	Power-on master reset (active-low). 0 = all internal states reset to default values. 1 = not reset.
F9	LOCKED	O	TTL/CMOS	Device locked status pin: 0 = ACS9522 not in lock. 1 = ACS9522 in lock.
H9	ALARM	O	TTL/CMOS	Use subject to firmware version. If not used, leave to float.
J7	OSCFSEL1	I	TTL_{D}	Oscillator frequency select pins, which set the expected local oscillator frequency.
M12	OSCFSEL0	I	TTL_{D}	
U12	SONSDHB	I	TTL	Selects between SONET and SDH signal rates: 0 = SDH. 1 = SONET.
V15	INTREQ	O	TTL	Interrupt request output.
G7	PWM0	O	TTL	Contact DAPU for application information.
R10	PWM1	O	TTL	
T10	DACOUT	O	Analog	
U9	DACPOS	I	Analog	
V10	DACNEG	I	Analog	

Table 3 SGMII Interface

Pin	Symbol	I/O	Signal type	Description
R1	TX0POS	O	LVDS	SGMII Port 0, TX data output.
P1	TX0NEG			
N1	RX0POS	I	LVDS	SGMII Port 0, RX data input.
M1	RX0NEG			
H1	TX1POS	O	LVDS	SGMII Port 1, TX data output.
J1	TX1NEG			
K1	RX1POS	I	LVDS	SGMII Port 1, RX data input.
L1	RX1NEG			
C1	SGMIICLKP	I	LVDS	125 MHz clock input to the SGMII PLL.
D1	SGMIICLKN			
E1	SGMIICLK	I	TTL/CMOS	SGMII clock input. Maximum frequency 125 MHz + 100 ppm.
F8	SGMIICLKSEL	I	$\text{TTL}^{U}/\text{CMOS}^{U}$	SGMII clock select input. Pull low for differential clock. Leave unconnected for single-ended clock.
R6	MDC	O	TTL	MII clock.
V4	MDIO	I/O	TTL	MII data input/output.

The pins of the SGMII interface are not 5 V tolerant.

NOTE: The SGMII data TX and RX differential pairs have 100 Ω resistors across them. External resistors are unnecessary.

Table 4 Time of day ports

Pin	Symbol	I/O	Signal type	Description
T4	UARTRX1	I	TTL_D	ToD1 receive data.
R4	UARTRX0	I	TTL_D	ToD0 receive data.
R2	UARTTX1	O	TTL	ToD1 transmit data.
V2	UARTTX0	O	TTL	ToD0 transmit data.

Table 5 Configuration pins

Pin	Symbol	I/O	Signal type	Description
G11	SYSMODE0	I	TTL_D	Operating mode selection signal, bit 0.
G8	SYSMODE1	I	TTL_D	Operating mode selection signal, bit 1.

Table 6 Input reference clocks (IPCLK0 to IPCLK17 are not 5 V tolerant and must be pulled low if not used)

Pin	Symbol	I/O	Signal type	Description
E11	IPCLK0	I	TTL	Clock reference input 0, PTP or TDM module. Acceptable frequencies into the PTP module from: 1 PPS/1 Hz to 161MHz (input reference for PTP Master). Acceptable frequencies directly into the TDM module: n × 8 kHz 1.544 MHz (SONET)/2.048 MHz (SDH) 6.48 MHz 19.44 MHz 25.92 MHz 38.88 MHz 51.84 MHz 77.76 MHz. (Pull low if not used).
D11	IPCLK1	I	TTL	Clock reference input 1. PTP or TDM module. Acceptable input frequencies as IPCLK0. (Pull low if not used).
E10	IPCLK2	I	TTL	Clock reference input 2. PTP or TDM module. Acceptable input frequencies as IPCLK0. (Pull low if not used).
E9	IPCLK3	I	TTL	Clock reference input 3. PTP or TDM module. Acceptable input frequencies as IPCLK0. (Pull low if not used).
F10	IPCLK4	I	TTL	Clock reference input 4. PTP module only. Acceptable input frequencies from 1 PPS/1 Hz to 161 MHz. (Pull low if not used).
D10	IPCLK5	I	TTL	Clock reference input 5. PTP module only. Acceptable input frequencies from 1 PPS/1 Hz to 161 MHz. (Pull low if not used).

Table 6 Input reference clocks (IPCLK0 to IPCLK17 are not 5 V tolerant and must be pulled low if not used)

Pin	Symbol	I/O	Signal type	Description
F11	IPCLK6	I	TTL	Clock reference input 6. PTP module only. Acceptable input frequencies from 1 PPS/1 Hz to 161 MHz. (Pull low if not used).
D9	IPCLK7	I	TTL	Clock reference input 7. PTP module only. Acceptable input frequencies from 1 PPS/1 Hz to 161 MHz. (Pull low if not used).
K18	IPCLK8NEG	I	LVPECL/ LVDS	Clock reference input 8. TDM module only. Differential input. Programmable input frequencies to a maximum of 155.52 MHz. Default 19.44 MHz. Default signal type LVDS.
L18	IPCLK8POS			
P17	IPCLK9	I	AMI	Clock reference input 9. AMI, composite clock 64 kHz + 8 kHz (input reference for TDM Timing mode only). Default 64/8 kHz composite clock.
N17	IPCLK10	I	AMI	Clock reference input 10. AMI, composite clock 64 kHz + 8 kHz (input reference for TDM Timing mode only). Default 64/8 kHz composite clock.
J18	IPCLK11NEG	I	LVPECL/ LVDS	Clock reference input 11. TDM module only. Differential input. Programmable input frequencies to a maximum of 155.52 MHz. Default 19.44 MHz. Default signal type LVPECL.
H18	IPCLK11POS			
J17	IPCLK12	I	TTL_D	Clock reference input 12. TDM module only. Acceptable frequencies directly into the TDM module: n × 8 kHz 1.544 MHz (SONET)/2.048 MHz (SDH) 6.48 MHz 19.44 MHz 25.92 MHz 38.88 MHz 51.84 MHz 77.76 MHz. (Pull low if not used).
H17	IPCLK13	I	TTL_D	Clock reference input 13. TDM module only. Acceptable input frequencies as IPCLK12. (Pull low if not used).
H16	IPCLK14	I	TTL_D	Clock reference input 14. TDM module only. Acceptable input frequencies as IPCLK12. (Pull low if not used).
G16	IPCLK15	I	TTL_D	Clock reference input 15. TDM module only. Acceptable input frequencies as IPCLK12. (Pull low if not used).
G17	IPCLK16	I	TTL_D	Clock reference input 16. TDM module only. Acceptable input frequencies as IPCLK12. (Pull low if not used).
G18	SYNC2K	I	TTL_D	Partner phase/frequency monitor.
J16	IPCLK17	I	TTL_D	Clock reference input 17. TDM module only. Acceptable input frequencies as IPCLK12. (Pull low if not used).

Table 7 Output reference clocks

Pin	Symbol	I/O	Signal type	Description
R11	OPCLK0	O	TTL/CMOS	For PTP mode operation, refer to Frequency and time generator. For operation in TDM timing mode, refer to Table 43.
E7	OPCLK1	O	TTL/CMOS	Clock reference output 1. Same clock frequency configuration options as OPCLK0.
T11	OPCLK2	O	TTL/CMOS	Clock reference output 2. Same clock frequency configuration options as OPCLK0.
U11	OPCLK3	O	TTL/CMOS	Clock reference output 3. Same clock frequency configuration options as OPCLK0.
P18	OPCLK4NEG	O	LVDS/ LVPECL	Clock reference output 4. Default frequency 77.76 MHz. Default signal type LVDS.
R18	OPCLK4POS			
N18	OPCLK5NEG	O	LVDS/ LVPECL	Clock reference output 5. Default frequency 155.52 MHz. Default signal type LVPECL.
M18	OPCLK5POS			
U18	OPCLK6NEG	O	AMI	Clock reference output 6. TDM module only. 64/8 kHz (composite clock, 64 kHz + 8 kHz). Fixed frequency.
T18	OPCLK6POS			
H12	OPCLK7	O	TTL/CMOS	Clock reference output 7. TDM module only. Same clock frequency configuration options as OPCLK0. For operation in TDM Timing mode.
P12	OPCLK8	O	TTL/CMOS	Clock reference output 8. TDM module only. Same clock frequency configuration options as OPCLK7.
M17	OPCLK9	O	TTL/CMOS	Clock reference output 9. TDM module only. Same clock frequency configuration options as OPCLK7.
L17	OPCLK10	O	TTL/CMOS	Clock reference output 10. TDM module only. Same clock frequency configuration options as OPCLK7.

Table 8 PPnS

Pin	Symbol	I/O	Signal type	Description
P11	PPNS0	O	TTL/CMOS	Pulses per n second reference output. Default 1 pps. Fully programmable high time: default 100 ms. [1] Rising edge specifies seconds rollover.
F7	PPNS1	O	TTL/CMOS	Pulses per n second reference output. Default 1 pps. Fully programmable high time: default 100 ms. [1] Rising edge specifies seconds rollover.

1. May vary with software revision.

Table 9 Serial interfaces

Pin	Symbol	I/O	Signal type	Description
Slave SPI				
K9	SLVMISO	O	TTL/CMOS	Master in/slave out data output.
T8	SLVMOSI	I	TTL_D	Master out/slave in data input.
M9	SLVSCLK	I	TTL_D	Slave mode serial clock.
J9	SLVCSB	I	TTL^U	Chip select (slave): 0 = slave serial interface enabled. 1 = slave serial interface disabled. Asserted by the microprocessor.
H8	SLVINT	O	TTL/CMOS	Slave interrupt output: 0 = no interrupt. 1 = interrupt.
M10	SLVCFGCLKE	I	TTL_D	Clock control for slave serial interface: 0 = sampling of SLVMOSI occurs on the rising edge and clocking out of SLVMISO occurs on the falling edge of SLVSCLK. 1 = sampling of SLVMOSI occurs on the falling edge and clocking out of SLVMISO occurs on the rising edge of SLVSCLK.
L10	SLVCFGSPI	I	TTL_D	For future use. Must be fitted with a 10 kΩ pull-down resistor.
I^2C				
K12	SCL	O	CMOS open drain	I2C SCL for the interface to ACS1790.
K8	SDA	I/O	CMOS open drain	I2C SDA for the interface to ACS1790.

Table 10 System clocks

Pin	Symbol	I/O	Signal type	Description
Local oscillator				
C10	REFCLK	I	TTL	Input for local oscillator in normal operating mode. Expected input frequency set by OSC_SEL[1:0].

If REFCLK is not supplied by a good quality oscillator, the ACS9522 may still appear to work but performance may be seriously compromised.

Table 11 Power supply pins

Pin	Symbol	Description	Pin	Symbol	Description
L2	VDDASGMIIRX0	1.2 V SGMII RX analogue supply.	C2	VDDIO	3.3 V I/O supply
P2	VDDASGMIITX0	1.2 V SGMII TX analogue supply.	C12		
M2	VDDHASGMIIRX0	3.3 V SGMII RX analogue supply.	D2		
N2	VDDHASGMIITX0	3.3 V SGMII TX analogue supply.	D12		
M3	VDDSGMII0	1.2 V SGMII digital supply.	D18		
K2	VDDASGMIIRX1	1.2 V SGMII RX analogue supply.	E12		
G2	VDDASGMIITX1	1.2 V SGMII TX analogue supply.	E18		
J2	VDDHASGMIIRX1	3.3 V SGMII RX analogue supply.	F5		
H2	VDDHASGMIITX1	3.3 V SGMII TX analogue supply.	F6		
K3	VDDSGMII1	1.2 V SGMII digital supply.	F12		
J4	VDDCORE	1.2 V digital supply.	F18		
J5			G4		
J6			G5		
J8			G6		
L9			G12		
P5			G14		
P7			G15		
R5			H5		
R7			H6		
T1	VDDCMUD	1.2 V digital supply for CMU	H11		
T2			J14		
U1	VDDCMU	3.3 V analogue supply for CMU	K5		
U2			K6		
U14	ESVA1	3.3 V analogue PLL supply	K7		
V17	ESVA2		K10		
P13	ESVA3		K11		
B2	VDDIO	3.3 V I/O supply	N10		
B12			P4		
B13			P6		
B14			P8		
B15			P10		
B16			R3		
B17			U4		

Table 11 Power supply pins

Pin	Symbol	Description
V11	VDDIO	3.3 V I/O supply
K14	VDD_SETS	3.3 V supply for SETS
K15		
K16		
K17		
L12		

Pin	Symbol	Description
M16	VDD_SETS	3.3 V supply for SETS
N16		
P16		
R16		
U13		

Table 12 Ground pins

Pin	Symbol	Description
P3	GNDCMU	Digital PLL ground.
R13	ESGNDA	Analogue PLL ground.
V13		
U17		
A1	VSS	
A2		
A3		
A18		
B1		
B3		
B4		
B5		
B6		
B18		
C3		
C4		
C5		
C6		
C13		
C14		
C15		
C16		
C17		
C18		
D3		
D4		
D5		
D6		
D13		
D14		
D15		
D16		
D17		
E4		

Pin	Symbol	Description
E5	VSS	
E6		
E13		
E14		
E15		
E16		
E17		
F1		
F13		
F14		
F15		
F16		
F17		
G1		
J10		
J11		
L4		
L5		
L6		
L7		
L8		
L11		
L13		
L14		
L15		
L16		
M4		
M5		
M6		
M7		
M8		
M11		
M13		
M14		

Table 12 Ground pins

Pin	Symbol	Description	Pin	Symbol	Description
M15	VSS		R14	VSS	
N4			R15		
N5			T13		
N6			T14		
N7			T15		
N8			T16		
N9			V1		
N13			V18		
N14			L3	VSSSGMII0	
N15			N3		
P14			J3	VSSSGMII1	
P15			K4		

Table 13 Internally connected pins

Pin	Symbol	Description
A4	IC 01	Leave to float.
A5	IC 02	
A13	IC 03	
A17	IC 04	
C11	IC 05	
D8	IC 06	
E2	IC 07	
E3	IC 08	
E8	IC 09	
F2	IC 10	
F4	IC 11	
G3	IC 12	
G9	IC 13	
G10	IC 14	
G13	IC 15	
H3	IC 16	
H4	IC 17	
H13	IC 18	
H14	IC 19	
H15	IC 20	
J13	IC 21	
J15	IC 22	
K13	IC 23	
N11	IC 24	
N12	IC 25	
P9 [1]	IC 26	

Pin	Symbol	Description
R8 [1]	IC 27	Leave to float.
R9	IC 28	
R12	IC 29	
R17	IC 30	
T3 [1]	IC 31	
T5 [1]	IC 32	
T6 [1]	IC 33	
T7 [1]	IC 34	
T9	IC 35	
T12	IC 36	
T17	IC 37	
U3 [1]	IC 38	
U5 [1]	IC 39	
U6[1]	IC 40	
U7 [1]	IC 41	
U8 [1]	IC 42	
U10	IC 43	
U15	IC 44	
V3 [1]	IC 45	
V5	IC 46	
V6 [1]	IC 47	
V7 [1]	IC 48	
V8 [1]	IC 49	
V9	IC 50	
V12	IC 51	

1.

Table 14 Not connected pins

Pin	Symbol	Description
A6	NC	Leave to float
A7		
A8		
A9		
A10		
A11		
A12		
A14		
A15		
A16		

Pin	Symbol	Description
B7	NC	Leave to float
B8		
B9		
B10		
B11		
C7		
C8		
C9		
D7		
F3		

Interfaces

This section describes the various interfaces provided on the ACS9522.

Input reference clocks

There are 18 clock reference inputs denoted IPCLK[17:0], using these variety of I/O technologies:

- AMI (for Alternate Mark Inversion signals)
- LVPECL/LVDS
- LVTTL

AMI input and output ports

Input clocks IPCLK9 and IPCLK10 are for AMI composite 64 kHz/8 kHz clocks. The composite clock timing signals convey the 64 kHz bit-timing information using AMI coding with a 50% to 70% duty ratio and the 8 kHz octet phase information by introducing violations in the code rule. The structure of the signals and the voltage levels are shown in Figure 8 and Figure 9.

The AMI signal is DC balanced, and consists of positive and negative pulses with a peak-to-peak voltage of 2.0 ±0.2 V.

The electrical specifications are obtained from the digital 64 kbit/s centralized clock interface.

The 400 Hz component is not supported.

The electrical characteristics of the 64 kbit/s interface are as follows:

- Nominal bit rate: 64 kbit/s. The tolerance is determined by the network clock stability.
- There should be a symmetrical pair carrying the composite timing signal (64 kHz and 8 kHz). The use of transformers is recommended.
- For the over-voltage protection requirement, refer to ITU Recommendation K.41[21].

Table 15 DC characteristics of the AMI input and output ports

Across all operating conditions, unless otherwise stated.

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input pulse width.	t_{PW}	1.56	7.8	14.04	µs
Input pulse rise/fall time.	$t_{R/F}$	-	-	5	µs
AMI input voltage high.	$V_{IH\ AMI}$	2.5	-	V_{DD} + 0.3	V
AMI input voltage middle.	$V_{VIM\ AMI}$	1.5	1.65	1.8	V
AMI input voltage low.	$V_{VIL\ AMI}$	0	-	1.4	V
AMI output current drive.	I_{AMIOUT}	-	-	20	mA
AMI output high voltage. Output current = 20mA.	$V_{OH\ AMI}$	V_{DD} - 0.16	-	-	V
AMI output low voltage. Output current = 20mA.	$V_{OL\ AMI}$	-	-	0.16	V
Output pulse width	tPW_out	-	7.8	-	µs
Nominal test load impedance.	R_{TEST}	-	110	-	Ω
“Mark” amplitude after transformer.	V_{MARK}	0.9	1.0	1.1	V
“Space” amplitude after transformer.	V_{SPACE}	- 0.1	0	0.1	V

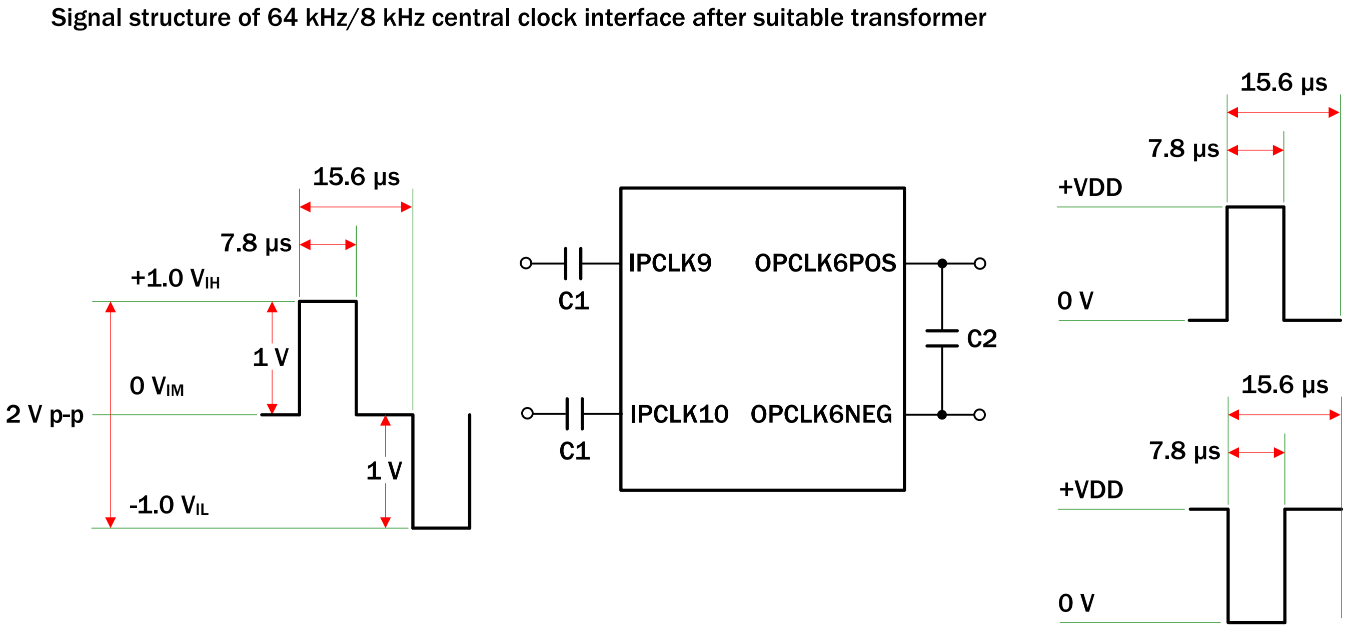

Figure 8 - AMI input and output signal level

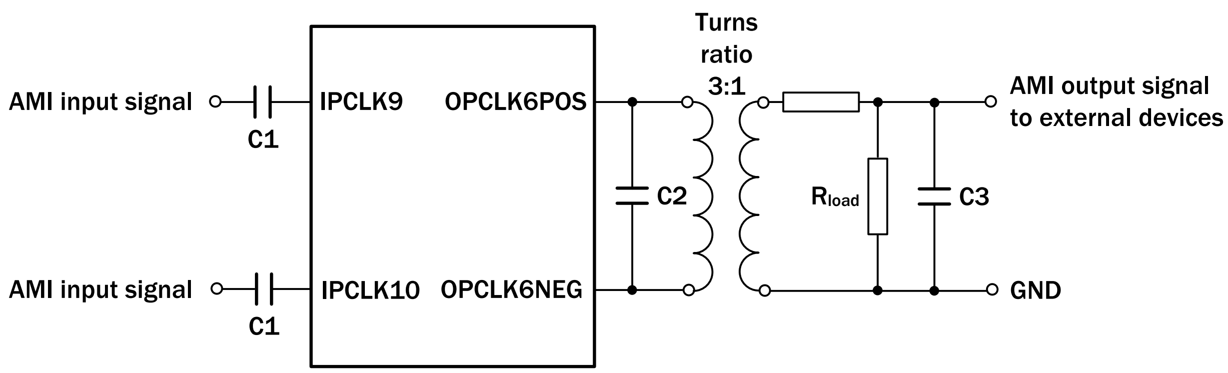

Figure 9 - Recommended line termination for the AMI input and output ports

NOTE: AMI input channels IPCLK9 and IPCLK10 should be connected to the external AMI clock source by 470 nF coupling capacitor C1.

The AMI differential output OPCLK6 should be coupled to a line transformer with a turns ratio of 3:1. Components C2 = 470 pF and C3 = 2 nF. If a transformer with a turns ratio of 1:1 is used, a 3:1 ratio potential divider R_{load} must be used to achieve the required 1 V p-p voltage level for the positive and negative pulses.

LVPECL input and output ports

Table 16 DC characteristics of the LVPECL input and output ports

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
LVPECL input low voltage. Differential inputs [1,2].	V_{ILPECL}	V_{DD}-2.5	-	V_{DD}-0.5	V
LVPECL input high voltage. Differential inputs [1,2].	V_{IHPECL}	V_{DD}-2.4	-	V_{DD}-0.4	V
Input differential voltage.	V_{IDPECL}	0.1	-	1.4	V
LVPECL input low voltage. Single-ended input [3].	V_{ILPECL_S}	V_{DD}-2.4	-	V_{DD}-1.5	V
LVPECL input high voltage. Single-ended input [3].	V_{ILPECL_S}	V_{DD}-1.3	-	V_{DD}-0.5	V
Input high current. Input differential voltage V_{ID} = 1.4V.	I_{IHPECL}	-10	-	+10	µA
Input low current. Input differential voltage V_{ID} = 1.4V.	I_{ILPECL}	-10	-	+10	µA
LVPECL output low voltage [4].	V_{OLPECL}	V_{DD}-2.10	-	V_{DD}-1.62	V
LVPECL output high voltage [4].	V_{OHPECL}	V_{DD}-1.40	-	V_{DD}-1.00	V
LVPECL output differential voltage [4].	V_{ODPECL}	550	-	900	mV

1. Unused differential input ports should either be left floating and set to LVDS mode, or the positive and negative inputs should be tied to V_{DD} and GND respectively.
2. Assuming a differential input voltage of at least 100 mV.
3. Unused single-ended input should be terminated to V_{DD} - 1.4 V.
4. With 50 Ω load on each pin to V_{DD} - 2 V. i.e. 82 Ω to GND and 130 Ω to VDD.

Input clock IPCLK8 and IPCLK11 are differential inputs that can accept the same frequencies as the LVTTL ports and also 2 kHz, 4 kHz and 155.52 MHz.

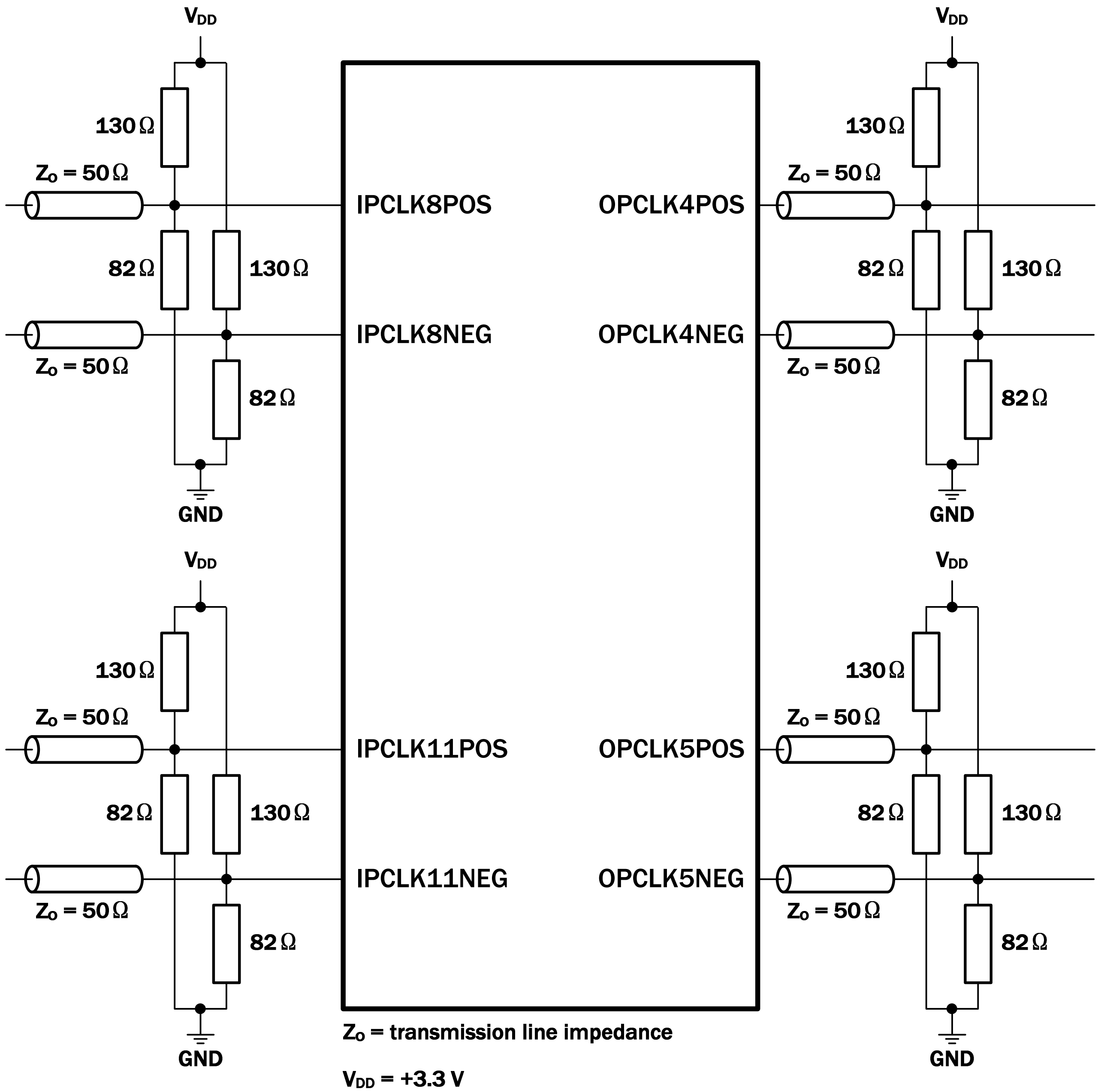

Figure 10 - Recommended line termination for the LVPECL input and output ports

LVDS input and output ports

Table 17 DC characteristics of the LVDS input and output ports

Across all operating conditions, unless otherwise stated.

Parameter	Symbol	Minimum	Typical	Maximum	Units
LVDS input voltage range. Differential input voltage = 100 mV.	V_{VRLVDS}	0	-	2.40	V
LVDS differential input threshold.	V_{DITH}	-100	-	+100	mV
LVDS input differential voltage.	$V_{IDLVTSDS}$	0.1	-	1.4	V
LVDS input termination resistance.	R_{TERM}	95	100	105	Ω
LVDS output high voltage. [1]	V_{OHLVDS}	-	-	1.585	V
LVDS output low voltage.	V_{OLLVDS}	0.885	-	-	V
LVDS differential output voltage.	V_{ODLVDS}	250	-	450	mV
LVDS change in magnitude of differential output voltage for complementary states. [2]	$V_{DOSLVDS}$	-	-	25	mV
LVDS output offset voltage. Temperature = 25°C.	V_{OSLVDS}	1.125	-	1.375	V

1. With 100 Ω load across differential terminals.

Note that Table 17 is only applicable to IPCLK8P/N, IPCLK11P/N, OPCLK4P/N and OPCLK5P/N when configured in LVDS mode.

Time of day port

A ToD port is used in PTP Timing modes only. In PTP GM mode, the port is an input comprising UARTRX and a 1 PPS signal. In PTP Slave mode, the port is an output comprising UARTTX and a PPnS signal, which gives a pulse every n seconds (t_W configurable for a minimum of 100 ns to a maximum of 400 ms). The UART has an integrated baud rate generator using 1 stop bit and no parity. The maximum baud rate of the UART port is 19200 baud.

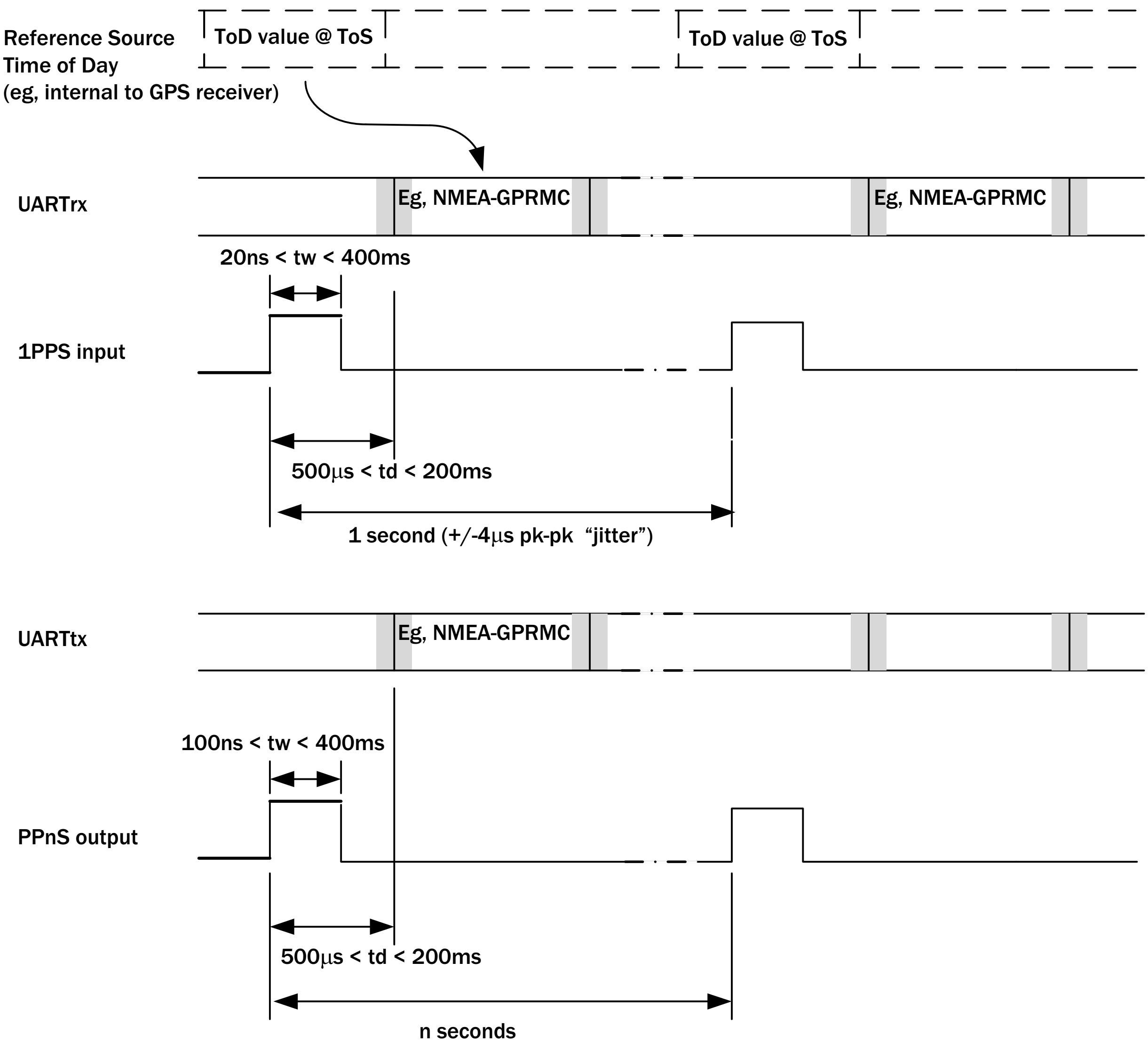

Figure 11 - ToD port timing

Jitter tolerance of the 1PPS input

The ACS9522 will reject a 1PPS signal if the jitter is greater than 4 µs peak-to-peak. However, it is strongly recommended that jitter on this signal is avoided as much as possible because the distribution of jitter on this signal is not known and so cannot be correctly attenuated by filtering. Any filtering applied to this signal will introduce a phase offset error. This treatment differs from that of more traditional reference sources because the phase of a 1PPS signal, relative to a recognised source of time such as UTC, is the parameter of most significance. For other references, the rate (frequency) is the more significant parameter.

Time of day message format

The ToD message format can be a GPRMC message or one of a group of other GPS messages or proprietary messages to suit specific causes. Refer to the DPSync Resource Center[1] for more details.

GPRMC message format

A GPRMC message has the format $GPRMC,122356,A,0000.0000,N,00000.0000,W,0.0.0.0,120508,,,A*F6 in which the commas are separators. The architecture of the message is shown in Table 18. The message is 62 characters in length (i.e. 62 bytes). No parity bit is used, but each byte has a stop bit.

Table 18 Architecture of GPRMC message

Element	Description
$GPRMC	Message header.
122356	UTC value.
A	Status (A = active, V = void).
0000.0000,N	Latitude, north (fixed to zero).
00000.0000,W	Longitude, west (fixed to zero).
0.0	Speed over ground (fixed to zero).
0.0	Track angle (fixed to zero).
120508	Date (ddmmyy).
A	A = autonomous, D = differential, E = estimated, S = simulation, N = not valid.
*F6	Checksum.

Phase aligned output clock port

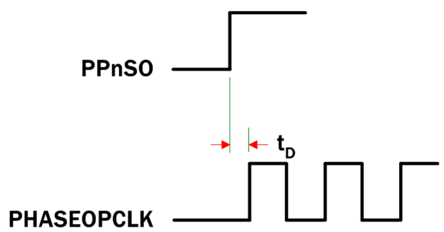

Figure 12 - Phase aligned clock timing

Table 19 Phase aligned clock timing data

Symbol	Parameter	Minimum	Typical	Maximum
t_D	Delay from rising edge of PPnSO to rising edge of PHASEOPCLK.	2 ns	6 ns	12 ns

Serial peripheral interface

The serial peripheral interface (SPI) is a slave port for communication with a serial microprocessor bus, allowing the ACS9522 to be controlled by an external processor. The serial interface header must be connected to the host processor, which acts as the master. The ACS9522 requires data to be transmitted LSB first, MSB first is not supported.

Figure 13 and Table 20 show the read access timing for the serial interface. Figure 13 shows two clock configurations. When SLVCFGCLKE = 1 (CPOL =1), the data is sampled on the falling edge and driven on the rising edge. When SKLVCFGCLKE = 0 (CPOL=0), the data is sampled on the rising edge and driven on the falling edge

Figure 14 and Table 21 show the write access timing for the serial interface. Figure 14 shows two clock configurations. When SLVCFGCLKE = 1 (CPOL =1), the data is sampled on the falling edge and driven on the rising edge. When SKLVCFGCLKE = 0 (CPOL=0), the data is sampled on the rising edge and driven on the falling edge.

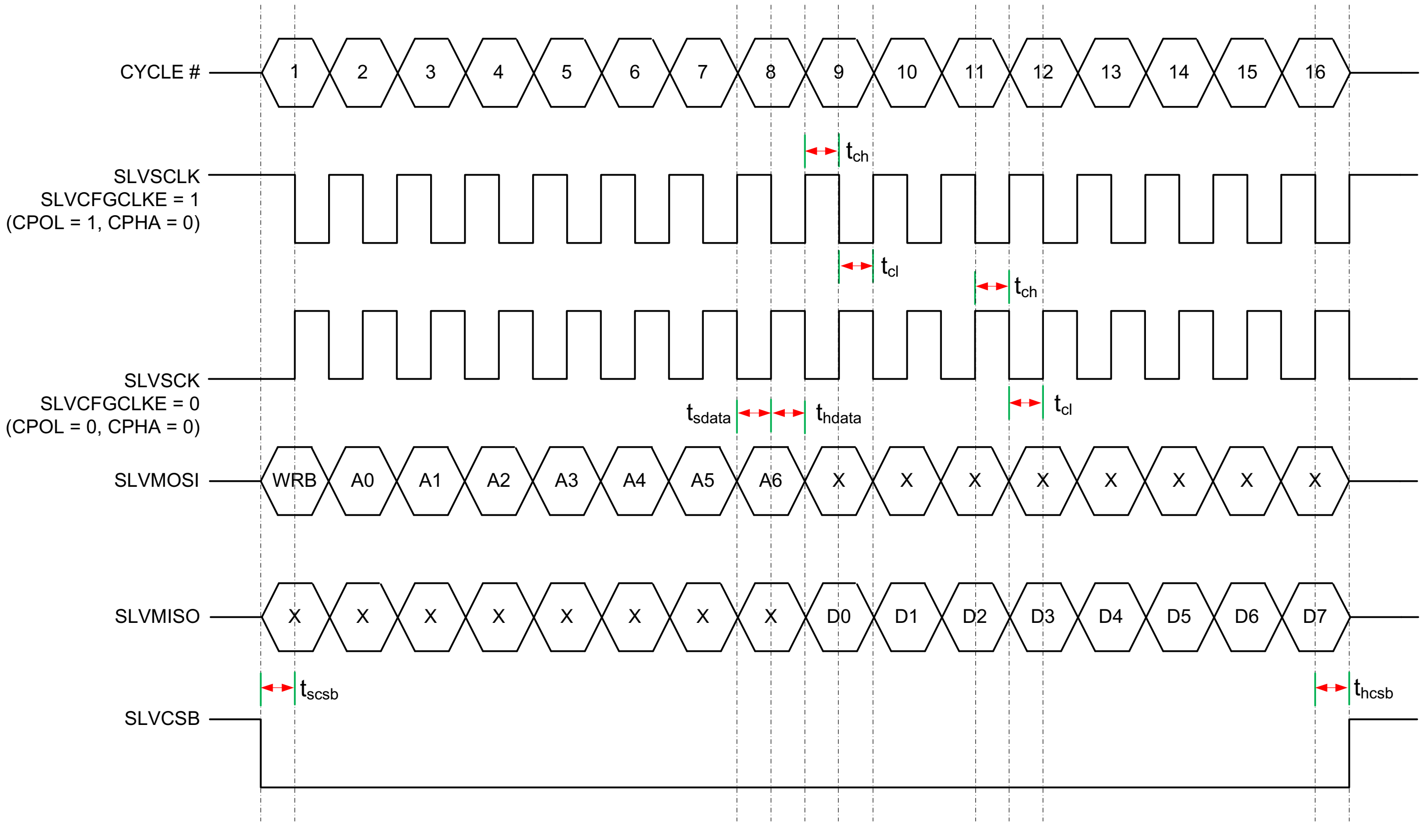

Figure 13 - Read access timing of the serial interface

Table 20 Serial interface read access timing data

Symbol	Parameter	Minimum	Typical	Maximum	Unit
F_{sck}	SPI clock frequency	-	-	10	MHz
t_{sdata}	Setup MOSI valid to $SCK_{rising\ edge}$	4	-	-	ns
t_{scsb}	Setup $CSB_{falling\ edge}$ to $SCK_{rising\ edge}$	14	-	-	ns
t_{d1}	Delay $SCK_{falling\ edge}$ to MISO valid	-	-	45	ns
t_{d2}	Delay $CSB_{rising\ edge}$ MISO high-Z	-	45	-	ns
t_{cl}	SCK Low time	45	-	-	ns
t_{ch}	SCK High time	45	-	-	ns
t_{hdata}	Hold MOSI valid after $SCK_{rising\ edge}$	6	-	-	ns
t_{hcsb}	Hold CSB low after $SCK_{rising\ edge}$	6	-	-	ns
t_p	Time between accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	45	-	-	ns

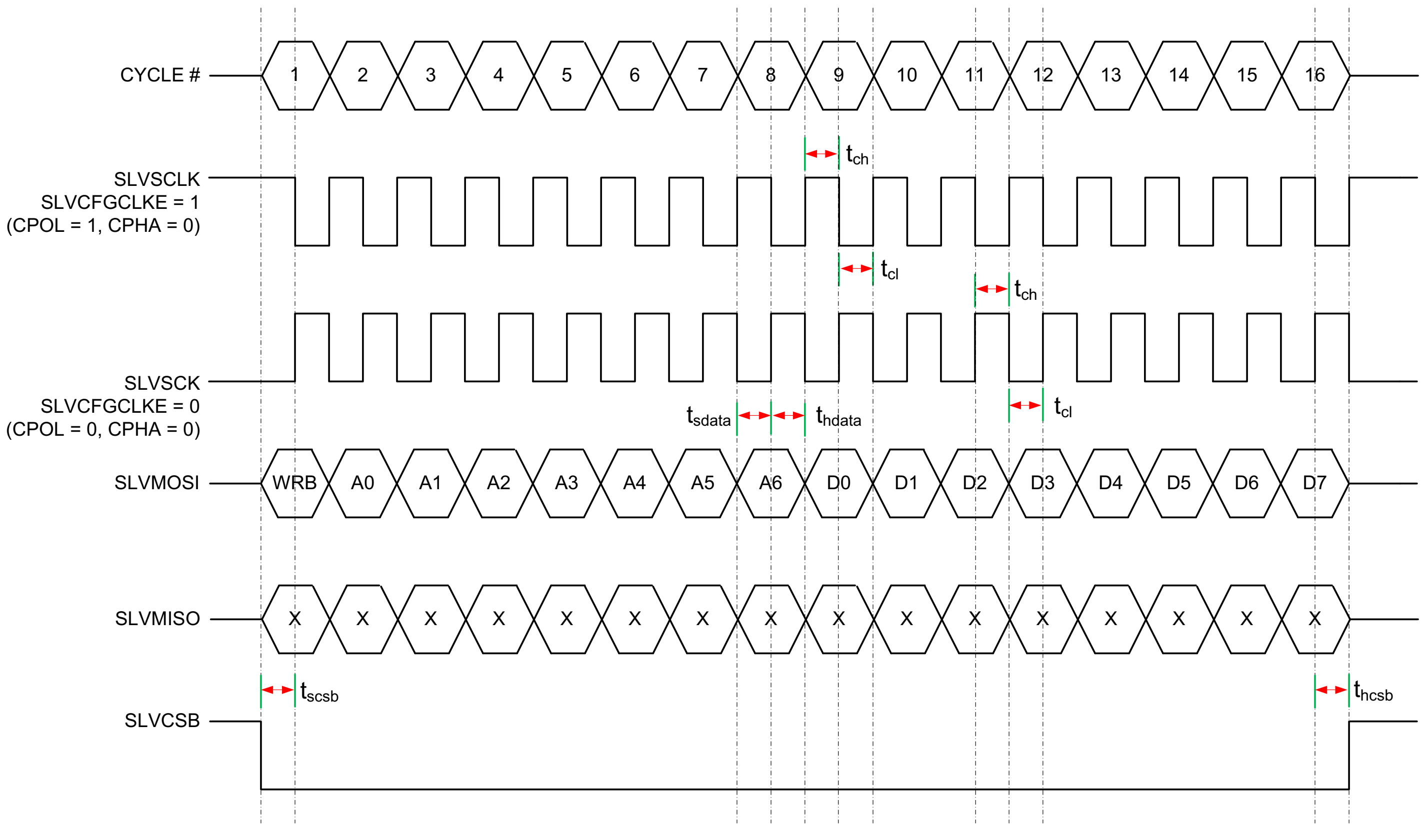

Figure 14 - Write access timing of the serial interface

Table 21 Serial interface write access timing data

Symbol	Parameter	Minimum	Typical	Maximum	Unit
F_{sck}	SPI clock frequency	-	-	10	MHz
t_{sdata}	Setup MOSI valid to $SCK_{rising\ edge}$	4	-	-	ns
t_{scsb}	Setup $CSB_{falling\ edge}$ to $SCK_{rising\ edge}$	14	-	-	ns
t_{d1}	Delay $SCK_{falling\ edge}$ to MISO valid	-	-	45	ns
t_{d2}	Delay $CSB_{rising\ edge}$ MISO high-Z	-	45	-	ns
t_{cl}	SCK Low time	45	-	-	ns
t_{ch}	SCK High time	45	-	-	ns
t_{hdata}	Hold MOSI valid after $SCK_{rising\ edge}$	6	-	-	ns
t_{hcsb}	Hold CSB low after $SCK_{rising\ edge}$	6	-	-	ns
t_p	Time between accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	45	-	-	ns

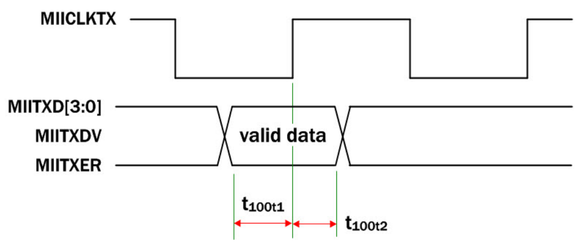

Table 22 100M MII receive timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{100r1}	Rx signal setup time to MACnCLKRX rising edge.	10	-	-	ns
t_{100r2}	Rx signal setup time from MACnCLKRX rising edge.	10	-	-	ns
	MACnCLKRX frequency.	-	25	-	MHz

Figure 15 - MII transmit timing

Table 23 100M MII transmit timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{100t1}	Tx signal setup time to MACnCLKTX rising edge.	20	-	-	ns
t_{100t2}	Tx signal setup time from MACnCLKTX r ising edge.	3	-	-	ns
	MACnCLKTX frequency.	-	25	-	MHz

SGMII interfaces

The ACS9522 has two serial SGMII interfaces running with a 100 Mbps data rate and a 1.25 Gbps line rate. The interfaces are IEEE 802.3[7] compliant for communication via a suitable packet PHY. SGMII functional, timing, electrical and mechanical requirements are supported as defined in IEEE 802.3[7] part 3, section two, sub-section 22 and annexes 22A, 22B and 22C. (See also[12] clauses 36 and 37). The timing arrangements of both interfaces are identical. See [30] for more information. Note that this interface may be clocked via differential or single-ended SGMIICLK input ports.

Table 24 SGMII clock timing characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
FIN	SGMIICLK frequency	-	125	-	MHz
FT	SGMIICLK frequency tolerance	-100	-	+100	ppm
DuCy	SGMIICLK duty cycle	40	-	60	%
T_{JTRIN}	SGMIICLK peak-to-peak input jitter	-	-	40	picosec
T_{RCR}, T_{RCF}	SGMIICLK rise and fall time (20% to 80%)	-	-	1	nanosec

Table 25 SGMII output data AC characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
DR[1]	Serial data rate	-	1,25	-	Gbits/sec
t_{FALL}	Vod fall time (80% to 20%)	100	-	200	picosec
t_{RISE}	Vod rise time (20% to 80%)	100	-	200	picosec
t_{skew}[2]	Skew between two members of a differential pair: [tp_{HLP} - tp_{LHN}] or [tp_{LHP} - tp_{HLN}]	-	-	±20	picosec

1. Packets will be delivered by DPSync at the data rate DR, but DPSync can only support a sustained data rate of 100 Mbit/s (as per Fast Ethernet).
2. SGMIIRX differential input pairs have an internal 100 Ω resistor between the input pins. No external resistor is needed. Damage to the internal resistor may occur if the differential voltage, Vidth, exceeds the maximum allowed value of 400 mV.

Table 26 SGMII output data DC characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Voh	Output voltage high state	-	-	1525	mV
Vol	Output voltage low state	875	-	-	mV
Vod	Output differential voltage	150	-	400	mV

Table 27 SGMII input data AC characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
DRT[1]	Serial input data rate tolerance	-300	-	+300	ppm

1. Packets may be delivered to DPSync at the data rate DR, but DPSync can only support a sustained data rate of 100 Mbit/s (as per Fast Ethernet).

Table 28 SGMII input data DC characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Vi	Input voltage range	675	-	1725	mV
Vidth	Input differential threshold	-50	-	50	mV
Vid[1]	Input differential voltage	-	-	650	mV
Rin	Differential input impedance	80	-	120	Ω

1. SGMIIRX differential input pairs have an internal 100 Ω resistors between the input pins. No external resistor is needed. Damage to the internal resistor may occur if the differential voltage, Vid, exceeds the maximum allowed value of 650 mV.

I²C interface

The characteristics of this interface are defined in the Philips-NXP I²C specification[31].

JTAG port

The JTAG port is provided to allow a full boundary scan to be made.

JTAG implementation is fully compliant with IEEE 1149.1[6], with the following minor exceptions:

1) The output boundary scan cells do not capture data from the core, and do not therefore support INTEST. However this does not affect board testing.
2) The polarity of TRST complies with the standard:

   0 = normal operation.

   1 = enable JTAG boundary scan mode.

Refer to the standard for more information.

Figure 16 and Table 29 show the JTAG boundary scan timing.

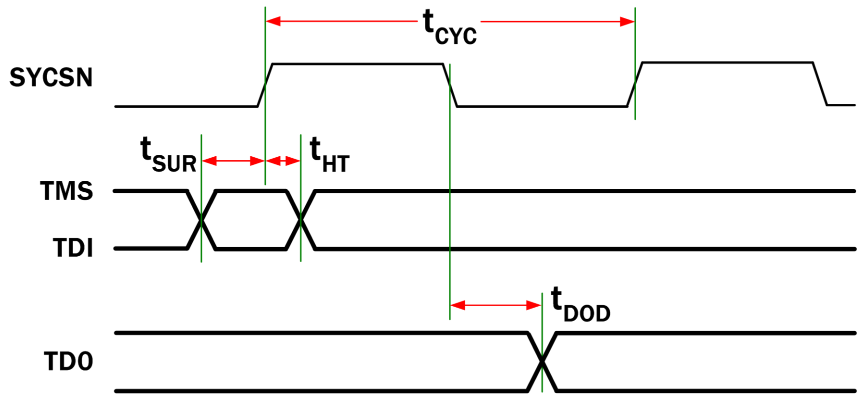

Figure 16 - JTAG boundary scan timing diagram

Table 29 JTAG timing data (for use with Figure 16)

Symbol	Parameter	Minimum	Maximum	Units
t_{CYC}	Cycle time.	50	-	ns
t_{SUR}	TMS/TDI to TCK rising edge time.	3	-	ns
t_{HT}	TCK rising to TMS/TDI hold time.	30	-	ns
t_{DOD}	TCK falling to TDO valid.	-	5	ns

Table 30 DC characteristics of the JTAG ports

Parameter	Symbol	Minimum	Nominal	Maximum	Units
V_{IN} High	V_{IH}	2	-	-	V
V_{IN} Low	V_{IL}	-	-	0.8	V

Operating mode selection port

Mode select pins SYSMODE1 and SYSMODE0 set the operating mode of the ACS9522 as shown in Table 31. Mode selection changes on reset only.

Table 31 Operating mode selection truth table

SYSMODE1	SYSMODE0	Operating mode
0	0	Combined PTP and Physical Layer Timing.
0	1	SGMII / Ethernet self test physical port 0
1	0	SGMII / Ethernet self test physical port 1
1	1	Restore default factory programmed device settings

Local oscillator clock

The master system clock on the ACS9522 should be provided by an external clock signal selected according to Table 34. The clock specification is important for meeting the ITU/ETSI and Telcordia performance requirements for holdover mode. ITU and ETSI specifications permit a combined drift characteristic of all non-temperature-related parameters of up to 10 ppb per day, at constant temperature. The same specifications allow a drift of 1 ppm over a temperature range of 0 to +70°C.

Table 32 ITU and ETSI specification

Parameter	Value
Tolerance.	±4.6 ppm over 20-year lifetime.
Drift (Frequency drift over supply voltage range of +2.7 V to +3.3 V).	±0.01 ppm/day @ constant temperature.
	±1 ppm over temperature range 0°C to +70°C.

Telcordia specifications require a non-temperature-related drift of less than 40 ppb per day and a drift of 280 ppb over the temperature range 0 to +50°C.

Table 33 Telcordia GR-1244 CORE specification

Parameter	Value
Tolerance.	±4.6 ppm over 20 year lifetime.
Drift (Frequency drift over supply voltage range of +2.7 V to +3.3 V).	±0.28 ppm/over temperature range 0°C to +50°C.

Please contact DAPU for information on recommended crystal oscillator suppliers.

Oscillator frequency selection

Two oscillator frequency select pins (OSCFSEL1 and OSCFSEL0) set the expected local oscillator frequency, as shown in Table 34.

Table 34 Oscillator frequency selection truth table

OSCFSEL1	OSCFSEL0	Selection
0	0	XTAL source 20 MHz.
0	1	XTAL source 10 MHz.
1	0	XTAL source 12.8 MHz.
1	1	Not used.

Reset (PORB)

Active low. Must be active low for a minimum of 100 ns. The ACS9522 will internally hold reset on until the PLLs have settled, after which the device enters the operating mode selected on the SYSMODE[1:0] port (see Table 31). If PORB is forced low, all internal states are reset to default values.

Locked status

Indicates (active high) that the device has achieved lock to the selected reference. The degree of lock indicated is software defined. The LOCKED pin (F9) is used in PTP and self test modes only.

Firmware specific input/output (IO)

Use subject to firmware version. If not used, leave to float.

Power supply and internally connected pins and grounds

Power supply and grounds

The ACS9522 is supplied with +3.3 V and 1.2 V (see Table 11 and Table 12).

Internally connected pins

All other pins are internally connected. They should be connected to ground or left to float as described in Table 13.

ELECTRICAL SPECIFICATIONS

Electrical protection

Over-voltage protection

The ACS9522 may require over-voltage protection on input reference clock ports according to ITU Recommendation K.41[21]. DAPU protection devices are recommended for this purpose. See the protection section at www.DPTEL.com for appropriate parts.

ESD protection

Suitable precautions should be taken to protect against electrostatic damage during handling and assembly. This device incorporates ESD protection structures that protect the device against ESD damage at ESD input levels up to at least ±4 kV using the human body model (HBM) ANSI/ESDA/JEDEC standard JS-001-2012 for all pins except the AMI I/O pins which are protected up to 500 V. In addition the device is protected to at least +/-1000 V using the Charged Device Model (CDM) to JEDEC standard JESD22-C101-E.

Latchup protection

This device is protected against latchup for input current pulses of magnitude up to at least ±100 mA at JEDEC Standard No. 78C September 2010.

Absolute maximum ratings

The absolute maximum ratings of the ACS9522 are shown in Table 35. When these values are the same as the operating conditions given in Table 36, the device will operate at the maximum ratings

Table 35 Absolute maximum ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage DC, 3.3 V, input/output	V_{DDIO}	-0.5	-	3.7	V
Supply voltage DC, 3.3 V, analog	V_{A1}, V_{A2}, V_{A3}	-0.5	-	3.7	V
Supply voltage DC, 3.3 V, CMU	V_{DDCMU}	-0.5	-	3.7	V
Supply voltage DC, 1.2 V, CMU, digital	V_{DDCMUD}	-0.5	-	1.4	V
Supply voltage DC, 1.2 V, CORE	V_{DDCORE}	-0.5	-	1.4	V
SGMII Rx analogue supply voltage DC, 1.2 V.	$VDD_{ASGMIIRX0}$	-0.5	-	1.4	V
SGMII Tx analogue supply voltage DC. 1.2 V	$VDD_{ASGMIITX0}$	-0.5	-	1.4	V
SGMII Rx analogue supply DC, 3.3 V.	$VDD_{HASGMIIRX0}$	-0.5	-	3.7	V
SGMII TX analogue supply DC, 3.3 V.	$VDD_{HASGMIITX0}$	-0.5	-	3.7	V
SGMII digital supply DC, 1.2 V.	VDD_{SGMII0}	-0.5	-	1.4	V
SGMII RX analogue supply DC, 1.2 V.	$VDD_{ASGMIIRX1}$	-0.5	-	1.4	V
SGMII TX analogue supply DC, 1.2 V.	$VDD_{ASGMIITX1}$	-0.5	-	1.4	V
SGMII RX analogue supply DC, 3.3 V.	$VDD_{HASGMIIRX1}$	-0.5	-	3.7	V
SGMII TX analogue supply DC, 3.3 V.	$VDD_{HASGMIITX1}$	-0.5	-	3.7	V
SGMII digital supply DC, 1.2 V.	VDD_{SGMII1}	-0.5	-	1.4	V
Input voltage, non-supply pins	V_{IN}	-0.3	-	V_{DDIO}	V
Output voltage, non-supply pins	V_{OUT}	-0.5	-	V_{DDIO}	V
Storage temperature	T_{STOR}	-50	-	+125	ºC

CAUTION!
To avoid potentially damaging internal currents, the power rails should be applied to the device simultaneously (no more than 100 ms apart). See Figure 17.

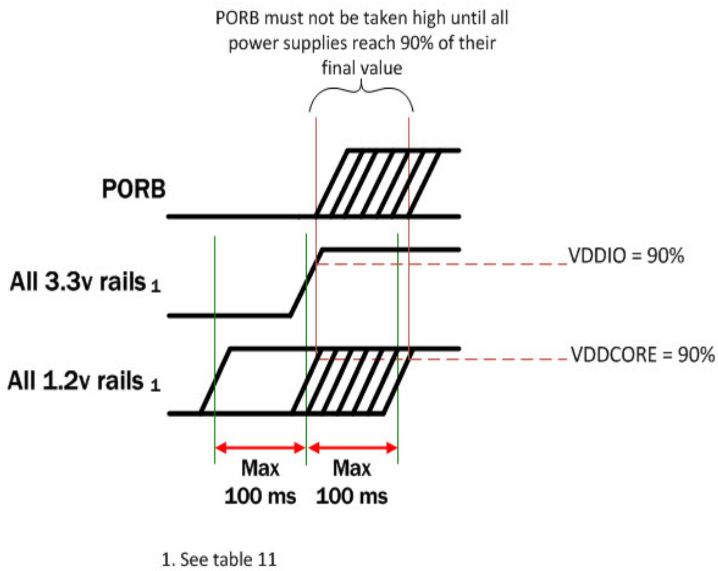

Figure 17 - Power rail application timing

Operating conditions

Table 36 Operating conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power supply DC voltage, 3.3 V, input/output	V_{DDIO}	3.135	3.3	3.465	V
Power supply DC voltage, 3.3 V, analog	V_{A1}, V_{A2}, V_{A3}	3.135	3.3	3.465	V
Power supply DC voltage, 3.3 V, CMU	V_{DDCMU}	3.135	3.3	3.465	V
Power supply DC voltage, 1.2 V, CMU, digital	V_{DDCMUD}	1.14	1.2	1.26	V
Power supply DC voltage, 1.2 V, CORE	V_{DDCORE}	1.14	1.2	1.26	V
SGMII Rx analogue supply voltage DC, 1.2 V.	$VDD_{ASGMIIRX0}$	1.14	-	1.26	V
SGMII Tx analogue supply voltage DC. 1.2 V	$VDD_{ASGMIITX0}$	1.14	-	1.26	V
SGMII Rx analogue supply DC, 3.3 V.	$VDD_{HASGMIIRX0}$	3.135	-	3.465	V
SGMII TX analogue supply DC, 3.3 V.	$VDD_{HASGMIITX0}$	3.135	-	3.465	V
SGMII digital supply DC, 1.2 V.	VDD_{SGMII0}	1.14	-	1.26	V
SGMII RX analogue supply DC, 1.2 V.	$VDD_{ASGMIIRX1}$	1.14	-	1.26	V
SGMII TX analogue supply DC, 1.2 V.	$VDD_{ASGMIITX1}$	1.14	-	1.26	V
SGMII RX analogue supply DC, 3.3 V.	$VDD_{HASGMIIRX1}$	3.135	-	3.465	V
SGMII TX analogue supply DC, 3.3 V.	$VDD_{HASGMIITX1}$	3.135	-	3.465	V
Ambient operating temperature range	T_A	-40	-	+85	°C
Supply current (3.3 V)	$I_{DDHASGMIIRX0}+I_{DDHASGMIITX0}+I_{DDHASGMIIRX1}+I_{DDHASGMIITX1}+I_{A1}+I_{A2}+I_{A3}+ +I_{DDCMU}+I_{DDIO}+I_{DD\_RAM}$	-	238[1] 209[2]	333[3]	mA
Supply current (1.2 V)	$I_{DDCORE}+I_{DDASGMIIRX0}+I_{DDASGMIITX0}+I_{DDASGMIIRX1}+I_{DDASGMIITX1}+I_{DDSGMII0}+I_{DDSGMII1}+I_{DDCMUD}$	-	230[1,2]	231[3]	mA
Total power dissipation	P_{TOT}	-	1.061[1] 0.962[2]	1.502[3]	W

1. Slave configuration, locking to a PTP Master with the PTP module supplying a 2.048 MHz reference to the TDM module and the TDM module providing a single 2.048 MHz output.
2. Master configuration, locking to a 1PPS reference and supporting a single Slave with the PTP module supplying a 2.048 MHz reference to the TDM module and the TDM module providing a single 2.048 MHz output.
3. Master configuration supporting 128 Slaves and the TDM module outputs TO1 to TO6 running at 125 MHz.

DC characteristics

Unless otherwise stated, the DC characteristics apply to all operating conditions.

Table 37 DC characteristics of the TTL ports

Parameter	Symbol	Minimum	Typical	Maximum	Units
TTL input port					
V_{IN} High.	V_{IH}	2	-	-	V
V_{IN} Low.	V_{IL}	-	-	0.8	V
Input current.	I_{IN}	-	-	10	μA
TTL input port with internal pull-up					
V_{IN} High.	V_{IH}	2	-	-	V
V_{IN} Low.	V_{IL}	-	-	0.8	V
Pull-up resistor.	PU	20	-	200	kΩ
Input current.	I_{IN}	-	-	100	μA
TTL input port with internal pull-down					
V_{IN} High.	V_{IH}	2	-	-	V
V_{IN} Low.	V_{IL}	-	-	0.8	V
Pull-down resistor.	PD	20	-	200	kΩ
Input current.	I_{IN}	-	-	100	μA
TTL output port (OPCLKx, PPNSx)					
V_{OUT} Low (I_{OL} = 8 mA).	V_{OL}	0	-	0.4	V
V_{OUT} High (I_{OH} = 8 mA).	V_{OH}	2.4	-	-	V
Drive current.	I_D	-8	-	8	mA
TTL output port (other pins)					
V_{OUT} Low (I_{OL} = 4 mA).	V_{OL}	0	-	0.4	V
V_{OUT} High (I_{OH} = 4 mA).	V_{OH}	2.4	-	-	V
Drive current.	I_D	-	-	4	mA

DESCRIPTION OF BLOCK DIAGRAM

Figure 2 shows a block diagram of the main functional blocks of the ACS9522. Some interfaces have been omitted for clarity. The diagram is not a physical representation of the actual design, but a simple diagram intended to assist with the description of the function of the device. For example, the PTP Block is described as a collection of sub-blocks each of which performs a specific duty; however, in reality, the PTP Block contains an embedded RISC microprocessor and various associated design cores, and the functionality is determined by software held in the Flash memory. In contrast, the TDM Block is a complete replication of the SETS function of an ACS8520 device. The three main multiplexers (TDM, PTP and OPClk Block multiplexers) interconnect the TDM and PTP blocks and can be controlled by the host microprocessor to route clock signals between the blocks as needed.

The PTP Block

Figure 18 shows a block diagram of the PTP Block. The main functions are described below. Control of the blocks is achieved by using API calls. For details, please refer to the API documentation in the DPSync Resource Center[1].

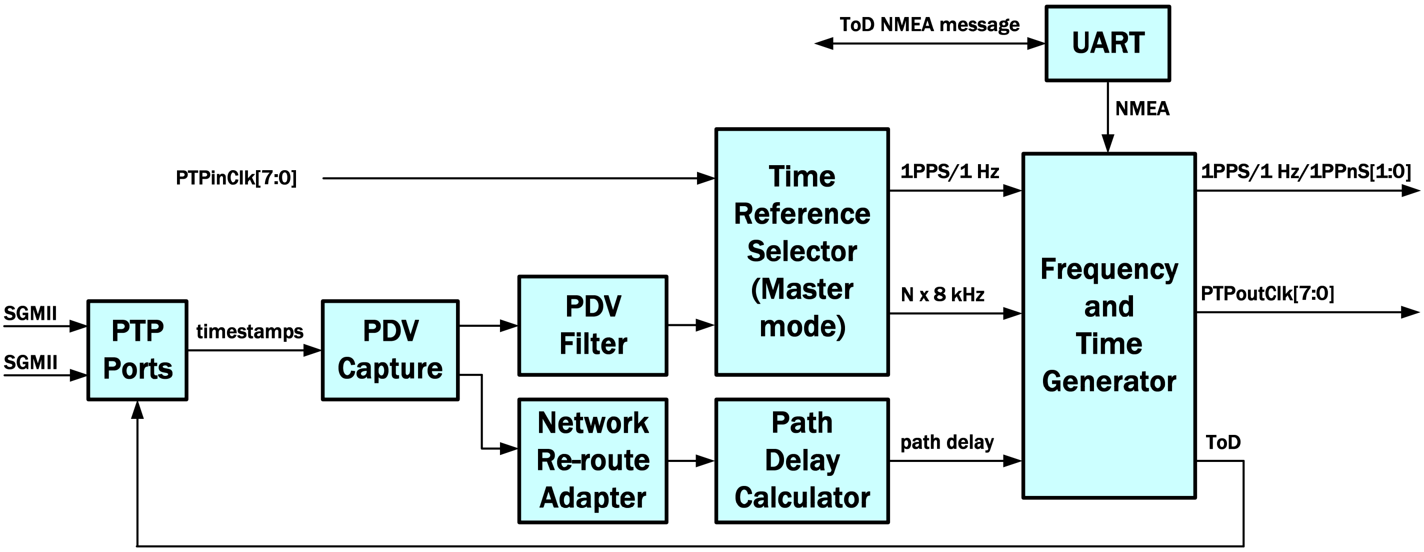

Figure 18 - Block diagram of PTP functions

PTP port

The PTP port is the interface to the rest of the PTP network. It handles PTP controls and performs hardware timestamping. The PTP port has many configurable functions involved in interfacing with the network. These functions have sensible defaults which suit many situations. If specific configurations are required, these can be performed using appropriate API calls, the most important of which are listed in PTP port API calls.

The PTP Port operates at the MAC layer of the Ethernet stream. It is responsible for generating PTP timestamps for all PTP event messages. The timestamps use the local timebase generated by the frequency and time generator.

When the ACS9522 is operating in the Master Clock mode, the PTP Port generates the timestamps of all outgoing Sync messages (the t1 timestamp) and the timestamps of all incoming delay-request messages (the t4 timestamp). It also inserts the timestamps of all received delay-request messages into the timestamp field of the corresponding delay-response messages.

When the ACS9522 is operating in the Ordinary Clock (OC, an end-point slave clock) mode, the PTP Port generates timestamps for all incoming Sync messages (the t2 timestamp) and all outgoing delay-request messages (the t3 timestamp).

PTP port API calls

API calls that are relevant to this block are described in the DPSync Control Interface Functional Specification in the API Documentation and User Guide.

PDV capture

When the ACS9522 is operating in the OC mode, the PDV Capture function calculates the apparent delays in each direction and files them in sequence for processing by the PDV Filter function.

PDV filter

When the ACS9522 is operating in the OC mode, the PDV Filter function calculates a mix of statistics from the PDV Capture file. These statistics are then used by the Path Delay Calculator.

Network re-route adapter

When the ACS9522 is operating in the OC mode, the Network Re-route Adapter detects path change events. The amplitude and direction of the path change are supplied to the Path Delay Calculator.

Path delay calculator

When the ACS9522 is operating in the OC mode, the Path Delay Calculator determines the path delay between the Master and Slave clocks. It uses the PDV statistics calculated by the PDV Filter, together with the path change vector calculated by the Network Re-route Adapter. The path delay is supplied to the Frequency and Time Generator, where the local timebase is aligned with the Master timebase. The path delay is used to align the output phase with the input phase of the remote PTP GM. Path delay compensation is not required for frequency transport and is not used when the PTP flow is one-way only. The output of the Network Re-route Adapter is still used to prevent large path delays causing transient steps on the output phase.

API calls that are relevant to this block are described in the DPSync Control Interface Functional Specification in the API Documentation and User Guide.

PTP input reference port (time selector)

The PTP Input Reference Port is used to supply a local source clock when in the PTP Master mode. It is responsible for selecting the reference source which should be used to drive the rate of the local timebase. The selection is controlled by host code. The PTP Input Reference Port accepts up to 8 input clock signals from the PTP Block Multiplexer. These signals may have been routed directly to the PTP Block from the IPCLK input pins, or they may first have gone through the TDM Block. They can be independent signals and can operate at individual frequencies, but they must obey the following rule:

Input Freq = k * 2^n, where 0 <= n <= 5 and 1 <= k <= 2^32 (upper limit of 170 MHz)

(For example, for an input frequency of 2.048 MHz, k would be 64,000 and n would be 5, so 64,000 x 2^5 = 2,048,000).

If an input reference signal is passed first through the TDM Block, then it may have a frequency which does not obey the above rule. However, the TDM Block can generate a new frequency, which must be selected to obey the rule (a commonly-used frequency is 8 kHz).

Under software control, one of the active inputs will be selected and passed to the Frequency and Time Generator to control the rate of change of the local timebase. If the input clock signal is a telecom-rate clock (or an integer multiple of 8 kHz) and is expected to contain significant levels of wander noise, the signal may first be passed through the SETS function to reduce this.

The routing is obtained by controlling the TDM Block Multiplexer, the SETS T0/T4 Output Selectors, and the PTP Block Multiplexer; appropriate API calls are available for all of these actions.

If, however, the input is a 1PPS signal, then this cannot be passed through the SETS function; however, 1PPS is expected to be a very quiet signal because it would not have passed along a network.

Whatever its rate, the input clock signal or a clock derived from the input clock signal is supplied to the Frequency and Time Generator to control the rate of change of the local timebase. If the Master is to provide a frequency delivery service, there is no need to align the local timebase to any external timebase and its epoch will be the beginning of the PTP timebase (in other words, the first timestamp generated after power-on will indicate 1st January 1970, whatever the actual time and date).

If the selected input clock signal is a 1PPS signal, and if the Master timebase should be aligned to Temps Atomic International (TAI, International Atomic Time), then the ingoing 1PPS signal should indicate the top-of-second point and the current second will be indicated in a timing message going in on the UART. Similarly, if the Master should be aligned to an external timebase which is not traceable to TAI, the timing message will hold the current seconds count of the external timebase but neither this value, nor the 1PPS signal, will necessarily be aligned to TAI.

API calls that are relevant to this block are described in the DPSync Control Interface Functional Specification in the API Documentation and User Guide.

UART

The ACS9522 includes a UART to which the timing message is written when the PTP Block is acting in the PTP GM mode. This is only needed when a PTP GM must be aligned with an external timebase (TAI or arbitrary). A timing message is generated by the UART when the block is acting in the PTP OC mode. The message could be ignored if the PTP timebase is free-running. The UART is a LVTTL-compatible port and needs an external translator to work with other signal types (such as RS-232C or RS-485). The format of the timing message is shown in Time of day message format.

The timing message should be provided regularly; a consecutive sequence of 3 missing timing messages is taken to indicate that the reference source timebase has failed. This will activate an alarm which can be accessed using an API call; the time-traceable flag in outgoing Sync messages will be cleared. The timing message carries GPS time and not TAI. If the PTP Master is to be aligned to TAI, then it must convert GPS time to PTP time (derived from TAI), but the Master must know the current count of leap seconds since the GPS epoch. The PTP Master obtains this from host code using an API call. The PTP Master must also know when a leap second event is pending, and this is also obtained from host code using an API call.

When a PTP OC is aligned to TAI, it converts PTP time to GPS time for the outgoing timing message, and allows leap second information to be read using an API call. Given the GPS time and current leap second information, an application can easily obtain any other timescale (TAI, UT1, etc). When the PTP timebase is either arbitrary or free-running, the timing message carries the current time of the timebase in GPS format. Leap second information is not needed in these cases.

API calls that are relevant to this block are described in the DPSync Control Interface Functional Specification in the API Documentation and User Guide.

Frequency and time generator

The Frequency and Time Generator is the heart of the ACS9522 PTP Block. In PTP Master mode, the function generates the local timebase at a rate determined by the clock signal supplied to it by the PTP Input Reference Port (or by the local oscillator if no such signal is available). If the Master timebase is required to be aligned to an external timebase, then the signal supplied should be a 1PPS signal and the rising edge should indicate the top-of-second point of the external timebase. The function will align the timebase so that the beginning of each new second occurs coincidentally with the top-of-second point.

The 1PPS signal is checked for consistency and low jitter before being accepted. It requires three consecutive pulses spaced at a nominal 1-second interval and is rejected if a pulse is missed. The timebase time and date will be aligned to the external timebase using the values presented in the timing message on the UART, but converted to the PTP epoch. If the external timebase is TAI, the leap second information will also be used.

In the PTP OC mode, the timebase will use the path delay from the Path Delay Calculator to align itself to the timebase of the PTP Master. The timebase will be aligned to the PTP epoch, but is converted to UTC time using the leap second information carried in the PTP messages, so that the UART output timing message carries UTC time. If the application needs to convert the UTC time to TAI, it can retrieve the UTC offset by using the appropriate API call.

In Master mode and OC mode, this function is responsible for the holdover performance. Holdover performance depends on two characteristics: adequate stability of the local oscillator and adequate holdover data acquired whilst locked to a stable reference source. The former is satisfied by selecting a suitable oscillator. The latter is satisfied by ensuring that the ACS9522 is adequately locked to a suitable reference source for an adequate period of time.

The selection of the reference source is determined by factors outside the ACS9522, but making sure that the device is adequately locked before it begins to acquire holdover data, and then acquiring holdover data for a long enough period, are actions that the device can execute.

Firstly, the device will not begin to acquire holdover data until it is adequately locked.

Secondly, the device will acquire holdover data for a rolling period set by the software.

The phase of an output clock signal of an OC is fundamentally tied to the asymmetry in the path delays in each direction; changes in asymmetry naturally feed through to the phase of the output, causing a phase error. This can be minimised, or avoided, by enabling the suppression of phase jumps.

API calls that are relevant to this block are described in the DPSync Control Interface Functional Specification in the API Documentation and User Guide.

For the frequencies available at output ports OPCLK[3:0] in PTP modes, an output frequency (F_{OUT}) is programmed in Hz via the API interface. Not all possible values of F_{OUT} are supported (i.e. not all 1 Hz increments). The maximum value of F_{OUT} is 62.5 MHz.

To determine whether a particular value of F_{OUT} is supported, apply the following test:

M must be an integer less than 2^{17} (131072) where M is calculated as below:

GCD = greatest common divisor of 125 x 10^6 and F_{OUT}
M = 125 x 10^6/GCD

See GPRMC message format for information on the phasing of output clock PHASEOPCLK.

Refer to the ACS9522 User Guide, the Application Programmers Interface Document and the DPSync Resource Center.

Phase-aligned clock port

Output ports OPCLK[3:0] may be individually programmed to carry one of a set of clock signals, PHASEOPCLK[3:1] respectively, which are specially conditioned to maintain a tight phase alignment with the PPnS0 signal. See GPRMC message format for information on the phasing of output PHASEOPCLK.

The phase-aligned clock channels are used in PTP modes only.

PPnS0 - a single pulse per n second reference output with a fully programmable *high* time (default 1 ms). The rising edge specifies the seconds rollover point.

PHASEOPCLK - phase-aligned with PPnS0. Default 5 MHz programmable as an integer division of 125 MHz subject to the following limits:

maximum of 25 MHz (divide by 4).
minimum of 100 Hz (divide by 1249999).

with the divisor calculated according to the formula: *divisor=(125MHz/frequency)-1*

Note that PHASEOPCLK may be selected on OPCLK0 to OPCLK3. See the ACS9522 Application Note[32].

Importance of the local oscillator

The PTP Block contains digital phase locked loops which perform filtering duties when the ACS9522 is acting as an OC. These filters use long time constants and therefore a stable source of frequency is required locally. This is usually provided by a compensated crystal oscillator. The stability of this oscillator can have a significant impact on the performance so care must be taken to select an oscillator that will support the performance required by the application being driven by DPSync. The performance requirements can often be met using a suitable temperature-controlled crystal oscillator (TCXO), but some applications will require an oven-controlled crystal oscillator (OCXO).

The choice of oscillator type can depend on the amount of noise (i.e. packet delay variation) in the path between the GM and the OC which, unfortunately, is impossible to predict accurately. The best recommendation is to plan to fit an OCXO and exchange it for a less expensive device if network circumstances permit. The PTP Block can operate with local oscillators operating at frequencies of 10 MHz, 12.8 MHz or 20 MHz.

Self test

The ACS9522 device includes a software module which tests the Ethernet PHYs connected to it. Full details are contained in associated document Application Note AN-TS 2 5.0 Self Test Module Test Specification.

The self-test software module is instigated by controlling mode selection pins SYSMODE[1:0] as shown in Table 31, and performing a power-on reset cycle.

The TDM Block

Figure 19 is a block diagram of the TDM Block showing the main functions. They are described below.

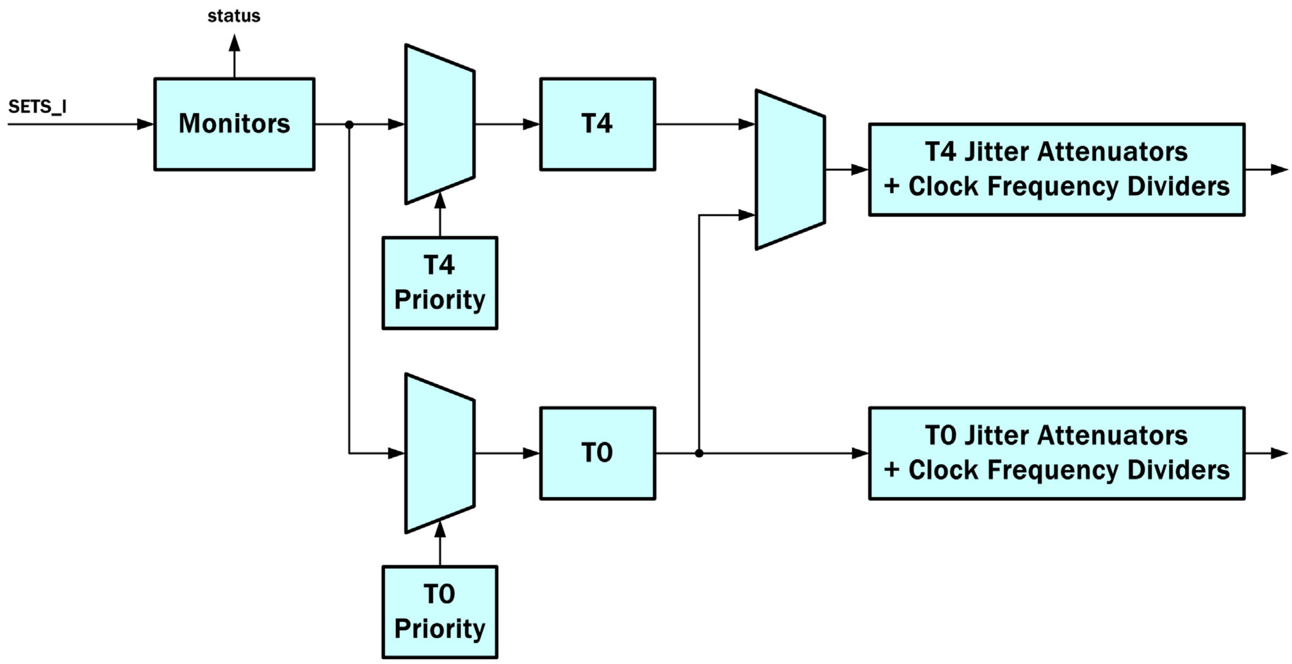

Figure 19 - Block diagram of TDM functions

SETS reference sources

The TDM Block of the ACS9522 supports up to 14 possible reference sources, using a range of I/O technologies to suit many design situations. A wide range of pre-determined spot frequencies can be selected from for each reference source individually. The spot frequencies match popular bit rates found in telecom networks in both the ETSI and ANSI hierarchies, as listed below. Alternatively, any integer multiple of 8 kHz can be applied to any individual reference by employing an integrated pre-divider circuit to divide a frequency down to 8 kHz (refer to section DivN Mode for details). This allows the SETS function to receive frequencies which are not commonly used in telecom networks, including 10 MHz and 25 MHz.

Acceptable input frequencies for the LVTTL inputs of the TDM Block:

n × 8 kHz.

1.544 MHz (SONSDHB=SONET)/2.048 MHz (SONSDHB=SDH).

6.48 MHz.

19.44 MHz.

25.92 MHz.

38.88 MHz.

51.84 MHz.

77.76 MHz.

Input clock IPCLK8 and IPCLK11 are differential inputs which can accept the same frequencies as IPCLK[3:0] and also 2 kHz, 4 kHz and 155.52 MHz.

Input clocks IPCLK9 and IPCLK10 are for AMI composite 64 kHz/8 kHz clocks as defined in Appendix II.1 of ITU Recommendation G.703[8].

Monitors

Each reference source can be individually monitored for activity and frequency offset.

The frequency offset monitors can detect references that are more than 13 ppm off frequency. They should not be expected to reject references that are free-running within the allowed 4.6 ppm, nor any that are in holdover (until they pass beyond the 13 ppm threshold, but that can take many hours). However the frequency offset monitors can detect references that are wildly out of range. They are an optional feature in G.781[28].

The activity monitors can detect failure of their references, or erratic behavior. They are best used to detect failures within the equipment (bad connectors, faulty devices, etc.).

Any references which the monitors declare as invalid are automatically suspended from the priority tables until declared valid again. Such suspensions and restorations are instantaneous, and there is no hold-off or wait-to-restore operation applied by the device. As such, the monitors do not meet the requirements of G.781[28]. However, external timers can be used to apply holdoff and wait to restore periods and these can be used to enable the selection of references.

The T0 and T4 paths can switch automatically between the references in their priority tables. Alternatively, each channel can be forced to select a particular reference source. Using the forced-selection capability in conjunction with hold-off and wait-to-restore timers implemented in host software, the monitors can be made compliant to G.781[28]. Such software can integrate the monitors together with other reference disqualifiers such as Loss of Signal (LOS), Alarm Indication Signal (AIS), Synchronous Status Messages (SSM), etc, to protect the timing from remote and local failures.

T0 source selection

Each reference source can be given a unique priority to position it in the selection order of the T0 signal. Phase build-out can be used when switching between references for the T0 signal in order to maintain the output phase when the new reference phase is significantly different to the phase of the previous reference.

The ACS9522 includes a holdover mode for use by the T0 signal when no reference is available. Holdover is similar to the free running mode in that the output phase drift is determined by the quality of the local oscillator. However, the initial frequency offset, compared to the long-term average of the reference source, is reduced as much as possible. Holdover is normally used when all preferred references have been disqualified.

However, it can also be used temporarily to help avoid phase disturbances on the output when the selected reference suffers a problem; the T0 signal would be forced by software into the holdover mode while the software runs through the hold-off period to check if the reference has suffered a real problem or is just undergoing a temporary disturbance. The order of source selection can be pre-configured into the T0 priority table and T0 source selection can be driven by the status of the internal monitors; however external failures such as cable breaks or upstream failures must be handled by an external mechanism. In particular conditions such as LOS or AIS should be soaked in external holdoff and wait to restore timers the result used to determine the preferred source.

T4 source selection

In addition to the priority used for selecting the T0 signal, each reference source can also be given a second unique priority to position it in the selection orders of the T4 signal.The order of source selection can be pre-configured into the T4 priority table and T4 source selection can be driven by the status of the internal monitors; however external failures such as cable breaks or upstream failures must be handled by an external mechanism. In particular conditions such as LOS or AIS should be soaked in external holdoff and wait to restore timers the result used to determine the preferred source.

T0 digital phase-locked loop

The SETS function of the ACS9522 provides a configurable loop filter bandwidth down to 100 milliHertz (mHz) to filter the reference that feeds the T0 signal.

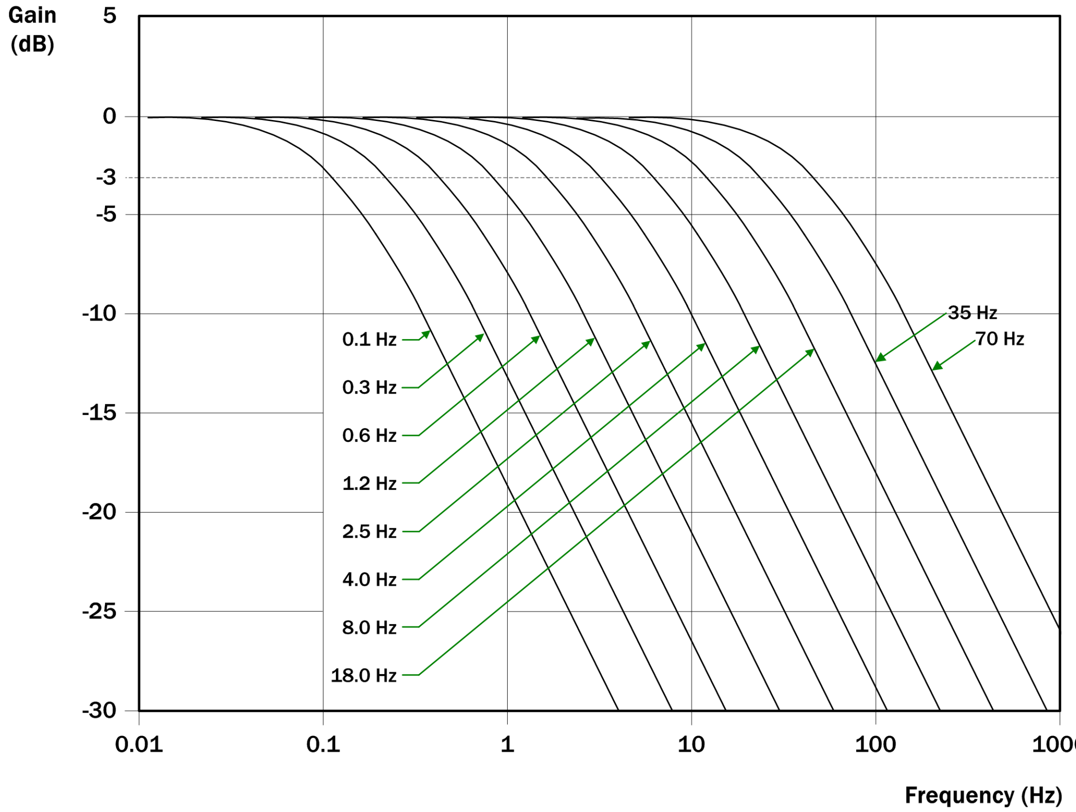

Figure 20 - Sample of measured wander and jitter transfer

T4 digital phase-locked loop

The SETS function also provides a filter, down to 18 Hz, for the T4 signal.

T4 output selection

In accordance with G.783[11], it is possible to obtain the T4 signal from the post-filtered T0 signal using the T4 Output Selection Multiplexer.

T0 analog phase-locked loop, clock dividers and output selectors

The SETS function includes analog phase locked loops to reduce jitter on the output signals. Jitter levels suitable for direct use at output frequencies up to 155.52 MHz are achieved; for applications which require higher frequencies, external phase locked loops should be used to raise the frequency and reduce the jitter further. The SETS function provides up to 11 output signals simultaneously. The output signals can be routed to the output pins via the SETS Output Selection Multiplexer and the OPCLK Block Multiplexer. A wide range of output frequencies is provided, again at pre-determined spot frequencies chosen to suit the TDM telecom networks. Each output can be configured separately to provide one of the spot frequencies, although the choice is not the same on all outputs.

T4 analog phase-locked loop, clock dividers and output selectors

Similarly to the T0 channel, an analog phase locked loop is used on the T4 signal to obtain lower jitter levels. Up to 9 output signals can be generated simultaneously, and most signals can chose from a range of frequencies. The output signals can be routed to the output pins via the SETS Output Selection Multiplexer and the OPCLK Block Multiplexer.

SETS output selection

Many of the outputs can select between the T0 and T4 signals. The final selection of which signals appear on the output pins is made by the OPCLK Block Multiplexer. The output frequencies in TDM Timing mode are given in Table 45 to Table 48.

USING THE TDM BLOCK

The following description refers to the block diagram of TDM functions in the ACS9522 Application Note[32].

The ACS9522 device accepts 18 input clocks, of which up to 14 can be used in the TDM Timing mode. From these, the device generates 11 output clocks, and has a total of 59 possible output frequencies.

Of the 18 input references, two are AMI composite clocks, two are LVDS/LVPECL and the remaining 14 are TTL/CMOS compatible inputs. The AMI inputs are ±1 V and are typically AC-coupled. Refer to ELECTRICAL SPECIFICATIONS for more detailed information on the device's electrical performance.

The range of supported input frequencies is 2 kHz to 155.52 MHz. The DPLLs directly lock to common telecom frequencies and sub-divisions. An inbuilt programmable frequency divider also allows locking to any input frequency that is a multiple of 8 kHz, up to a maximum of 100 MHz.

Note that most input clock ports are disabled by default and must be enabled before use; please refer to the TDM Block register set for details.

When using automatic input reference selection, the T0 path has a more complex state machine than the T4 path. The T0 and T4 PLL paths support the following common features:

- Automatic source selection according to assigned input priorities and measured input quality level.
- Different quality levels (activity alarm thresholds) can be assigned to each input.
- Variable bandwidth, lock range and damping factor.
- Direct PLL locking to common SONET/SDH input frequencies, or any multiple of 8 kHz.
- Automatic mode switching between free-run, locked and holdover modes.
- Fast detection of input failure and entry into holdover mode (holds at the last good frequency value).
- Frequency translation between input and output rates via direct digital synthesis.
- High accuracy digital architecture for stable PLL dynamics, combined with an APLL for low-jitter final output clocks.

There are a number of features supported by the T0 path that are not supported by the T4 path. These features could all be implemented for the T4 path in the host software, if required. These additional T0 features are:

- Non-revertive mode.
- Phase build-out on source switch (hit-less source switching).
- I/O phase offset control.
- Bandwidth is programmable in 10 steps between 0.1 Hz to 70 Hz in 10 steps (For the T4 path the bandwidth is programmable in 3 steps: 18 Hz, 35 Hz and 70 Hz).
- Noise rejection on the low frequency input.
- Manual holdover frequency control.
- Controllable automatic holdover frequency filtering.
- Frame sync pulse alignment.

The operation of the DPLL in the T0 path is either controlled by software, or by an internal state machine. The state machine for the T4 path is very simple and cannot be manually set or controlled externally. Overall operation of the T4 path can be controlled by manual selection of reference sources. One additional feature of the T4 path is the ability to measure a phase difference between two inputs.

The T0 path DPLL always produces an output at 77.76 MHz to feed the APLL, regardless of the frequency selected at the output pins. The T4 path can be operated at a number of frequencies. This is to enable the generation of extra output frequencies which cannot be easily related to 77.76 MHz. When the T4 path is selected to lock to the T0 path, the T4 DPLL locks to the 8 kHz output from the T0 DPLL. This is because all of the possible operating frequencies of the T4 path can be divided to 8 kHz. Using the T0 8 kHz output in this way ensures synchronization of all the frequencies within the two paths.

The outputs of both DPLLs are connected to multiplying and filtering APLLs. The outputs of these APLLs are fed into output dividers, providing a number of frequencies that can be simultaneously selected at the output clock ports. The various possible combinations of DPLLs, APLLs and frequency divider allow a comprehensive set of frequencies to be generated, as listed in the Output frequency selection and configuration section.

Input reference clock ports in the TDM Timing mode

Because inputs can be switched between the T0 and T4 paths, this entire section applies to both paths.

Input reference source selection and priority table gives details of the input reference ports, showing the input technologies and the range of frequencies supported on each port. The table also lists the default spot frequencies and default priorities that are assigned to each port when the device is reset or is powered up. SDH and SONET networks use different default frequencies. To allow for this, the network type is selectable. On power-up, or after a reset, the default network type is set by the state of the SONSDHB pin.

The network type can also be selected by setting the *ip_sonsdhb* bit in the cnfg_input_mode register:

for SONET, *ip_sonsdhb* = 1.

for SDH, *ip_sonsdhb* = 0.

Specific frequencies and priorities are set by configuration.

Frequency selection is programmed via the appropriate *cnfg_ref_source_frequency* register.

Locking modes

There are three locking modes that can be configured:

Direct lock mode
Lock8K mode
DivN mode

Direct lock mode

In direct lock mode, the internal DPLL directly locks to the selected input frequency. For example, if the input frequency is 19.44 MHz, the circuit performs the DPLL phase comparisons at 19.44 MHz. This mode can be used on any of the 14 inputs to the TDM Block.

The maximum frequency allowed for phase comparisons in this mode is 77.76 MHz. However a feature is provided on the high-speed differential inputs to accommodate the special frequency of 155.52 MHz. To use a 155.52 MHz input, set the input to direct lock mode, and a frequency divider is automatically selected to halve the frequency before it is presented to the DPLL.

Lock8K mode

Lock8K mode is available individually on each of the 14 inputs to the TDM Block. Each input includes an internal frequency divider which, when Lock8K mode is selected for that input, is automatically configured to produce an 8 kHz internal frequency. The DPLL then locks to this 8kHz signal if the input channel is the selected source. This mode provides a greater tolerance to input jitter than direct lock mode. However Lock8K mode can only be used with certain supported spot frequencies.

Lock8k mode is enabled by setting the Lock8k bit in the appropriate *cnfg_ref_source_frequency* register location. Setting the 8K edge polarity bit in test_register1 configures the DPLL to lock to either the rising edge or the falling edge of the input reference clock.

DivN mode

DivN mode uses a single internal frequency divider to provide the DPLL input frequency. The divider ratio must be manually set by configuration, and the divider can be applied to just one of the 14 TDM Block inputs at a time. The divider must be configured so that the frequency after division is 8 kHz. It can be used with a much greater range of input frequencies than Lock8k mode.

In DivN mode the input frequency can be divided by any integer value between 2 to 12500. Consequently any input frequency which is a multiple of 8 kHz, between 8 kHz to 100 MHz, can be supported by using DivN mode.

The division factor is programmed using the cnfg_freq_divn [7:0] and cnfg_freq_divn [13:8] registers. The division factor is the combined value in the two registers plus one.

DivN mode is enabled by setting the *divn_<n>* bit in the appropriate *cnfg_ref_source_frequency* register location.

NOTE: Any reference input can be set to use DivN mode independently of the frequencies and configurations of the other inputs. Only one value of N is allowed at a time, so all inputs with DivN selected must be running at the same frequency if re-programming is to be avoided. However, if different frequencies are used on individual inputs, then corresponding individual values of N can be programmed in when the input selection is changed to divide the selected input down to 8kHz.

DivN Examples

To lock to 2.000 MHz:

a) Set the *cnfg_ref_source_frequency* register to 10XX0000 (binary) to enable DivN mode, and set the frequency to 8 kHz - the frequency required after division. (XX = "Leaky bucket" ID for this input).

b) To achieve 8 kHz, the 2 MHz input must be divided by 250. So, if DivN = 250 = (N + 1)

then N must be set to 249. This is done by writing F9 hex (249 decimal) to the DivN register pair cnfg_freq_divn [7:0] and cnfg_freq_divn [13:8].

To lock to 10.000 MHz:

a) The *cnfg_ref_source_frequency* register is set to 10XX0000 (binary) to set the DivN and the frequency to 8 kHz, the post-division frequency. (XX = "Leaky bucket" ID for this input).

b) To achieve 8 kHz, the 10 MHz input must be divided by 1,250. So, if DivN, = 1250 = (N+1)

then N must be set to 1,249. This is done by writing 4E1 hex (1,249 decimal) to the DivN register pair cnfg_freq_divn [7:0] and cnfg_freq_divn [13:8].

To lock to 25.000 MHz:

a) The *cnfg_ref_source_frequency* register is set to 10XX0000 (binary) to set the DivN and the frequency to 8 kHz, the post-division frequency. (XX = "Leaky bucket" ID for this input).

b) To achieve 8 kHz, the 25 MHz input must be divided by 3,125. So, if DivN, = 3125 = (N+1)

then N must be set to 3,124. This is done by writing C34 hex (3,124 decimal) to the DivN register pair cnfg_freq_divn [7:0] and cnfg_freq_divn [13:8].

LVPECL and/or LVDS input port selection

The choice of LVPECL or LVDS compatibility is programmed via the cnfg_differential_inputs register. Unused LVPECL differential inputs should either be fixed with one input high (VDD) and the other input low (GND), or set in LVDS mode and left floating. In the latter case, one input is internally pulled high and the other low.

AMI input port selection

An AMI port supports a composite clock. This consists of a 64 kHz AMI clock with 8 kHz boundaries marked by deliberate violations of the AMI coding rules, as specified in ITU recommendation G.703[8]. Departures from the nominal pattern are detected within the ACS9522, and may cause reference-switching if they are too frequent. See section AMI input and output ports, for more details.

If the AMI port is unused, the pins for input channel I1 and input channel I2 should both be tied to GND.

Clock quality monitoring in the TDM Block

This section applies to both the T0 and the T4 path.

The ACS9522 continually monitors all the reference clock inputs supplied to the TDM Block, so that it can select the best available reference clock if the current reference source fails.

For each input, the following parameters are monitored:

- Activity (toggling).
- Frequency (performed only when there is no irregular operation of the clock, or loss of clock condition).

Anomalies on the currently selected clock could affect the accuracy of the output clock, and must be dealt with immediately. Anomalies occurring on a non-selected reference source only affect that source's suitability for selection.

The following parameters are monitored:

- Activity (whether the input is toggling or not).
- Frequency (this monitoring is only performed when there is no irregular operation of the clock, or loss of clock condition).

This information is used to modify the priority tables of the local and remote ACS9522 devices.

In addition, input channels I1 and I2 carry AMI-encoded composite clocks that are monitored by the AMI-decoder blocks. LOS is declared by the decoders when the signal amplitude falls below +0.3 V or there is no activity for 1 ms.

Any reference source that suffers a loss-of-activity or clock-out-of-band condition is declared unavailable. The currently selected reference source can be disqualified for phase, frequency, inactivity or if the source is outside the DPLL lock range. If the currently selected reference source is disqualified, the qualified reference source with the next highest priority is selected.

Anomalies detected by an activity detector are integrated in a leaky bucket accumulator. Occasional anomalies do not cause the accumulator to cross the alarm setting threshold, so the selected reference source is retained. Persistent anomalies cause the alarm setting threshold to be crossed and result in the selected reference source being rejected.

Anomalies on the currently selected input reference clock could induce jitter or frequency offsets in the output clock, leading to anomalous behavior. These anomalies must be detected immediately, and the phase locked loop must be temporarily isolated until the clock is once again pure. The activity monitoring process described above is too slow for this purpose. The required fast response is provided by a fast activity detector in the phase locked loop itself. This is fully described in Ultra fast switching.

The reporting of inactivity, reference selection criteria, and methods of programming particular trigger settings are described in the ACS9522 API documentation.

A detailed description of the leaky bucket accumulator, is given in Activity monitoring in TDM Timing mode.

Activity monitoring in TDM Timing mode

The ACS9522 uses leaky bucket accumulators to control whether clock inactivity irregularity triggers an alarm. This circuit allows infrequent irregularities to be tolerated, whereas events occurring more frequently than a certain average rate trigger the alarm. Each reference input has its own dedicated leaky bucket accumulator.

The leaky bucket is a digital accumulator. circuit, operating on a 128 ms cycle. If an unacceptable irregularity occurs within a 128 ms cycle, then the accumulator is incremented by 1. If the accumulator reaches a programmable threshold number, then an alarm is raised. If no irregularities occur within the 128 ms cycle, then the accumulator is decremented by 1 every 1, 2, 4 or 8 cycles.

For each 128 ms cycle, there are four possible outcomes:

- One or more unacceptable events occur on the input. The accumulator is incremented by 1.
- One or more unacceptable events occur on the input, but the accumulator has reached its maximum size. The accumulator holds it value.
- No events occur on the input. No decrement is due, so the accumulator hold its current value.
- No events occur on the input, but a decrement is due. The accumulator is decremented by 1.

It can be seen that if an event occurs in the same cycle as a decrement is due, then the decrement is blocked.

The alarm setting threshold can be programmed to set the accumulator value which triggers an alarm. The leaky bucket incorporates hysteresis. This means it does not reset the alarm until the accumulator value has fallen below a second programmable threshold number. Once the leaky bucket alarm has been set, the input clock quality must improve significantly before the alarm can be reset, see Figure 21.

There is one leaky bucket accumulator per input channel. Each leaky bucket can be set to one of four possible configurations (leaky bucket configuration 0 to 3). Each leaky bucket configuration is programmable for bucket size, alarm set and reset thresholds, and decay rate.

Because each source is monitored over a 128 ms period, the fastest possible fill rate for the leaky bucket accumulator is 8 units/sec. The leak rate of the accumulator can be programmed in multiples of the fill rate (x 1, x 0.5, x 0.25 and x 0.125), to give a programmable leak rate between 8 units/sec and 1 unit/sec.

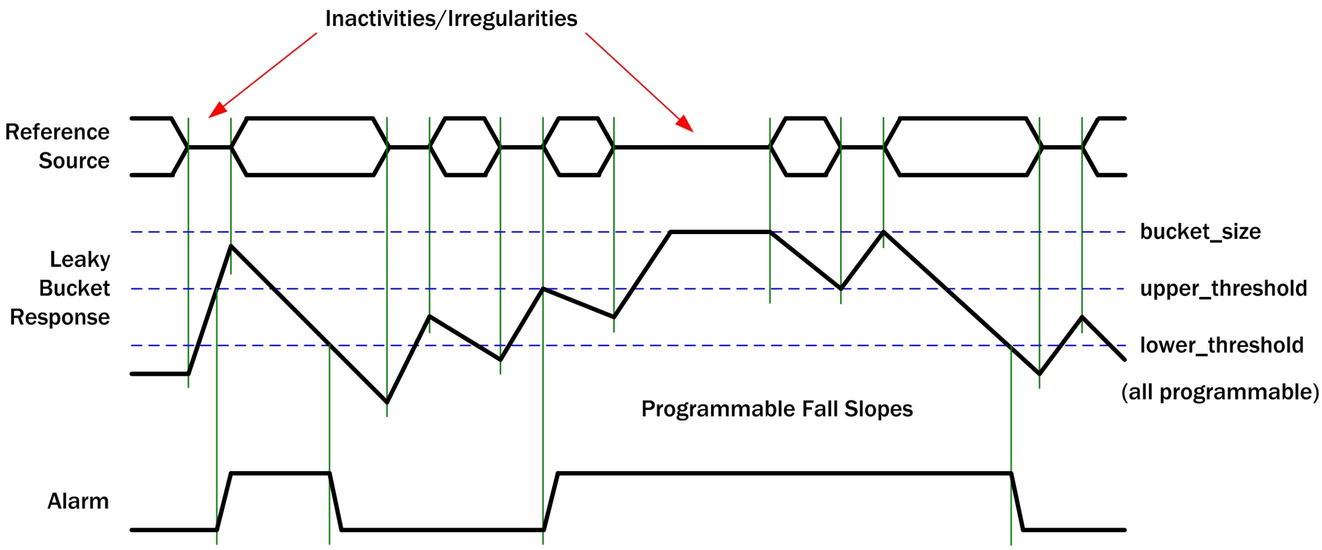

Figure 21 - Operation of the leaky bucket accumulator

Leaky bucket timing

Assume that a reference source has previously been fully active, so that its corresponding leaky bucket accumulator is empty. The time in seconds taken to raise an inactivity alarm if the source disappears is:

(cnfg_upper_threshold_n) / 8

where n is the number of the leaky bucket configuration.

This corresponds to one irregularity every 128 ms cycle of the leaky bucket.

If an input is intermittently inactive, then the time to raise an inactivity alarm is longer than this.

The default setting of *cnfg_upper_threshold_n* is 6, corresponding to a minimum alarm activation time of 0.75 seconds.

Assume that a reference source has previously been completely inactive, so that its corresponding leaky bucket accumulator is full. The time in seconds taken to cancel the activity alarm once the reference source returns is:

$[2^{(a)} \times (b - c)] / 8$

where:

a = cnfg_decay_rate_n
b = cnfg_bucket_size_n
c = cnfg_lower_threshold_n
(where n = the number of the relevant leaky bucket configuration).

The default configuration of the leaky bucket gives the following minimum alarm de-activation time:

$[2^1 \times (8 - 4)] / 8 = 1.0$ secs

Frequency monitoring of clock inputs

The ACS9522 performs frequency monitoring to identify reference sources which have drifted outside the acceptable frequency range. This acceptable range is measured with respect to either the output clock, or to the local oscillator clock.

The *sts_reference_sources* registers contain out-of-band alarms for each of the inputs. For IPCLK[3:0] and IPCLK[8], the out-of-band alarm for a particular reference source is raised when the reference source is outside the acceptable frequency range. With the default register settings, a soft alarm is raised if the drift exceeds ±11.43 ppm, and a hard alarm is raised if the drift exceeds ±15.24 ppm. Both of these limits are programmable between ±3.8 ppm and ±61 ppm.

The reporting of out-of-frequency conditions for all inputs is described in the API documentation for this product[1].

The ACS9522 DPLL has a default lock and capture range frequency limit of ±9.2 ppm. This limit is also programmable up to ±80 ppm.

Selection of input reference clock sources

The ACS9522 can allow the input reference sources to be selected automatically by an order of priority. The T0 and T4 paths can do this individually. The individual priority tables for the T0 and T4 paths can be changed automatically in response to the internal monitoring, and reference-switching can occur when the highest priority is no longer assigned to the currently-selected reference.

This is usually appropriate when the application provides no means to influence the selection order externally. For example, in networks where SSM are not used, the selection would be based on clock availability as determined by the internal monitors. However, there are three situations when automatic selection based purely on internal monitoring would not be appropriate. In both cases, the internal monitoring would not detect the change in clock status and would not be able to re-order the priority.

The first situation would be if a line interface unit (LIU) or a framer automatically switched to an alternative clock if it detected a failed input signal (some framers or LIUs automatically switch to a crystal oscillator when they detect that the input has failed, so that the recovered clock output signal gets to be timed from the crystal instead of from the line); this results in the TDM Block receiving a clock signal which is not traceable to the synchronisation network, and is therefore not suitable for timing purposes, yet is behaving cleanly and cannot be rejected by the internal monitors. In this circumstance, some means has to be provided externally to the ACS9522 to detect that the recovered clock has been replaced and to modify the priority tables accordingly (a popular method is to monitor the LOS or LOF alarms and re-order the priority tables accordingly).

The second situation when internal monitoring is not sufficient is when an external flag is used to indicate the signal is not traceable: SSMs and AIS are examples because they indicate the quality of the source of timing. This can be an important consideration when prioritising input sources. This circumstance would also have to be handled externally to the ACS9522, with the AIS and/or the SSM values being used to decide the priority order.

The third situation is when the network equipment has to apply hold-off and wait-to-restore times before making a reference switch. While the activity monitors can be configured to implement a short hold-off time, they cannot meet the requirement for a long wait-to-restore time. These times are best implemented in host software, in conjunction with the priority-ordering and source-selection processes.

If the priority order is to be updated externally to the ACS9522, the priority tables of the TDM Block can either be updated, and a internal reference switch allowed to happen, or a forced selection can be made using the appropriate registers. For the T0 path, external code can apply a reference switch by writing the highest-priority reference source into the force_select_reference_source register. For the T4 path, this can be achieved using the cnfg_T4_path register.

Forced-selection can also be used for special circumstances, such as chip or board testing.

The restoration of repaired reference sources is handled carefully to avoid inadvertent disturbance of the output clock. The ACS9522 has two modes of operation to manage this:

- Revertive mode - available to both the T0 and the T4 path.
- Non-revertive mode - available on the T0 path only (can be applied in external software).

In revertive mode, the ACS9522 reverts to a re-validated source, if it has a higher priority than the currently-selected reference source.

In non-revertive mode, the ACS9522 does not revert to a re-validated source, even if it has a higher priority than the currently-selected reference source. Instead, the re-validation (using the internal monitors) of the reference source is flagged in the sts_sources_valid register. This sets the bit (appropriate to the input source) in the sts_interrupts register. The host software can then control when the re-validated source is available for selection. To make the reference switch happen automatically, the software must briefly select revertive mode. Alternatively, the switch can be made using the force_select_reference_source register.

A failure of the currently-selected reference always triggers a switch-over, regardless of whether revertive or non-revertive mode is active.

If a redundancy-protection scheme is being used, the standby device must always be ready to select the same input reference as the active device. Each ACS9522 device monitors its inputs locally, and the results are passed to the active device.

Specifically, the contents of the sts_sources_valid register of the standby device are written by host code into the cnfg_sts_remote_sources_valid register of the active device, and vice versa; this means that each device knows which sources are available to the other.

This feature protects against local failures within the network equipment (such as faulty connectors, failed tracks, etc); such failures could be unique to each device and may not otherwise be visible to external reference-selection code. Forced control selection

The force_select_reference_source register controls both the choice of automatic or forced selection, and the selection itself (when forced selection is required). In order to select automatic choice of source selection, the 4-bit value is set to all zeros or all ones. To force-select a particular input (SETS_I[n]), the bit value is set to n.

The force_select_reference_source register defaults to all ones on reset, causing automatic selection of the reference source to be the default setting.

Automatic selection control

Automatic selection of inputs is controlled by the priority values programmed into the *cnfg_ref_selection_priority* registers. These registers consist of seven, 8-bit registers organized as one 4-bit register per input reference port, two input reference ports per register. Each half of the register holds a 4-bit value which represents the desired priority of that particular reference port. The priority value of unused ports should be set to 0000, indicating that they are not to be included in the priority table. On power-up or after a reset, the entire configuration file defaults to defined values.

All selection priority values are relative to each other, with numbers of lower value taking higher priorities. Each reference source in use should be given a unique priority value between 1 to 15 (decimal).

If two or more inputs are given the same priority number, those inputs are selected on a first in, first out basis. Assume that the first of two same priority number sources becomes invalid. In this event the second source is switched in. If the first source becomes valid again, there will not be a switch. If a third source with the same priority number as the other two becomes valid, it joins the priority list on the same first in, first out basis.

There is no implied priority of sources based on their channel numbers. Switching between sources of the same priority value is not affected by the selection of revertive or non-revertive mode.

Input channel SETS_I11 is used in a special way in redundancy-protection configurations. If a device is acting in a standby role, input channel SETS_I11 must be connected to an output port that is carrying a T0 signal of the active device. This input is used to align the standby device's T0 outputs with those of the active device.

Ultra fast switching

Using the internal monitors, the loss of a reference source eventually causes the input to be considered invalid, triggering one of the interrupt inputs. The time taken to raise this interrupt depends on the leaky bucket configuration of the activity monitors (this can be used as a hold-off time). The fastest leaky bucket setting still takes a minimum of 128 ms to trigger the interrupt. If the failed input is one of the set of standby sources, this time is not important since the source is not driving the DPLL and so has no effect on the output. However, the situation is very different if it is the currently-selected source which has failed because loss-of-clock or erratic behavior on the currently-selected source could affect the output stability; for this reason it is useful to quickly isolate the currently-selected source while its failure is checked for consistency. The ACS9522 TDM Block contains a fast-detection mechanism for quickly detecting poor behavior of the currently-selected source and going immediately into holdover while the input is checked for consistency. This is described below.

A faster disqualification mechanism is provided for the currently selected reference source. This detector is triggered if the input clock is missing for approximately two clock cycles. This applies to both the T0 and the T4 path.

The registers can be configured such that this detector triggers one of the following actions:

- Raises a bit in the sts_interrupts register. This action is enabled or disabled by setting the *main_ref_failed* bit in the cnfg_interrupt_mask [15:8] register.
- Immediately disqualifies the current reference source. This action is enabled or disabled by writing to the *ultra_fast_switch* bit of the cnfg_monitors register.
- Raises a bit in the sts_interrupt register and immediately disqualifies the current reference source. This action is enabled or disabled by setting both the *main_ref_failed* bit and the *ultra_fast_switch* bit.

If the interrupt action is enabled, a missing input clock is flagged on the *main_ref_failed* bit in the sts_interrupts register. This bit is reset by writing to the sts_interrupts register in the normal way.

If the reference source disqualification option is enabled, a loss of the input clock for approximately two clock cycles causes the DPLL to switch to holdover mode. When the DPLL is in holdover mode it is isolated from further disturbances in the input clock.

If the input clock returns before the activity or frequency monitor rejection alarms have been raised, then the DPLL resumes locking to the input with little disturbance. In this scenario, the DPLL normally uses "nearest edge locking" mode (±180° capture) to re-lock to the input clock.

This avoids possible cycle slips or glitches that could be caused by trying to lock to an edge that is 360° away. Setting the *noact_ph_loss* bit of the cnfg_phase_loss_fine_limit register causes the DPLL to use ±360° capture when the input clock returns.

The *main_ref_failed* bit in the sts_interrupts register can be used to drive the TDOB pin in order to provide a fast hardware indication of failure of the selected reference source. This is useful in some applications. To enable or disable this feature, write to the *los_flag_on_ TDO* bit of the cnfg_monitors register. Once asserted, the pin then remains high until the interrupt is cleared.

NOTE: Using the TDOB signal on pin R17 to flag a reference source failure is not enabled by default.

Output clock phase continuity on source switchover

In order to ensure the device complies with the GR-1244-CORE[24] specification for stratum 3 for all input frequencies (maximum rate of phase change of 81 ns/1.326 ms), one of the following conditions must be true:

- Phase build out (PBO) is selected on (default).
- The DPLL frequency limit is set to less than ±30 ppm or (±9.2 ppm default).

NOTE: PBO is available on the T0 path only.

Modes of operation

The T0 path in the ACS9522 has three primary modes of operation (free-run, locked and holdover). There are also three temporary modes (pre-locked, lost-phase and pre-locked2). These modes are shown in Figure 22.

The ACS9522 can operate in forced or automatic control. On reset, the device reverts to automatic control, where transitions between states are controlled automatically. Forced control can be invoked by configuration, allowing transitions to be controlled externally. Forced control is not the normal mode of operation, but can be used for testing, or situations where a high degree of control over the state transitions is required.

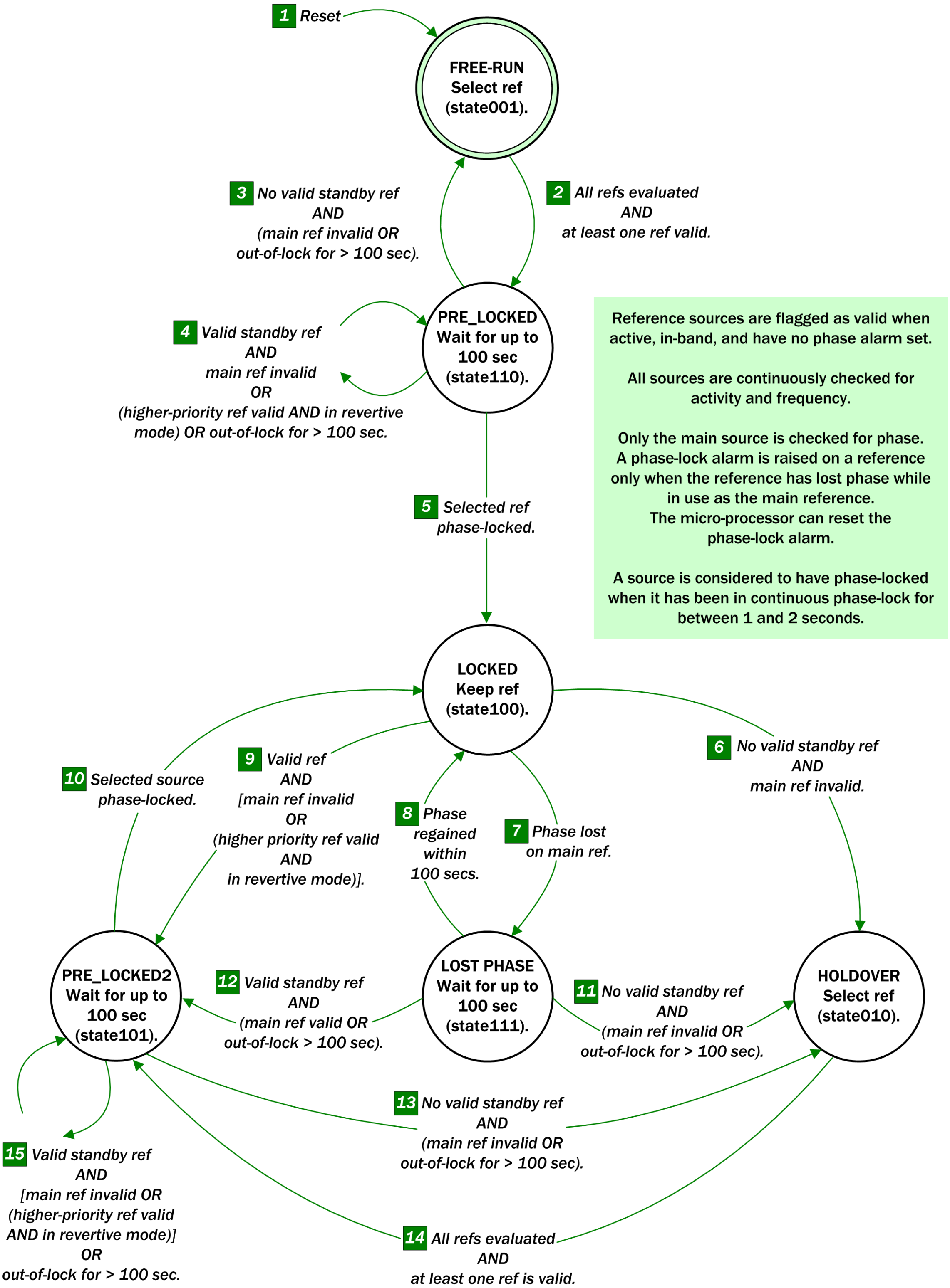

Figure 22 - Automatic mode control state diagram (T0 DPLL)

The state diagram above is for T0 DPLL only, and the 3-bit state value refers to the T0_DPLL_operating_mode bits in the sts_operating register. By contrast, the T4 DPLL has only automatic operation and can be in one of only two possible states: *instantaneous automatic holdover* with zero frequency offset (its start-up state), or *locked*. The T4 DPLL states are not configurable by the user and there is no *free-run* state.

Free-run mode

The device reverts to free-run mode after a power-on-reset, or a device reset. The device is not synchronized to the network in this mode. In free-run mode, the timing and synchronization signals generated from the ACS9522 are based on the reference clock frequency provided from the external oscillator, and are not synchronized to an input reference source. By default, the frequency of the output clock is a fixed multiple of the frequency of the external oscillator, and the accuracy of the output clock is equal to the accuracy of the oscillator. However the external oscillator frequency can be calibrated to improve its accuracy by a software calibration routine, using the cnfg_nominal_frequency [7:0] and cnfg_nominal_frequency [15:8] registers. For example a crystal with a 500 ppm offset could be made to look like one that is accurate to within ±0.02 ppm.

The transition from free-run to pre-locked occurs when the ACS9522 selects a reference source.

Pre-locked mode

In pre-locked mode, the device attempts to lock to the selected reference source. If the source is of good quality, the ACS9522 should enter the locked state after a short period. If lock is not achieved within 100 seconds, as defined by GR-1244-CORE[24] specification, the device reverts to free-run mode and another reference source is selected.

Locked mode

Locked mode is the normal operating state of the device. Locked mode can be entered from either pre-locked mode, pre-locked2 mode or phase-lost mode. Locked mode is achieved when an input reference source has been selected and the phase loss/lock detectors indicate that the DPLL has continuously remained in phase lock for at least one second (see Phase lock/loss detection). When the ACS9522 is in locked mode, the output frequency and phase track the selected input reference source.

Lost-phase mode

The device enters lost-phase mode whenever the phase loss/lock detectors indicate that the DPLL has lost phase lock (see Phase lock/loss detection). The DPLL still tries to lock to the input clock reference, if it exists. If lock is achieved within a short time, the device then re-enters locked mode.

However the current reference source is disqualified if one of the following conditions is true:

- The leaky bucket accumulator for the reference source is triggered.
- The device spends more than 100 seconds in lost-phase mode, causing a phase alarm to be raised.

If the current reference source is disqualified, one of the following transitions takes place:

- The device enters pre-locked2 mode, if a known good stand-by source is available.
- The device enters holdover mode if no stand-by sources are available.

Holdover mode

The device enters holdover mode if its currently selected input source becomes invalid, and no other valid replacement source is available. In this mode, the device controls its output frequency by using frequency data that was acquired and stored when the input reference source was still valid.

In holdover mode, the ACS9522 still provides the timing and synchronization signals to maintain the network element but is not phase locked to any input reference source.

Holdover mode can be configured to operate in either automatic mode or manual mode:

Automatic mode is selected by setting the *man_holdover* bit of the cnfg_input_mode register low.

Manual mode is selected by setting the *man_holdover* bit of the cnfg_input_mode register high.

Automatic holdover mode

In automatic holdover mode, the device can be configured to operate using either averaged or instantaneous frequency:

Averaged mode is selected by setting the *auto_ averaging* bit of the cnfg_holdover_modes register high.

Instantaneous mode is selected by setting the *auto_averaging* bit of the cnfg_holdover_modes register low.

Holdover using averaged frequency

In averaged mode the frequency reported by the *sts_current_DPLL_frequency* register, is internally filtered using an infinite impulse response filter.

This filter has two options:

- Fast response: giving a -3 dB filter response point corresponding to a period of approximately eight minutes.
- Slow response: giving a -3 dB filter response point corresponding to a period of approximately 110 minutes.

Fast response is selected by setting the *fast_averaging* bit of the cnfg_holdover_modes register high.

Slow response is selected by setting the *fast_averaging* bit of the cnfg_holdover_modes register low.

Holdover using instantaneous frequency

In instantaneous mode the DPLL freezes at the operating frequency it was using when it entered holdover mode. It does this by using only its internal DPLL integral path value (as reported in the sts_current_DPLL_frequency [7:0] register) to determine the output frequency. Because the integral path responds relatively slowly, it effectively averages the locked output frequency over a short time period that is inversely proportional to the DPLL bandwidth setting. The DPLL proportional path is not used, isolating the holdover frequency from any recent phase disturbances.

Manual holdover mode

In manual holdover mode the holdover frequency of the T0 DPLL is determined by the offset value programmed into the cnfg_holdover_frequency [7:0] register. This is a 19-bit signed number, with a LSB resolution of 0.0003068 ppm, giving an adjustment range of ±80 ppm. The value that is written to this register could be derived by reading the *sts_current_DPLL_frequency* register, which reports the current frequency offset of the DPLL in the same number format. This value is internally derived from the integral path of the DPLL, which effectively averages the current frequency over a short time period. The averaging period is inversely proportional to the locked loop bandwidth, which is selected by the cnfg_T0_DPLL_locked_bw register. Writing this value back to the *cnfg_holdover_frequency* register at regular intervals ensures that a recent averaged frequency value is already set when the device enters holdover mode.

It is possible to combine the internal averaging filters with some additional software filtering. For example the internal fast filter could be used as an anti-aliasing filter, and the software could further filter this value before determining the actual holdover frequency. To support this feature, a facility to read out the internally averaged frequency has been provided. Setting the *read_average* bit of the cnfg_holdover_modes register causes the *cnfg_holdover_frequency* register to return a filtered value when it is read. Clearly this results in the register returning different values to those that were written to it. The filtered value is available even if the device is not in holdover mode. The software could thus use the *cnfg_holdover_frequency* register as the source of frequency data rather than the *sts_current_DPLL_frequency* register.

An example using software averaging to eliminate temperature drift during holdover mode.

1. Select manual holdover mode by setting the *man_holdover* bit of the cnfg_input_mode register high.
2. Select fast holdover averaging mode by setting the *auto_averaging* and *fast_averaging* bits of the cnfg_holdover_modes register high.
3. Configure the cnfg_holdover_frequency [7:0]/cnfg_holdover_frequency [15:8] register to return a filtered value by setting the *read_average* bit of the cnfg_holdover_modes register high.
4. Configure the software to periodically read the averaged value from the cnfg_holdover_frequency [7:0]/ cnfg_holdover_frequency [15:8] register and the temperature from some external source. The software processes the frequency and temperature values and places the data in a software look-up table or other algorithm. The software then writes back an appropriate averaged value into the cnfg_holdover_frequency [7:0]/cnfg_holdover_frequency [15:8] register.

Once holdover mode is entered, the software periodically updates the cnfg_holdover_frequency [7:0]/cnfg_holdover_frequency [15:8] register using measured temperature information (not supplied by the ACS9522).

Mini-holdover mode

To smooth the transition between locked mode and holdover modes, a fast mechanism is provided to freeze the current DPLL frequency within one or two missing clock cycles. This transition is the mini-holdover mode, which operates rapidly and therefore prevents a failed input from disturbing the frequency of the DPLL.

There are four possible methods for determining the mini-holdover frequency. The method used is defined by setting the mini_holdover_mode bits of the cnfg_holdover_modes register.

Mini-holdover mode only prevails until one of the following occurs:

- A new source has been selected.
- The state machine enters holdover mode.
- The original input recovers from its fault.

External factors affecting holdover mode

ETSI ETS-300 462-54, Section 9.1, requires that the short-term phase error during switchover between locked and holdover modes be limited to an accumulation rate no greater than 0.05 ppm during a 15 second interval. The frequency accuracy of holdover mode also has to meet the ITU-T, ETSI and Telcordia performance requirements.

The frequency stability of the external oscillator clock is critical in this mode, as the stability and accuracy of the output frequency directly depend on it. Steps should be taken to shield the external TCXO/OCXO from fast temperature fluctuations and any other influences that might affect its stability.

Pre-locked2 mode

Pre-locked2 mode is very similar to pre-locked mode. It is entered from holdover mode when an input reference source has been selected and applied to the phase locked loop. It is also entered if the device is operating in revertive mode and a higher-priority reference source is restored.

Upon applying a reference source to the phase locked loop, the ACS9522 should enter the locked state in a maximum of 100 seconds if the selected reference source is of good quality, as defined by GR-1244-CORE19 specification. If the device cannot achieve lock within 100 seconds, it reverts to holdover mode and another reference source is selected.

DPLL architecture and configuration

A digital PLL gives a stable and consistent level of performance and can be easily programmed for different dynamic behavior or operating range. It is not affected by operating conditions or silicon process variations. Digital synthesis is used to generate all the required SONET/SDH output frequencies. The digital logic operates at 204.8 MHz, which is generated by multiplying the reference clock from the oscillator module. Hence the best time resolution for the output signals from the DPLL is one 204.8 MHz cycle or 4.9 ns.

The output of the DPLL can be passed through an analog PLL to provide further resolution and reduce the jitter on the final output. The bandwidth of this APLL is set four orders of magnitude higher than the bandwidth of the DPLL, which means that the overall response is set by the DPLL. This APLL reduces the 4.9 ns p-p jitter from the DPLL to typical values of 500 ps p-p and 60 ps RMS at the final outputs. These values are measured broadband, from 10 Hz to 1 GHz. This arrangement combines the flexibility and repeatability of a DPLL with the low jitter of an APLL.

The DPLLs in the ACS9522 are extremely programmable. All of the following PLL parameters can be programmed:

- Bandwidth (from 0.1 Hz up to 70 Hz).
- Damping factor (from 1.2 to 20).
- Frequency acceptance and output range (from 0 to 80 ppm, typically 9.2 ppm).
- Input frequency (12 common SONET/SDH spot frequencies).
- Input-to-output phase offset (in 6 ps steps up to 200 ns).

There is no requirement to understand the loop filter equations or detailed gain parameters, since all the high level factors (such as overall bandwidth) can be set directly via registers in the serial interface. No critical external components are required for either the internal DPLLs or APLLs. This provides another key advantage over traditional discrete designs.

The T4 DPLL is similar in structure to the T0 DPLL, but its bandwidth is limited to the high end. It also does not incorporate many of the phase build-out and adjustment facilities of the T0 DPLL. This is because the T4 DPLL is only intended to provide clock synthesis and input to output frequency translation functions. These operations have no defined requirement for jitter attenuation or input phase jump absorption.

T0 DPLL main features

- Two programmable DPLL bandwidth controls (locked and acquisition bandwidth), each with 10 steps from 0.1 Hz to 70 Hz.
- Programmable damping factor, for optional faster locking and peaking control. Factors = 1.2, 2.5, 5, 10 or 20.
- Multiple phase lock detectors.
- Input to output phase offset adjustment (master/slave), ±200 ns, 6 ps resolution step size.
- PBO phase offset on source switching - disturbance down to ±5 ns.
- Multi-cycle phase detection and locking, programmable up to ±8192 UI - improves jitter tolerance in direct lock mode.
- Holdover frequency averaging with a choice of averaging times: 8 minutes or 110 minutes.
- Multiple E1 and DS1 outputs supported.

T4 DPLL main features

- A single programmable DPLL bandwidth control: 18 Hz, 35 Hz, or 70 Hz.
- Programmable damping factor, for optional faster locking and peaking control. Factors = 1.2, 2.5, 5, 10 or 20.
- Multiple phase lock detectors.
- Multi-cycle phase detection and locking, programmable up to ±8192 UI - improves jitter tolerance in direct lock mode.
- DS3/E3 support (44.736 MHz / 34.368 MHz) at same time as OC-N rates from T0.
- Low jitter E1/DS1 options at same time as OC-N rates from T0.
- Frequencies of n x E1/DS1 including 16 and 12 x E1, and 16 and 24 x DS1 supported.
- Can use the phase detector in T4 DPLL to measure the input phase difference between two inputs.

The structures of the T0 and T4 PLLs are shown in the PLL block diagram and in the section Output clock paths. This section also details how the DPLLs, and particular output frequencies, are configured. The following sections detail some component parts of the DPLL.

T0 DPLL automatic bandwidth controls

If the T0 DPLL is attempting to lock to a newly selected input, a wide bandwidth is normally desirable to reduce the locking time. Once the DPLL is locked, a narrower bandwidth is preferred as this reduces wander on the output (See the section Output jitter and wander). The ACS9522 allows the DPLL bandwidth to be automatically changed depending on the DPLL state. The bandwidth can also be set manually, if desired.

Automatic bandwidth selection mode is enabled or disabled by setting the *auto_BW_sel* bit in the cnfg_auto_bw_sel register. If this mode is selected, the T0 DPLL bandwidth setting is automatically switched between the acquisition bandwidth and the locked bandwidth configurations. These configurations are programmed in the cnfg_T0_DPLL_acq_bw and cnfg_T0_DPLL_locked_bw registers respectively.

If automatic bandwidth selection mode is not selected, the DPLL always uses the bandwidth set in the cnfg_T0_DPLL_locked_bw register, regardless of the state of the DPLL.

Phase and frequency detectors

The input of each DPLL uses a phase and frequency detector (PFD) to compare the input and feedback clocks. On the T0 path this PFD operates at input frequencies up to 77.76 MHz.

In direct lock mode, the whole DPLL can operate at spot frequencies between 2 kHz and 77.76 MHz. The special input frequency of 155.52 MHz can also be used by dividing its frequency to 77.76 MHz before it reaches the DPLL (see Direct lock mode).

In lock8k mode, all input frequencies are internally divided down to 8 kHz before they reach the DPLL (see Lock8K mode). Direct lock mode may produce marginally better maximum time interval error (MTIE) figures than lock8k mode, because the phase error measurement is performed more frequently. This direct locking capability is one of the unique features of the ACS9522.

A patented multi-phase detector is used to produce an infinitesimally small input phase resolution, combined with large jitter tolerance. The following phase detectors are used:

- Phase and frequency detector (±360° or ±180° range).
- An early/late phase detector for fine resolution.
- A multi-cycle phase detector for large input jitter tolerance. This captures, and remembers, phase differences between the input and feedback clocks over many cycles (up to 8191 UI).

The phase detectors in each path can either use nearest edge detection (±180° capture), or ±360° phase capture range. The ±360° capture range provides frequency locking as well as phase locking. However it may cause an unnecessary phase shift of ±360°.

Normally the device uses a ±180° capture range when initially locking to a new reference source. if lock is not achieved within 2 seconds, it automatically switches to a ±360° capture range. Nearest edge locking can be disabled by setting the *disable_180* bit of test_register1 to 1. This may reduce the time taken to lock to a new reference source by up to two seconds.

The device automatically switches to nearest edge detection when both the following conditions are true:

- The multi-UI phase detector is not enabled.
- The other phase detectors have detected that phase lock has been achieved.

The balance of usage between the phase and frequency detector and the early/late phase detector can be adjusted using registers cnfg_T4_DPLL_damping, cnfg_T0_DPLL_damping, cnfg_T4_DPLL_PD2_gain, and cnfg_T0_DPLL_PD2_gain.

The default settings of these registers should be sufficient for all modes. Adjusting these settings only affects small-signal overshoot and bandwidth.

The multi-cycle phase detector is enabled by setting the *wide_range_en* bit of the cnfg_phase_loss_coarse_limit register to 1. The range of the detector is set by programming the *phase_loss_coarse_limit* bits of the cnfg_phase_loss_coarse_limit register. When this detector is enabled it tracks phase errors over many input clock periods, giving excellent jitter tolerance. The multi-cycle phase detector provides an alternative to using lock8k mode, when high jitter tolerance is required.

Setting the *multi_ph_resp* bit of the cnfg_phase_loss_coarse_limit register to 1 enables the phase result from the multi-phase detector to be used in the DPLL algorithm. This gives a faster pull-in characteristic, but more overshoot. The characteristics of the loop in this configuration are similar to lock8k mode. Setting the bit to 0 limits the phase detector to ±360 degrees. This gives a slower pull-in characteristic, but with less overshoot. In both cases the multi-cycle phase detector tracks, and remembers, the final phase position that the loop has to lock to.

Phase lock/loss detection

There are several possible ways that phase lock or phase loss can be detected. Any of the following can indicate a phase loss condition:

- The fine phase lock detector, which measures the phase between the input and feedback clocks.
- The coarse phase lock detector, which monitors whole cycle slips.
- Detection that the DPLL is at its minimum or maximum frequency.
- Detection of no activity on the input.

These sources of phase loss indication can be individually enabled or disabled by setting bits in registers cnfg_phase_loss_fine_limit, cnfg_phase_loss_coarse_limit and cnfg_DPLL_soft_limit.

The phase lock / loss indication is used by the device to automatically switch between normal and nearest edge locking, and between acquisition or normal bandwidth settings of the DPLL, if these features are enabled.

The coarse phase lock detector detects phase differences of n cycles between the input and feedback clocks. The value of n is set by the *phase_loss_coarse_limit* bits of the cnfg_phase_loss_coarse_limit register. This same register is used to alter the coarse phase detector range, since these functions are related. The coarse phase lock detector is used in situations where an amount of input jitter needs to be tolerated without triggering a phase loss indication. The fine phase loss detector should be disabled if the coarse detector is enabled.

Damping factor programmability

The default settings of DPLL damping factor provide a maximum wander-gain peak of approximately 0.1 dB. Several standards specify a wander transfer gain of less than 0.2 dB (e.g. GR-1244-CORE[24], G.812[14] and G.813[15]). The GR-253[22] standard specifies jitter (not wander) transfer of less than 0.1 dB.

In order to accommodate different required levels of transfer gain, the ACS9522 provides a choice of damping factors. More choices of damping factor are provided at higher frequencies because these frequencies are classified as jitter.

Available damping factors for different DPLL bandwidths, together with the associated jitter peak values shows the damping factors that are available for selection at the different bandwidth settings, together with corresponding approximate gain peak values.

Table 38 Available damping factors for different DPLL bandwidths, together with the associated jitter peak values

Bandwidth	cnfg_T0_DPLL_damping bits [2:0]	Damping factor selected	Gain peak/dB
0.1 Hz to 4 Hz	1, 2, 3, 4, 5	5	0.1
8 Hz	1	2.5	0.2
	2, 3, 4, 5	5	0.1
18 Hz	1	1.2	0.4
	2	2.5	0.2
	3, 4, 5	5	0.1
35 Hz	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4,5	10	0.06
70 Hz	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4	10	0.06
	5	20	0.03

Local oscillator frequency calibration

The absolute accuracy of the local oscillator frequency is less important than its stability, since frequency offset can be compensated by adjustment of register values. An adjustment range of ±50 ppm should be sufficient to cope with most crystals and in fact the adjustment range provided is an order of magnitude larger than this. The cnfg_nominal_frequency [7:0] and cnfg_nominal_frequency [15:8] registers are used to make this adjustment. Increasing the value held in these registers by one LSB step increases the output frequencies by 0.0196229 ppm.

The default register value (in decimal) = 39321 (9999 hex), which corresponds to 0 ppm offset. The minimum to maximum offset range of the register is 0 to 65535 dec, giving an adjustment range of -771 ppm to +514 ppm of the output frequencies, in 0.0196229 ppm steps.

Example: Assume the desired local oscillator frequency is 12.800 MHz but the actual local oscillator frequency is 5 ppm higher than this. In order to calibrate the local oscillator, and remove this error, the following value must be programmed into the register:

39321 - (5/0.0196229) = 39066 (dec) = 989A (hex).

Output jitter and wander

Wander and jitter present on the output clocks are dependent on:

- The magnitudes of wander and jitter on the selected input reference clock (in locked mode)
- The internal wander and jitter transfer characteristic (in locked mode)
- The jitter on the local oscillator clock (in holdover mode)
- The wander on the local oscillator clock (in holdover mode).

Wander and jitter are treated in different ways to reflect their differing impacts on network design. Jitter is always strongly attenuated, while wander attenuation can be varied to suit the application and operating state. Wander and jitter attenuation is achieved by changing the bandwidth of the DPLL. This gives a transfer characteristic of a low pass filter, with a programmable pole. It is sometimes necessary to change the filter dynamics to suit particular circumstances. For example, when locking to a new source, the filter bandwidth can be opened up to reduce the locking time. Once locked, the bandwidth can be tightened up again to remove wander from the signal. This bandwidth change for locking and for acquisition is handled automatically within the ACS9522 (see T0 DPLL automatic bandwidth controls).

There may be a phase shift between the selected input reference source and the output clock that increases over time. This is mainly caused by frequency wander in the external oscillator module. This phase shift is characterized using two parameters, MTIE and time deviation (TDEV). Higher stability XOs give better performance for MTIE. The oscillator becomes more critical when the DPLL bandwidth is near to, or below, 0.1 Hz, as the DPLL response may be too slow to track the changing oscillator frequency. Shielding the OCXO or TCXO from temperature variations can improve output wander performance.

MTIE and TDEV values are specified in all relevant specifications. The acceptable limits are different in each specification.

Typical MTIE and TDEV measurement values for the ACS9522 are shown in Figure 23 for locked mode operation. Figure 24 shows a typical measurement of phase error accumulation in holdover mode operation.

The required performance for phase variation in holdover mode is specified in different ways in each specification (see References and related standards).

For example:

1 ETSI ETS-300 462-5[5], Section 9.1, requires that the short-term phase error during switchover (i.e. locked to holdover to locked) be limited to an accumulation rate no greater than 0.05 ppm during a 15 second interval.

2 ETSI ETS-300 462-5[5], Section 9.2, requires that the long-term phase error in holdover mode should not exceed

{(a1 + a2)S + 0.5bS2 + c}

where:

a1 = 50 ns/s (allowance for initial frequency offset)

a2 = 2000 ns/s (allowance for temperature variation)

b = 1.16x10-4 ns/s2 (allowance for ageing)

c = 120 ns (allowance for entry into Holdover mode).

S = Elapsed time (s) after loss of external ref. input

3 ANSI Tin1.101-1999[2], Section 8.2.2, requires that the phase variation be limited so that no more than 255 slips (of 125 µs each) occur during the first day of holdover. This requires a frequency accuracy better than:

((24x60x60)+(255x125µs))/(24x60x60) = 0.37 ppm

Temperature variation is only restricted to the normal bounds of 0 to 50°C.

4 Telcordia GR-1244-CORE[24], Section 5.2, shows that an initial frequency offset of 50 ppb is permitted on entering holdover mode, while a drift over temperature of 280 ppb is allowed. An allowance of 40 ppb is permitted for all other effects.

5 ITU G.822[16], section 2.6, requires that the slip rate during category (b) operation (interpreted as being applicable to holdover mode operation) be limited to less than 30 slips (of 125 µs each) per hour.

((60 x 60) + (30 x 125 µs))/(60 x 60)) = 1.042 ppm

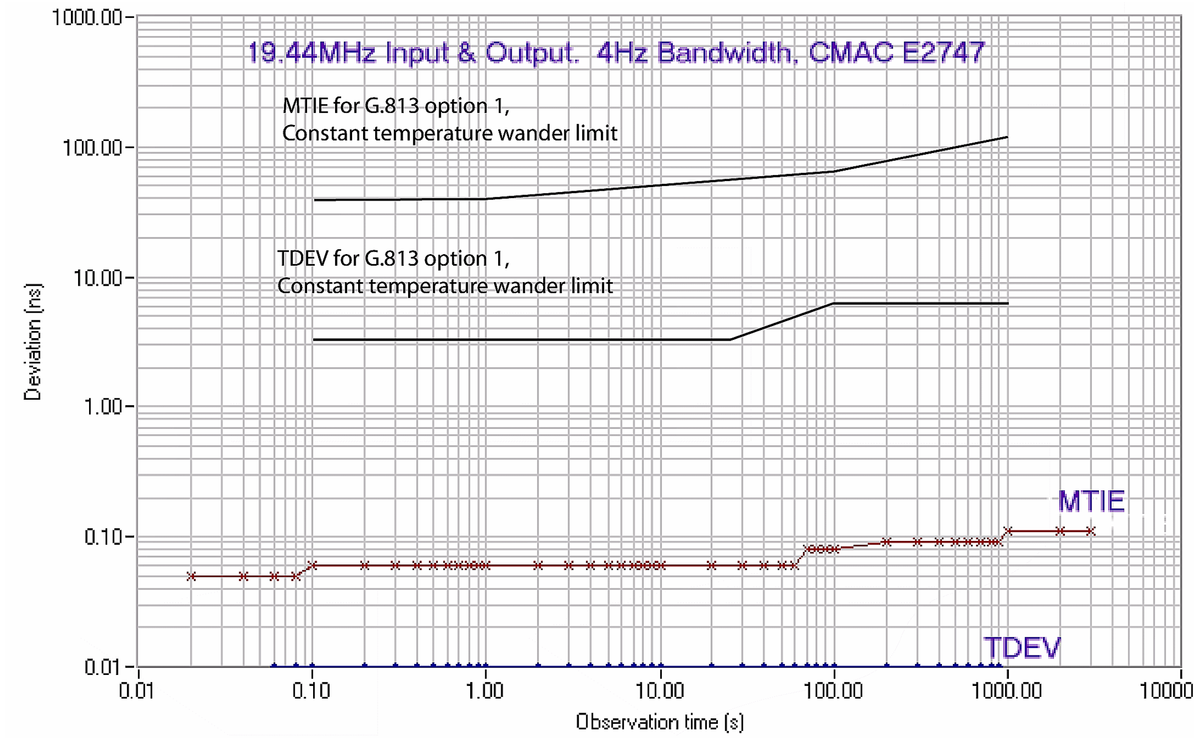

Figure 23 - Maximum time interval error (MTIE) and time deviation (TDEV) of T0 DPLL output port

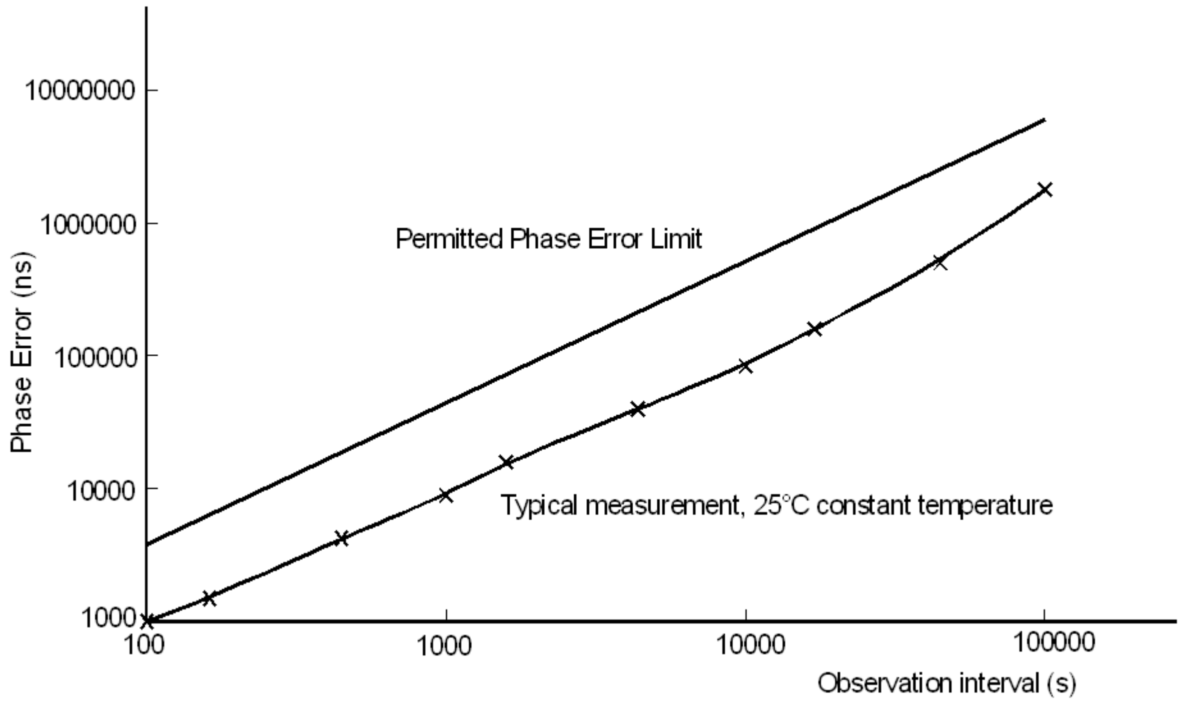

Figure 24 - Phase error accumulation of T0 PLL output port in holdover mode

Jitter and wander transfer

The ACS9522 has a programmable jitter and wander transfer characteristic, which is set by the DPLL bandwidth. The -3 dB jitter transfer attenuation point can be set in the range 0.1 Hz to 70 Hz, in 10 steps. The wander and jitter transfer characteristic is shown in Figure 25. Wander on the local oscillator clock does not have a significant effect on the output clock while in locked mode, provided that the DPLL bandwidth is set high enough so the DPLL can compensate quickly for any frequency changes in the crystal.

In free-run or holdover mode, wander on the crystal is more significant. Variation in crystal temperature or supply voltage, and ageing, can all cause drifts in operating frequency. These effects must be limited by careful selection of a suitable component for the local oscillator.

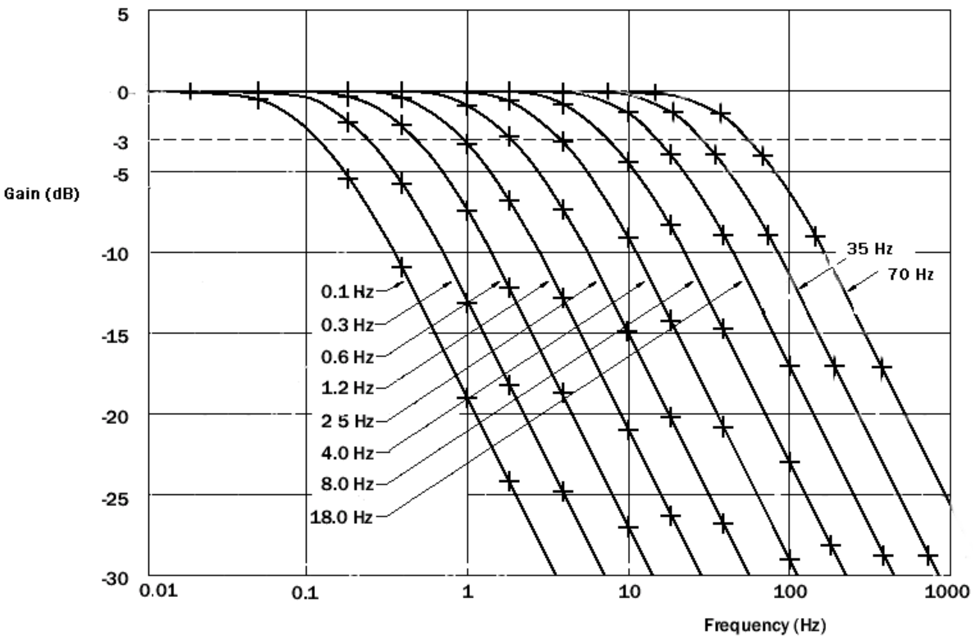

Figure 25 - Sample of measured wander and jitter transfer

Phase build-out

The phase build-out (PBO) feature is provided to minimize phase transients on the output SEC clock during input reference switching. If the currently selected input reference clock source is lost (due to a short interruption, out of frequency detection, or complete loss of reference) the next highest priority reference source is selected, and a PBO event is triggered. PBO is available on the T0 DPLL only.

ITU-T G.813[15] specifies the following conditions for a switch from one clock source to another via holdover mode:

- The maximum allowable short-term phase transient response is 1 µs over a 15 second interval.
- The maximum phase transient, or jump, is less than 120 ns, with a rate of change of less than 7.5 ppm.
- The performance should be better than 0.05 ppm.

The ACS9522 performs substantially better than these requirements. The typical phase disturbance on clock reference source switching is less than 5 ns on the ACS9522.

When a PBO event is triggered, the device enters a temporary holdover state. When in this temporary state, the phase of the input reference is measured, relative to the output. The device then automatically compensates for any measured phase difference by adding the appropriate phase offset into the DPLL. Following a PBO event the output phase transient is minimized to be no greater than 5 ns, whatever the phase difference between the inputs.

PBO is enabled or disabled by setting the *PBO_en* bit of the cnfg_monitors register. By default, it is enabled.

If PBO is enabled, it can be frozen at the current offset setting by setting the *PBO_freeze* bit of the cnfg_monitors register.

The device then ignores any further PBO events occurring on subsequent reference switches, and maintains the current phase offset. If PBO is disabled while the device is in locked mode, there may be a phase shift on the output SEC clocks as the DPLL locks back to 0 degrees phase error. The rate of phase shift depends on the programmed bandwidth of the DPLL. Enabling PBO while in the locked stated also triggers a PBO event.

PBO phase offset

In order to minimize the systematic (average) phase error for PBO, a PBO phase offset can be programmed in the cnfg_PBO_phase_offset register, in 0.101 ns steps. The range of the programmable PBO phase offset is restricted to ±1.4 ns. This feature can be used to eliminate an accumulation of phase shifts in one direction.

Input to output phase adjustment

When PBO is off, the system always tries to align the outputs to the inputs with 0° phase shift. However a mechanism is provided in the ACS9522 which allows precise fine tuning of the output phase position with respect to the input. This can be used to compensate for circuit and wiring delays. The output phase can be adjusted in 6 ps steps over the range ±200 ns. The phase adjustment actually changes the phase position of the feedback clock, so that the DPLL adjusts the output clock phases to compensate. The cnfg_phase_offset [7:0] and cnfg_phase_offset [15:8] registers control the output phase. The value programmed into these registers is only used when phase build-out is disabled.

The rate of change of phase is related to the DPLL bandwidth. For the DPLL to track large instant changes in phase, either lock8k mode should be on, or the coarse phase detector should be enabled.

Input wander and jitter tolerance

The ACS9522 complies with all relevant standards; principally ITU recommendation G.825[19], ANSI DS1.101-1999[2], Telcordia GR1244[24], GR253[22], G812[14], G813[15] and ETS 300 462-5 (1997)[5].

All reference clock inputs have a tight frequency tolerance but a generous jitter tolerance. Pull-in, hold-in and pull-out ranges are specified in Input reference source jitter tolerance. Minimum jitter tolerance masks are specified in Figure 26, Figure 27, Table 39 and Table 41.

The ACS9522 tolerates wander and jitter components that are greater than those shown in Figure 26 and Figure 27. The limit is determined by a combination of the apparent long-term frequency offset caused by wander, and the eye-closure caused by jitter. The input source is rejected if the frequency offset pushes the frequency outside the hold-in range for a long enough time to trigger one of the monitors. The signal is also rejected if the eye closes sufficiently to potentially affect data integrity.

Either lock8k mode, or one of the extended phase capture ranges, should be engaged for high jitter tolerance.

Table 39 Input reference source jitter tolerance

Jitter tolerance	Frequency monitor acceptance range	Frequency acceptance range (pull-in)	Frequency acceptance range (hold-in)	Frequency acceptance range (pull-out)
G.703[8]	±16.6 ppm	±4.6 ppm [1] ±9.2 ppm [2]	±4.6 ppm[1] ±9.2 ppm[2]	±4.6 ppm[1] ±9.2 ppm[2]
G.783[11]				
G.823[17]				
GR-1244-CORE[24]				

1. The frequency acceptance and generation range are ±4.6 ppm around the required frequency when the local oscillator frequency accuracy is within a tolerance of ±4.6 ppm.
2. The fundamental acceptance range and generation range is ±9.2 ppm with an exact local oscillator frequency of 12.800 MHz. This is the default DPLL range. The range is also programmable from 0 to 80 ppm in 0.08 ppm steps.

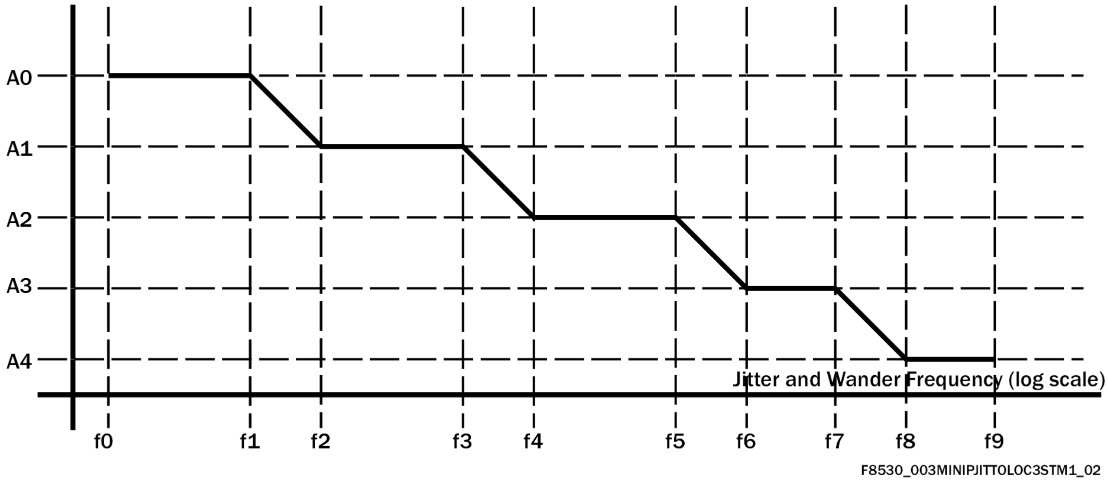

Figure 26 - Minimum input jitter tolerance (OC-3/STM-1)

Table 40 Amplitude and frequency values for jitter tolerance (OC-3/STM-1)

STM level	Peak-to-peak amplitude (unit interval)					Frequency (Hz)									
	A0	A1	A2	A3	A4	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9
STM-1	2800	311	39	1.5	0.15	12 u	178 u	1.6 m	15.6 m	0.125	19.3	500	6.5 k	65 k	1.3

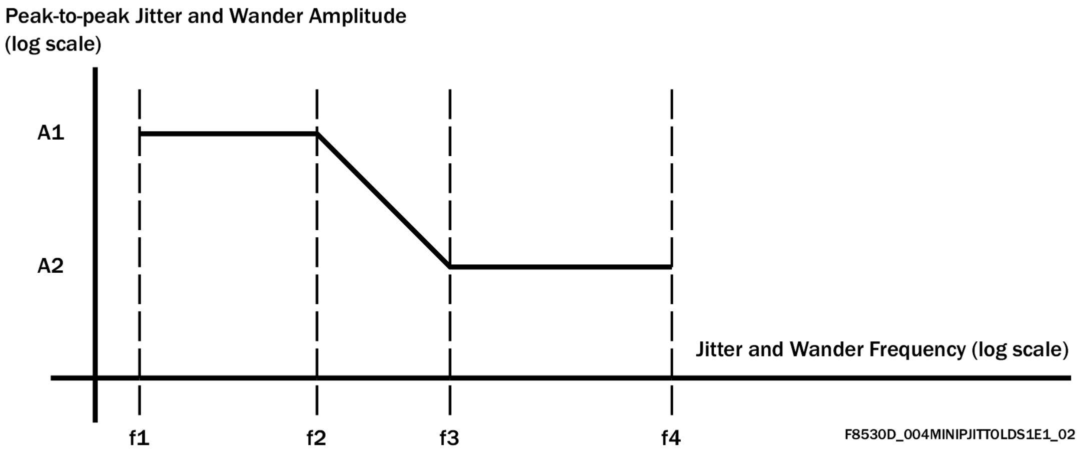

Figure 27 - Minimum input jitter tolerance (DS1/E1)

Table 41 Amplitude and frequency values for jitter tolerance (DS1/E1)

Type	Specification	Amplitude (UI p-p)		Frequency (Hz)			
		A1	A2	F1	F2	F3	F4
DS1	GR-1244-CORE[24]	5	0.1	10	500	8 k	40 k
E1	ITU G.823[17]	1.5	0.2	20	2.4 k	18 k	100

Using the DPLLs for accurate frequency and phase reporting

Frequency reporting

The frequency monitors in the ACS9522 perform frequency monitoring with a programmable acceptable limit of up to ±60.96 ppm. The resolution of the measurement is 3.8 ppm. The measured frequency can be read back from the sts_freq_measurement register, with channel selection being made by setting the *T4_T0_select* bit in the cnfg_registers_source_select register.

A more accurate measurement of both frequency and phase is possible by using the T0 and T4 DPLLs, and their phase detectors. The T0 DPLL is always monitoring the currently locked source. If the T4 path is not used, then the T4 DPLL can be used as a roving phase and frequency meter. It can be switched to monitor each input in turn, measuring both phase and frequency with a very fine resolution.

Registers sts_current_DPLL_frequency [7:0], sts_current_DPLL_frequency [15:8] and sts_current_DPLL_frequency [18:16] report the frequency of either the T0 DPLL, or T4 DPLL, with respect to the external crystal XO frequency. The external crystal frequency can be calibrated first, as described in Crystal frequency calibration.

The measured frequency value is a 19-bit signed number, with one LSB representing 0.0003068 ppm (range of ±80 ppm). This value is actually the integral path value in the DPLL, and is thus an averaged measurement of the input frequency. The averaging time is inversely proportional to the DPLL bandwidth setting. Reading this value at regular intervals effectively measures frequency wander on the currently locked source.

Phase reporting

Registers sts_current_phase [7:0] and sts_current_phase [15:8] report the phase of the input, as seen at the DPLL phase detector. One LSB of this value corresponds to approximately 0.7 degrees phase difference. A measurement made on T0 DPLL reports the phase difference between the input and the internal feedback clock.

The phase result is internally averaged or filtered with a -3 dB attenuation point at approximately 100 Hz. Selecting a low DPLL bandwidth allows the measurement of input phase wander in a frequency band of 0.1 Hz to 100 Hz, for example. This could be used in conjunction with external software to give a crude input MTIE measurement up to an observation period of approximately 1000 seconds. Selection between T4 or T0 DPLL is again made by setting the *T4_T0_select* bit in the cnfg_registers_source_select register.

In addition, the T4 DPLL phase detector can be used to make a phase measurement between two inputs. Set the *T4_meas_T0_ph* bit of the cnfg_T0_DPLL_frequency register to enable this feature. Setting this bit disables normal operation of the T4 path, and connects one input of the T4 phase detector to the current T0 input. The other phase detector input remains connected to the currently selected T4 input source. By forcing the T4 input source, a measurement can be made between the current T0 source and any other source.

This method could be used to measure the phase difference between the currently selected source and the stand-by source, or to measure the phase wander of each stand-by source with respect to the current source. An MTIE and TDEV calculation could be made for each input via external processing.

There are two methods that can be used to select the T4 source:

- Program the *T4_forced_reference_source* bits of the cnfg_T4_path register.
- Change the priority of T4 sources. To do this, set the *T4_T0_select* bit of the cnfg_registers_source_select register, and adjust the priority values contained in registers cnfg_ref_selection_priority (1 & 2) to cnfg_ref_selection_priority (13 & 14).

Output clock paths

The device supports two main output clock paths, T0 and T4, which are independent. The clock output pins can be individually assigned to either clock path as defined in Configure output frequency TO1 & TO2 register to Configure output frequency TO7 to TO11 register.

LVPECL/LVDS/AMI output port selection

The choice of LVPECL or LVDS compatibility of outputs is programmed using the cnfg_differential_outputs register.

The AMI output TO8 supports a composite clock. This consists of a 64 kHz AMI clock with 8 kHz boundaries marked by deliberate violations of the AMI coding rules. These rule violations follow the recommendations in ITU G.703[8].

The ACS9522 monitors this nominal pattern and may trigger a switch of input reference if departures are too frequent.

Output frequency selection and configuration

There are many options for generating output frequencies on the ACS9522. The device contains various circuit blocks that can be individually configured to adjust some of the output frequencies. There are also two main DPLL/APLL paths that can interact in various ways. Figure 28 shows an expanded view of the PLL paths within the device.

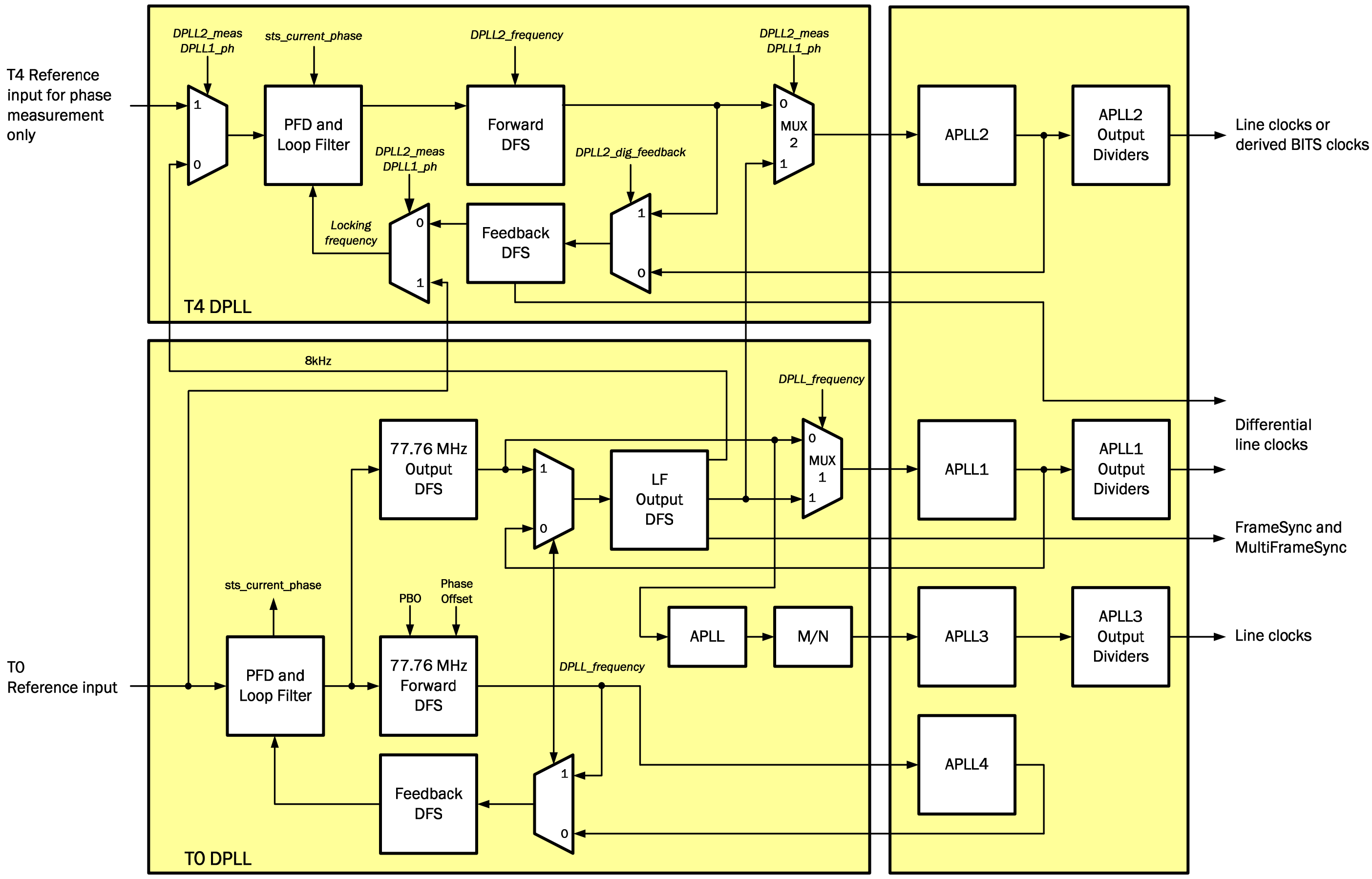

Figure 28 - PLL block diagram

T0 DPLL and APLLs

T0 input frequency, locking frequency and feedback frequency

The T0 DPLL always produces 77.76 MHz regardless of the input reference frequency or the locking frequency (the frequency at the input of the DPLL phase and frequency detector (PFD)). This means that the feedback signal is also 77.76 MHz. To allow operation with higher input frequencies, there is an optional pre-divider between the reference input and the first input to the PFD.

The feedback signal can also be raised or lowered in frequency. This is achieved by using dividers or digital frequency synthesis (DFS), before the feedback signal is fed to the second input to the PFD. In this way, the frequencies of the two inputs to the DFS are always matched but may be higher or lower than 77.76 MHz. Figure 29 illustrates the various frequencies in a simplified block diagram of the T0 DPLL circuit.

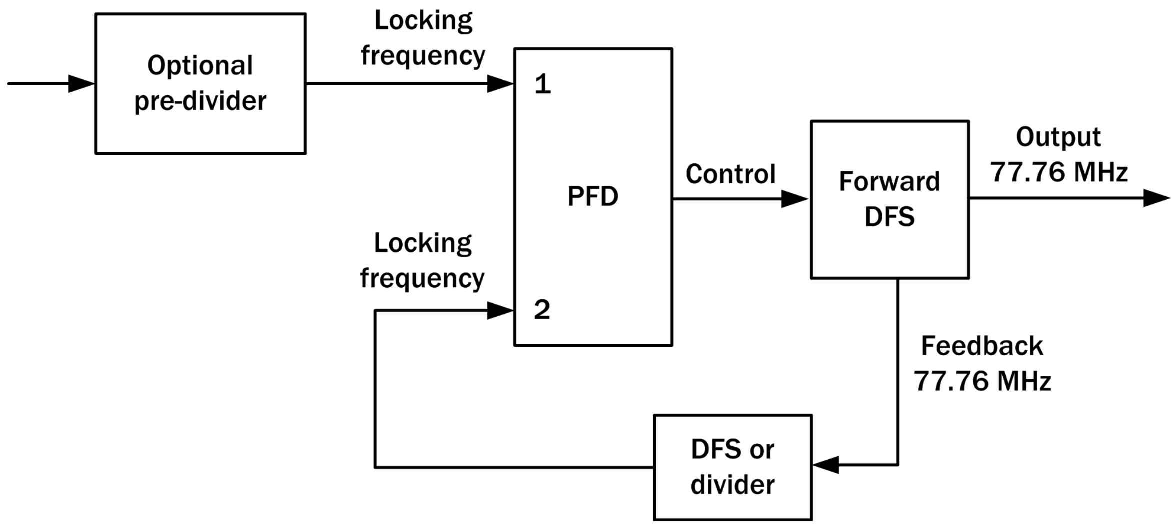

Figure 29 - T0 DPLL operating frequencies

T0 digital versus analog feedback

Digital frequency synthesis (DFS) generates an output frequency from a higher frequency system clock. However, the edges of the output clock are not evenly spaced as they align to the active edge of the system clock. This means that the generated clock frequency has an inherent jitter equivalent to one period of the system clock.

In the T0 path, the forward DFS generates 77.76 MHz from a 204.8 MHz system clock. The output jitter is therefore equal to one period of the 204.8 MHz clock, which is 4.9 ns peak-to-peak.

There is an option to use an APLL to filter out the jitter before the 77.76 MHz is used to generate the feedback locking frequency. Using the T0 feedback APLL in this way produces a lower jitter (<1 ns) feedback signal to give maximum performance. The digital feedback option is provided if the output path is switched to digital feedback, as it allows the two paths to remain synchronized.

T0 PBO and phase offset

The T0 77.76 MHz forward DFS block also handles phase build-out and any phase offset that is programmed into the device. The T0 77 MHz forward DFS and the T0 77 MHz output DFS blocks may therefore be offset in phase, even though they are locked in frequency.

T0 output DFS blocks

The T0 77 MHz output DFS block uses the 204.8 MHz system clock and always generates 77.76 MHz for the output clocks. This signal again has an inherent 4.9 ns of jitter. This 77.76 MHz signal is fed to another DFS block and to the T0 output APLL.

The low frequency T0 LF output DFS block is used to produce three frequencies. Two of these frequencies, Digital1 and Digital2, are available to be selected by any of the outputs TO1-TO7. The third frequency can produce multiple E1/DS1 rates via the filtering APLLs.

The input clock to the T0 LF output DFS block is either 77.76 MHz from the T0 output APLL, or 77.76 MHz directly from the T0 77 MHz output DFS. Routing the clock through the T0 output APLL produces lower jitter outputs from the T0 LF output DFS block. When the input to the T0 APLL is obtained from the T0 LF output DFS block, the input to that block comes directly from the T0 77M output DFS block so that a link to the input reference is maintained (see Figure 30).

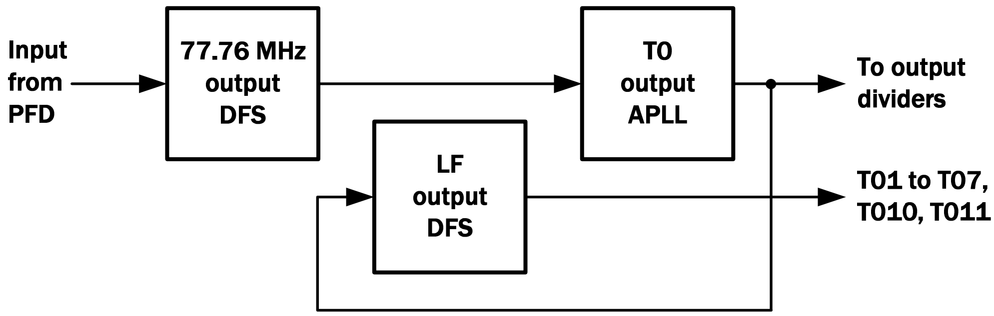

Figure 30 - T0 LF output DFS configured for low jitter outputs

T0 output APLL and output dividers

The input to the T0 output APLL can be either 77.76 MHz from the T0 77 MHz output DFS block, or an alternative frequency from the T0 LF output DFS block (offering 77.76 MHz, 12E1, 16E1, 24DS1 or 16DS1).

The output frequency from this APLL is four times its input frequency i.e. 311.04 MHz when used with a 77.76 MHz input. This output is subsequently divided by 1, 2, 4, 6, 8, 12, 16 and 48, and these divided frequencies are available at the T01-T07 outputs.

T4 DPLLs and APLLs

The T4 path is much simpler than the T0 path. This path offers no phase build-out or phase offset options. The T4 input can either be locked to a reference clock input, independently of the T0 path, or locked to the T0 path.

T4 forward DFS and feedback DFS

Unlike the T0 path, the T4 forward DFS block does not always generate 77.76 MHz. The possible frequencies generated by this DFS are listed in T4 APLL Frequencies. The output of the T4 forward DFS block is generated using DFS clocked by the 204.8 MHz system clock, and has an inherent jitter of 4.9 ns peak to peak.

The T4 feedback also has an optional APLL that can be used for filtering out the jitter. Again, this option produces the best performance.

T4 output APLL and dividers

The input to the T4 output APLL can come, either from the T4 forward DFS block, or from the T0 path.

The input to the T4 output APLL can be programmed to be one of the following:

- Output from the T4 forward DFS block (12E1, 24DS1, 16E1, 16DS1, E3, DS3, OC-N).
- 12E1 from T0.
- 16E1 from T0.
- 24DS1 from T0.
- 16DS1 from T0.

The frequency generated from the T4 output APLL block is four times its input frequency i.e. 311.04 MHz when used with a 77.76 MHz input. The output of this APLL is subsequently divided by 1, 2, 4, 6, 8, 12, 16 and 48, and these divided frequencies are available at the T01-T07 outputs.

Additional outputs

The TO8 and TO9 outputs can be driven from the T4 or the T0 path.

The TO10 and TO11 outputs are always generated from the T0 path.

2 kHz and 8 kHz clock outputs

8 kHz and 2 kHz frequencies are available on any of the TO1-TO7 outputs. See Table 47 (TO1 to TO7 output frequency selection) for the register settings to select these frequencies. The 8 kHz and 2 kHz frequencies can be generated from either the T0 path, or from the T4 path, by setting the *2k_8k_from_T4* bit in the cnfg_sync_pulses register.

All four of these outputs can be either clocks (with a 50:50 mark-space ratio) or pulses. They can also be inverted. When pulse outputs are selected, the pulse width is one cycle of the TO3 output. This means that TO3 must be configured to generate at least 1544 kHz to ensure that the pulses are generated correctly.

Figure 31 shows these various options being selected on an 8 kHz output or TO10, together with the required settings for the *8k_invert* and *8k_pulse* bits in the cnfg_sync_pulses register. The same options are provided for 2 kHz outputs or TO11 by setting the *2k_invert* and *2k_pulse* bits in the cnfg_sync_pulses register.

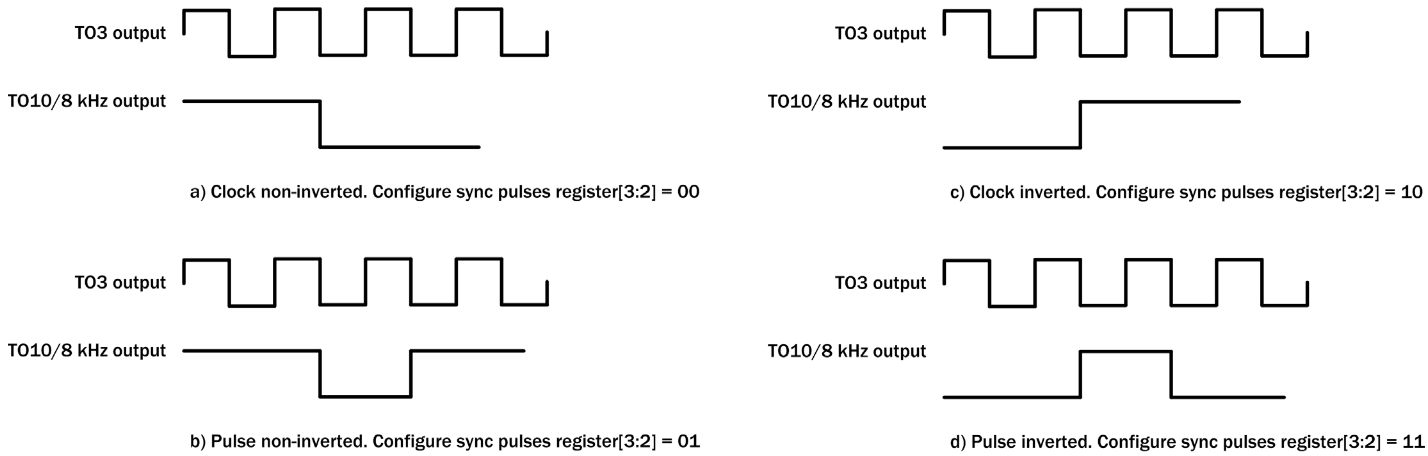

Figure 31 - Control of 8k options

Steps to configure the output frequencies

Perform the following steps to select the required output frequencies:

1 Decide if the application requires the use of the T4 path as an independent PLL path. If not, then the T4 path can be utilized to produce extra frequencies locked to the T0 path.

2 Refer to Table 44 to choose a set of output frequencies for each path, T4 and T0. Only one set of frequencies can be generated simultaneously from each path.

3 Refer to Table 44 to determine the required APLL frequency to support the frequency set.

4 Refer to Table 45 and Table 46 to determine how to configure the T0 and T4 paths. The required level of output jitter must be considered when making this decision.

5 Refer to Table 47 and the column headings in Table 44 to select the appropriate frequency from either of the APLLs on each output as required.

6 Set up SETS output selector to route the SETS function outputs to the DPSync outputs.

Jitter performance

Output jitter generation measured over 60 second interval, UI p-p max measured using DAPU 12.800 MHz TCXO on ICT Flexacom tester.

Table 42 Output jitter generation

Test definition		Conditions			Jitter spec	Device jitter
Specification	Filter	Bandwidth	I/P freq	Lock mode	UI	UI (typical)
G813[15] for 155 MHz o/p option 1.	65 kHz to 1.3 MHz	4 Hz	19.44 MHz	Direct lock	0.1 p-p	0.067 p-p
				8k lock		0.065 p-p
G813[15] & G812[10] for 2.048 MHz option 1.	20 Hz to 100 kHz	4 Hz	2.048 MHz	8k lock	0.05 p-p	0.012 p-p
G813[15] for 155 MHz o/p option 2.	12 kHz to 1.3 MHz	18 Hz	19.44 MHz	Direct lock/ 8k lock	0.1 p-p	0.072 p-p
	12 kHz to 1.3 MHz	8 Hz	19.44 MHz	Direct lock/ 8k lock	0.1 p-p	0.072 p-p
	12 kHz to 1.3 MHz	4 Hz	19.44 MHz	Direct lock/ 8k lock	0.1 p-p	0.078 p-p
	12 kHz to 1.3 MHz	2.5 Hz	19.44 MHz	Direct lock/ 8k lock	0.1 p-p	0.078 p-p
	12 kHz to 1.3 MHz	1.2 Hz	19.44 MHz	Direct lock/ 8k lock	0.1 p-p	0.078 p-p
	12 kHz to 1.3 MHz	0.6 Hz	19.44 MHz	Direct lock/ 8k lock	0.1 p-p	0.076 p-p
G812[14] for 1.544 MHz o/p.	10 Hz to 40 kHz	4 Hz	1.544 MHz	8k lock	0.05 p-p	0.006 p-p
G812[14] for 155 MHz electrical.	500 Hz to 1.3 MHz	4 Hz	19.44 MHz	8k lock	0.5 p-p	0.118 p-p
G812[14] for 155 MHz electrical.	65 kHz to 1.3 MHz	4 Hz	19.44 MHz	8k lock	0.075 p-p	0.065 p-p
ETS-300-462-3[4] for 2.048 MHz SEC o/p.	20 Hz to 100 kHz	4 Hz	2.048 MHz	8k lock	0.5 p-p	0.012 p-p
ETS-300-462-3[4] for 2.048 MHz SEC o/p.	49 Hz to 100 kHz	4 Hz	2.048 MHz	8k lock	0.2 p-p	0.012 p-p
ETS-300-462-3[4] for 2.048 MHz SSU o/p.	20 Hz to 100 kHz	4 Hz	2.048 MHz	8k lock	0.05 p-p	0.012 p-p
ETS-300-462-5[4] for 155 MHz o/p.	500 Hz to 1.3 MHz	4 Hz	19.44 MHz	8k lock	0.5 p-p	0.118 p-p
ETS-300-462-5[4] for 155 MHz o/p.	65 kHz to 1.3 MHz	4 Hz	19.44 MHz	8k lock	0.1 p-p	0.067 p-p
GR-253-CORE[22] net i/f, 51.84 MHz o/p.	100 Hz to 0.4 MHz	4 Hz	19.44 MHz	8k lock	1.5 p-p	0.027 p-p
GR-253-CORE[22] net i/f, 51.84 MHz o/p.	20 kHz to 0.4 MHz	4 Hz	19.44 MHz	8k lock	0.15 p-p	0.017 p-p
GR-253-CORE[22] net i/f, 155 MHz o/p.	500 Hz to 1.3 MHz	4 Hz	19.44 MHz	8k lock	1.5 p-p	0.118 p-p
GR-253-CORE[22] net i/f, 155 MHz o/p.	65 kHz to 1.3 MHz	4 Hz	19.44 MHz	8k lock	0.15 p-p	0.067 p-p
GR-253-CORE[22]cat II elect i/f, 155 MHz.	12 kHz to 1.3 MHz	4 Hz	19.44 MHz	8k lock	0.1 p-p	0.076 p-p
					0.01 rms	0.006 rms
GR-253-CORE[22] cat II elect i/f, 51.84 MHz.	12 kHz to 400 kHz	4 Hz	19.44 MHz	8k lock	0.1 p-p	0.018 p-p
					0.01 rms	0.003 rms
GR-253-CORE[22] DS1 i/f, 1.544 MHz.	10 Hz to 40 kHz	4 Hz	1.544 MHz	8k lock	0.1 p-p	0.001 p-p
					0.01 rms	<0.001 rms

Table 42 Output jitter generation

Test definition		Conditions			Jitter spec	Device jitter
Specification	Filter	Bandwidth	I/P freq	Lock mode	UI	UI (typical)
AT&T 62411[3] for 1.544 MHz.	10 Hz to 8 kHz	4 Hz	1.544 MHz	8k lock	0.02 rms	<0.001 rms
AT&T 62411[3] for 1.544 MHz.	8 Hz to 40 kHz	4 Hz	1.544 MHz	8k lock	0.025 rms	<0.001 rms
AT&T 62411[3] for 1.544 MHz.	10 Hz to 40 kHz	4 Hz	1.544 MHz	8k lock	0.025 rms	<0.001 rms
AT&T 62411[3] for 1.544 MHz.	Broadband	4 Hz	1.544 MHz	8k lock	0.05 rms	<0.001 rms
G-742[10] for 2.048 MHz.	DC to 100 kHz	4 Hz	2.048 MHz	8k lock	0.25 rms	0.012 rms
G-742[10] for 2.048MHz.	18 kHz to 100 kHz	4 Hz	2.048 MHz	8k lock	0.05 p-p	0.012 p-p
G-736[9] for 2.048MHz.	20 Hz to 100 kHz	4 Hz	2.048 MHz	8k lock	0.05 p-p	0.012 p-p
GR-499-CORE[23] & G824[18] for 1.544 MHz.	10 Hz to 40kHz	4 Hz	1.544 MHz	8k lock	5.0 p-p	0.006 p-p
GR-499-CORE[23] & G824[18] for 1.544 MHz.	8 kHz to 40kHz	4 Hz	1.544 MHz	8k lock	0.1 p-p	0.006 p-p
GR-1244-CORE[24] for 1.544 MHz.	>10 Hz	4 Hz	1.544 MHz	8k lock	0.05 p-p	0.006 p-p
25 MHz OP	12 kHz to 1.3 MHz	8 Hz	19.44 MHz	Direct	See [28]	0.021 p-p
50 MHz OP	12 kHz to 1.3 MHz	8 Hz	19.44 MHz	Direct	See [28]	0.025 p-p
62.5 MHz OP	12 kHz to 1.3 MHz	8 Hz	19.44 MHz	Direct	See [28]	0.035 p-p
125 MHz OP	12 kHz to 1.3 MHz	8 Hz	19.44 MHz	Direct	See [28]	0.066 p-p

NOTE: This table is only for comparing the device output jitter performance against values and quoted in various specifications for given conditions. It should not be used to infer compliance to any other aspects of these specifications.

Input/output timing

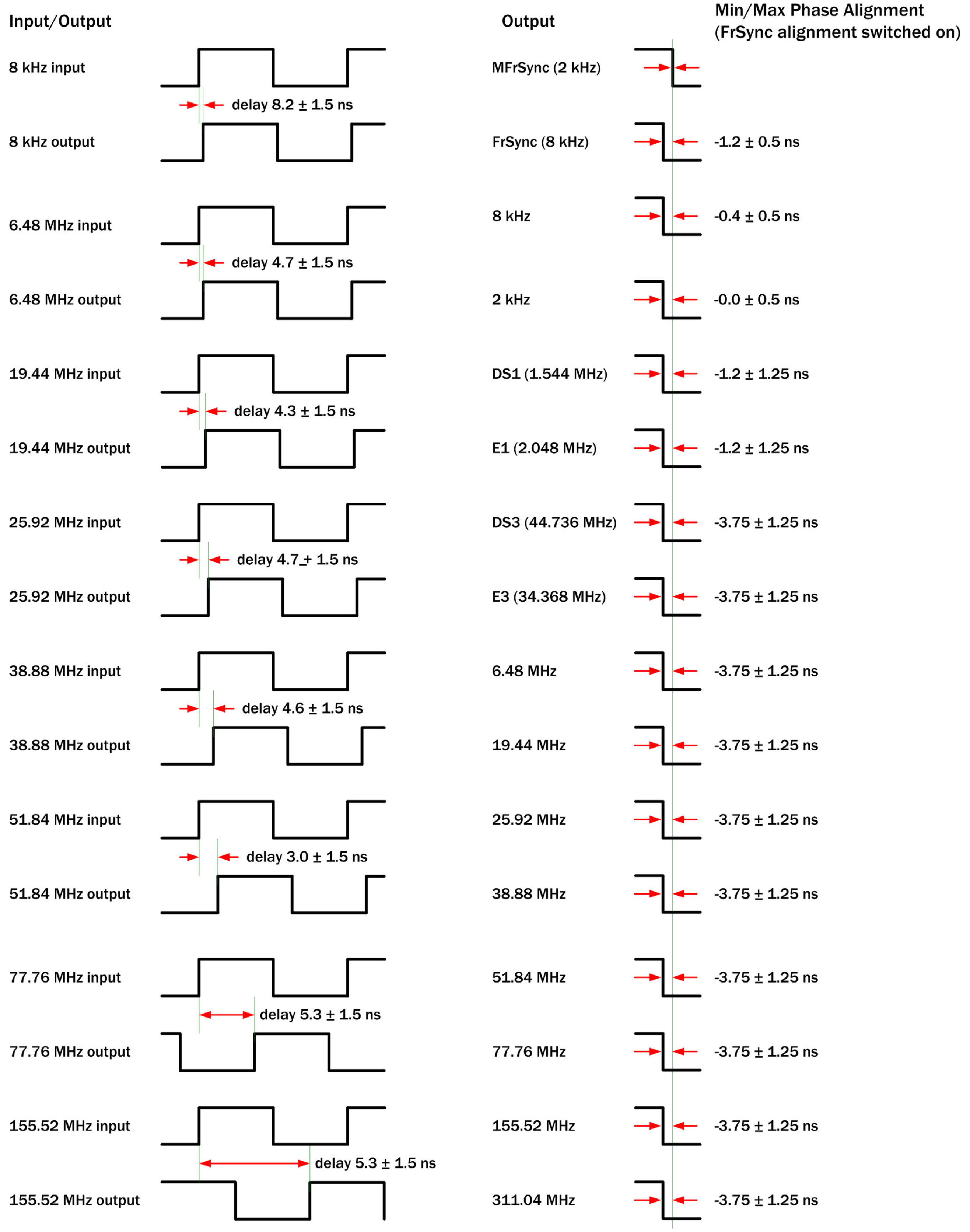

Figure 32 - Input/output timing diagram

Table 43 Output reference source selection table

SETS port name	ACS9522 signal name	Output port technology	Frequencies supported
T01	OPCLK0	TTL/CMOS	Frequency selection as per Table 44 and Table 47.
T02	OPCLK1	TTL/CMOS	Same as OPCLK0
T03	OPCLK7	TTL/CMOS	Same as OPCLK0
T04	OPCLK2	TTL/CMOS	Same as OPCLK0
T05	OPCLK3	TTL/CMOS	Same as OPCLK0
T06	OPCLK4	LVDS/LVPECL	Differential up to 311.04 MHz
T07	OPCLK5	LVDS/LVPECL	Differential up to 311.04 MHz
T08	OPCLK6	AMI	64/8 kHz (composite clock, 64 kHz + 8 kHz), fixed frequency
T09	OPCLK8	TTL/CMOS	Same as OPCLK0
FrameSync	OPCLK9	TTL/CMOS	8 kHz
MultiFrameSync	OPCLK10	TTL/CMOS	2 kHz

Table 44 Frequency divider look-up

APLL frequency	APLL/2	APLL/4	APLL/6	APLL/8	APLL/12	APLL/16	APLL/48	APLL/64
311.04	155.52	77.76	51.84	38.88	25.92	19.44	6.48	4.86
274.944	137.472	68.376	-	34.368	-	17.184	5.728	4.296
178.944	89.472	44.736	-	22.368	-	11.184	3.728	2.796
148.224	74.112	37.056	24.704	18.528	12.352	9.264	3.088	2.316
131.072	65.536	32.768	21.84533	16.384	10.92267	8.192	2.730667	2.048
98.816	49.408	24.704	16.46933	12.352	8.234667	6.176	2.058667	1.544
98.304	49.152	24.576	16.384	12.288	8.192	6.144	2.048	1.536

NOTE: All frequencies are in MHz.

Table 45 T0 APLL frequencies

T0 APLL frequency	T0 mode	T0 DPLL frequency control register bits cnfg_T0_DPLL_frequency [2:0]	Output jitter level ns (p-p)
311.04 MHz	Normal (digital feedback)	000	<0.5
311.04 MHz	Normal (analog feedback)	001	<0.5
98.304 MHz	12E1 (digital feedback)	010	<2
131.072 MHz	16E1 (digital feedback)	011	<2
148.224 MHz	24DS1 (digital feedback)	100	<2
98.816 MHz	16DS1 (digital feedback)	101	<2
-	Do not use	110	-
-	Do not use	111	-

Table 46 T4 APLL frequencies

T4 APLL frequency	T4 mode	T4 forward DFS frequency (MHz)	T4 DPLL frequency control register bits Reg 64 [2:0]	T4 APLL for T0 enable register bit Reg 65 [6]	T0 frequency to T4 APLL register bits Reg 65 [5:4]	Output jitter level ns (p-p)
311.04 MHz	Squelched	77.76	000	0	XX	<0.5
311.04 MHz	Normal	77.76	001	0	XX	<0.5
98.304 MHz	12E1	24.576	010	0	XX	<0.5
131.072 MHz	16E1	32.768	011	0	XX	<0.5
148.224 MHz	24DS1	37.056 (2*18.528)	100	0	XX	<0.5
98.816 MHz	16DS1	24.704	101	0	XX	<0.5
274.944 MHz	E3	68.736 (2*34.368)	110	0	XX	<0.5
178.944 MHz	DS3	44.736	111	0	XX	<0.5
98.304 MHz	T0-12E1	-	XXX	1	00	<2
131.072 MHz	T0-16E1	-	XXX	1	01	<2
148.224 MHz	T0-24DS1	-	XXX	1	10	<2
98.816 MHz	T0-16DS1	-	XXX	1	11	<2

Table 47   T01 to T07 output frequency selection

Value in register	Output frequency for given value in register for the Cnfg_output_frequency register of each output port						
	T01 Reg 60 [3:0]	T02 Reg 60 [7:4]	T03 Reg 61 [3:0]	T04 Reg 61 [7:4]	T05 Reg 62 [3:0]	T06 Reg 62 [7:4]	T07 Reg 63 [3:0]
0000	Off	Off	Off	Off	Off	Off	Off
0001	2 kHz	2 kHz	2 kHz	2 kHz	2 kHz	2 kHz	2 kHz
0010	8 kHz	8 kHz	8 kHz	8 kHz	8 kHz	8 kHz	8 kHz
0011	Digital2	Digital2	Digital2	Digital2	Digital2	T0 APLL/2	Digital2
0100	Digital1	Digital1	Digital1	Digital1	Digital1	Digital1	T0 APLL/2
0101	T0 APLL/48	T0 APLL/48	T0 APLL/48	T0 APLL/48	T0 APLL/48	T0 APLL/1	T0 APLL/48
0110	T0 APLL/16	T0 APLL/16	T0 APLL/16	T0 APLL/16	T0 APLL/16	T0 APLL/16	T0 APLL/16
0111	T0 APLL/12	T0 APLL/12	T0 APLL/12	T0 APLL/12	T0 APLL/12	T0 APLL/12	T0 APLL/12
1000	T0 APLL/8	T0 APLL/8	T0 APLL/8	T0 APLL/8	T0 APLL/8	T0 APLL/8	T0 APLL/8
1001	T0 APLL/6	T0 APLL/6	T0 APLL/6	T0 APLL/6	T0 APLL/6	T0 APLL/6	T0 APLL/6
1010	T0 APLL/4	T0 APLL/4	T0 APLL/4	T0 APLL/4	T0 APLL/4	T0 APLL/4	T0 APLL/4
1011	T4 APLL/64	T4 APLL/64	T4 APLL/64	T4 APLL/2	T4 APLL/2	T4 APLL/64	T4 APLL/64
1100	T4 APLL/48	T4 APLL/48	T4 APLL/48	T4 APLL/48	T4 APLL/48	T4 APLL/48	T4 APLL/48
1101	T4 APLL/16	T4 APLL/16	T4 APLL/16	T4 APLL/16	T4 APLL/16	T4 APLL/16	T4 APLL/16
1110	T4 APLL/8	T4 APLL/8	T4 APLL/8	T4 APLL/8	T4 APLL/8	T4 APLL/8	T4 APLL/8
1111	T4 APLL/4	T4 APLL/4	T4 APLL/4	T4 APLL/4	T4 APLL/4	T4 APLL/4	T4 APLL/4

Table 48 T01 to T06 output Ethernet frequency selection

Value in register	Output frequency for given value in register for the Cnfg_output_frequency register of each output port					
	T01 Reg 60 [3:0] Reg 20[0] = 1	T02 Reg 60 [7:4] Reg 20[1] = 1	T03 Reg 61 [3:0] Reg 20[2] = 1	T04 Reg 61 [7:4] Reg 20[3] = 1	T05 Reg 62 [3:0] Reg 20[4] = 1	T06 Reg 62 [7:4] Reg 20[5] = 1
xx00	25 MHz	25 MHz	25 MHz	25 MHz	25 MHz	25 MHz
xx01	50 MHz	2 kHz	2 kHz	2 kHz	2 kHz	2 kHz
xx10	62.5 MHz	8 kHz	8 kHz	8 kHz	8 kHz	8 kHz
xx11	125 MHz	125 MHz	125 MHz	125 MHz	125 MHz	125 MHz

T4 low frequency outputs

OPCLK6POS/NEG always produces a 64 kHz/8 kHz AMI composite clock, if enabled.

Jitter on the low frequency outputs

The T4 feedback DFS block is clocked by the T4 forward DFS, or its APLL. The frequency of the T4 forward DFS block can be determined by referring to Table 46 (T4 APLL frequencies). This is in the region of 65 MHz to 89 MHz and so has an approximate period of between 11 ns and 15 ns.

The output of the T4 forward DFS block has an inherent peak to peak jitter of approximately 4.9 ns. The clock to the T4 feedback DFS block has <1 ns of jitter when the T4 path is in analog feedback mode or 4.9 ns when in digital feedback mode.

Digital1 and Digital2 outputs

Frequencies Digital1 and Digital2 can be selected by outputs OPCLK[4:0]. Digital1 and Digtal2 are single frequencies selected from the range shown in Table 49.

Both of these frequencies are generated by the T0 LF output DFS block, which is clocked by the T0 77.76 MHz output DFS block. The T0 output APLL can be selected to reduce output jitter.

Jitter on the Digital1 and Digital2 outputs

The input clock frequency of the T0 DFS is always 77.76 MHz and so has a period of approximately 12 ns. The jitter generated on the digital outputs is relatively high, because they do not pass through an APLL for jitter filtering. The minimum level of jitter is when the T0 path is in analog feedback mode, when the p-p jitter is approximately 12 ns. The maximum jitter is generated when in digital feedback mode, when the total is approximately 17 ns.

Table 49 Digital frequency selections

Digital1 control Reg.39 [5:4]	Digital1 SONET/SDH Reg. 38 [5]	Digital1 Frequency (MHz)
00	0	2.048
01	0	4.096
10	0	8.192
11	0	16.384
00	1	1.544
01	1	3.088
10	1	6.176
11	1	12.352

Digital2 control Reg. 39 [7:6]	Digital2 SONET/SDH Reg.38 [6]	Digital2 frequency (MHz)
00	0	2.048
01	0	4.096
10	0	8.192
11	0	16.384
00	1	1.544
01	1	3.088
10	1	6.176
11	1	12.352

NOTE: If the EPLL is disabled at any point after and re-enabled, a manual toggle of extsync_en is required to guarantee ethernet frequencies on any output.

Interrupt requests from the TDM Block

Interrupt requests made by functions within the TDM Block are flagged onto the INTREQ pin. Bits in the sts_interrupts register are set high by any of the following events:

- Any reference source becoming valid or going invalid.
- A change in the operating state of the device (e.g. locked).
- A brief loss of the currently selected reference source.
- An AMI input error.

All interrupt sources can be masked by setting bits in the cnfg_interrupt_mask [7:0], cnfg_interrupt_mask [15:8] and cnfg_interrupt_mask [23:16] registers. Each interrupt source can be enabled by writing a 1 to the appropriate bit. If an unmasked interrupt source becomes active, the INTREQ pin is asserted. The active state of the INTREQ pin (high or low) is programmable via the cnfg_interrupt register.

Each interrupt is cleared by writing a 1 to the respective bit in the status register. Clearing all pending unmasked interrupts causes the interrupt pin to go inactive.

CONTROL REGISTERS OF THE TDM BLOCK

The TDM Block is controlled by a set of registers which are accessed via API calls over the SPI. A summary of the registers is shown in Table 50 and each register is described in detail in section TDM Block register descriptions.

TDM Block register organisation

The ACS9522 uses an array of register locations, each of 8 bits in length. Registers are identified by a register name and a corresponding hexadecimal register address. They are presented here in ascending address order.

Each register is organized with the left-most bit being the most significant bit (MSB), and the right-most bit being the least significant bit (LSB), as shown in Figure 33.

Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MSB							LSB

Figure 33 - Organization of the register bits.

The size of individual data fields ranges from single-bit values upwards. Data fields that are longer than 8 bits, for example the chip_id register, are spread across multiple registers. Refer to Table 50 for an overview of the register set.

Shaded areas in the register map are “don’t care” bits. Writing a 0 or a 1 to these bits does not affect any function of the device. Bits labelled “Set to zero” or “Set to one” must be set as stated during initialization of the device following power- up or after a power-on reset (POR). Failure to correctly set these bits may cause the device to operate in unexpected ways.

CAUTION!
Do not write to any undefined register addresses as this may cause the device to operate in a test mode. If an undefined register has been inadvertently addressed, the device should be reset, to ensure the undefined registers are returned to their default values.

Multi-word registers

For multi-word registers (e.g. sts_current_DPLL_frequency [7:0] and sts_current_DPLL_frequency [15:8]), every bit must be written to the correct address, without any other access taking place, before their combined value can take effect. If this sequence is interrupted, then the new bits that have been written are ignored. Reading an address that is part of a multi-word register freezes the other addresses in that register. This ensures that all of the bits that are read correspond to the same complete word.

Register access

Most registers are of one of two types, configuration registers or status registers.

Configuration registers

Configuration registers may be accessed at any time. The complete 8-bit register must be written, even if only one bit is being modified. Each configuration register reverts to a default value on power-up or after a reset. Most default values are fixed, but some are pin-settable. All configuration registers can be read out over the serial interface.

Status registers

All status registers may be read at any time. Some status registers, such as the sts_interrupts register, are designated R/W in the register map. In these registers, an individual data field may be cleared by writing a 1 into each bit of the field. Writing a 0 value into a bit does not affect the value of the bit.

All status registers are read via shadow registers, to avoid data hits caused by dynamic operation of the device. Each individual status register has a unique location.

Default values

Each register is given a defined default value at reset. These values are listed in the register map and the register description tables. Some read-only status registers may not necessarily default to the values that are given in the tables. This is because these registers reflect the status of the device at the time the register is read.

If the device is configured in a different way, or if its status changes immediately after the reset event, the register reports a different value. In the same way, the default values given for shaded areas could take different values to those stated

The entries in the Register name column are hyperlinks - click on a name to go to the register description.
In the Address and Default columns, the values are hexadecimal (0x).

TDM Block register map

Table 50 Register map

Register name	Address	Default	Bit significance							
			7 (MSB)	6	5	4	3	2	1	0 (LSB)
chip_id	*00*	*52*	*device part number [7:0] 8 least significant bits of the chip_ID*							
	01	*21*	*device part number [15:8] 8 most significant bits of the chip_ID*							
chip_revision	*02*	*04*	*chip_revision number [7:0]*							
test_register1	*03*	*14*	*phase_ alarm*	*disable_ 180*		*resync_ analog*	*Set to 0*	*8K_edge_ polarity*	*Set to zero*	*Set to zero*
sts_interrupts	*05*	*FF*	*I8_valid_ change*	*I7_valid_ change*	*I6_valid_ change*	*I5_valid_ change*	*I4_valid_ change*	*I3_valid_ change*	*I2_valid_ change*	*I1_valid_ change*
	06	*3F*	*operating_ mode*	*main_ref_ failed*	*I14_valid_ change*	*I13_valid_ change*	*I12_valid_ change*	*I11_valid_ change*	*I10_valid_ change*	*I9_valid_ change*
sts_current_DPLL_frequency [18:16], see 0C/DC	*07*	*00*						*bits [18:16] of sts_current_DPLL_frequency*		
sts_interrupts	*08*	*50*	*sync_ip_ alarm*	*T4_status*		*T4_inputs_ failed*	*AMI2_Viol*	*AMI2_LOS*	*AMI1_Viol*	*AMI1_LOS*
sts_operating	*09*	*41*	*SYNC2K_ alarm*	*T4_DPLL_ lock*	*T0_DPLL_ freq_soft_ alarm*	*T4_DPLL_ freq_soft_ alarm*		*T0_DPLL_operating_mode*		
sts_priority_table	*0A*	*00*	*Highest priority validated source*				*currently selected source*			
	0B	*00*	*3rd highest priority validated source*				*2nd highest priority validated source*			
sts_current_DPLL_frequency [7:0]	*0C*	*00*	*bits [7:0] of current_DPLL_frequency*							
sts_current_DPLL_frequency [15:8]	*0D*	*00*	*bits [15:8] of current_DPLL_frequency*							
sts_current_DPLL_frequency [18:16]	*07*	*00*						*bits [18:16] of current_DPLL_frequency*		
sts_sources_valid	*0E*	*00*	*I8*	*I7*	*I6*	*I5*	*I4*	*I3*	*I2*	*I1*
	0F	*00*			*I14*	*I13*	*I12*	*I11*	*I10*	*I9*
sts_reference_sources status of input channels:			*out-of-band alarm (soft)*	*out-of-band alarm (hard)*	*no_activity_ alarm*	*phase_lock _alarm*	*out-of-band _alarm (soft)*	*out-of band_alarm (hard)*	*no_activity_ alarm*	*phase_lock _alarm*
sts_reference_sources Input pairs (1 & 2)	*10*	*66*	*status_of_I2_input*				*status_of_I1_input*			
sts_reference_sources Input pairs (3 & 4)	*11*	*66*	*status_of_I4_input*				*status_of_I3_input*			
sts_reference_sources Input pairs (5 & 6)	*12*	*66*	*status_of_I6_input*				*status_of_I5_input*			
sts_reference_sources Input pairs (7 & 8)	*13*	*66*	*status_of_I8_input*				*status_of_I7_input*			
sts_reference_sources Input pairs (9 & 10)	*14*	*66*	*status_of_I10_input*				*status_of_I9_input*			
sts_reference_sources Input pairs (11 & 12)	*15*	*66*	*status_of_I12_input*				*status_of_I11_input*			
sts_reference_sources Input pairs (13 & 14)	*16*	*66*	*status_of_I14_input*				*status_of_I13_input*			
cnfg_ref_selection_priority (1 & 2)	*18*	*32*	*programmed_priority_I2*				*programmed_priority_I1*			
cnfg_ref_selection_priority (3 & 4)	*19*	*54*	*programmed_priority_I4*				*programmed_priority_I3*			

Table 50 Register map

Register name	Address	Default	Bit significance							
			7 (MSB)	6	5	4	3	2	1	0 (LSB)
cnfg_ref_selection_priority (5 & 6)	1A	76	*programmed_priority_I6*				*programmed_priority_I5*			
cnfg_ref_selection_priority (7 & 8)	1B	98	*programmed_priority_I8*				*programmed_priority_I7*			
cnfg_ref_selection_priority (9 & 10)	1C	BA	*programmed_priority_I10*				*programmed_priority_I9*			
cnfg_ref_selection_priority (11 & 12)	1D	DC	*programmed_priority_I12*				*programmed_priority_I11*			
cnfg_ref_selection_priority (13 & 14)	1E	FE	*programmed_priority_I14*				*programmed_priority_I13*			
cnfg_enet_freq	20	00	*enet_2K_ enable*	*enet_PLL_ enable*	*T06_enet*	*T05_enet*	*T04_enet*	*T03_enet*	*T02_enet*	*T01_enet*
cnfg_ref_source_frequency_2	21	00	*Set to zero*		*bucket_id_2*		*Set to zero*			
cnfg_ref_source_frequency_3	22	00	*divn_3*	*lock8k_3*	*bucket_id_3*		*reference_source_frequency_3*			
cnfg_ref_source_frequency_4	23	00	*divn_4*	*lock8k_4*	*bucket_id_4*		*reference_source_frequency_4*			
cnfg_ref_source_frequency_5	24	03	*divn_5*	*lock8k_5*	*bucket_id_5*		*reference_source_frequency_5*			
cnfg_ref_source_frequency_6	25	03	*divn_6*	*lock8k_6*	*bucket_id_6*		*reference_source_frequency_6*			
cnfg_ref_source_frequency_7	26	03	*divn_7*	*lock8k_7*	*bucket_id_7*		*reference_source_frequency_7*			
cnfg_ref_source_frequency_8	27	03	*divn_8*	*lock8k_8*	*bucket_id_8*		*reference_source_frequency_8*			
cnfg_ref_source_frequency_9	28	03	*divn_9*	*lock8k_9*	*bucket_id_9*		*reference_source_frequency_9*			
cnfg_ref_source_frequency_10	29	03	*divn_10*	*lock8k_10*	*bucket_id_10*		*reference_source_frequency_10*			
cnfg_ref_source_frequency_11	2A	03	*divn_11*	*lock8k_11*	*bucket_id_11*		*reference_source_frequency_11*			
cnfg_ref_source_frequency_12	2B	01	*divn_12*	*lock8k_12*	*bucket_id_12*		*reference_source_frequency_12*			
cnfg_ref_source_frequency_13	2C	01	*divn_13*	*lock8k_13*	*bucket_id_13*		*reference_source_frequency_13*			
cnfg_ref_source_frequency_14	2D	01	*divn_14*	*lock8k_14*	*bucket_id_14*		*reference_source_frequency_14*			
cnfg_sts_remote_sources_valid [I8:I1]	30	FF	*I8 remote status*	*I7 remote status*	*I6 remote status*	*I5 remote status*	*I4 remote status*	*I3 remote status*	*I2 remote status*	*I1 remote status*
cnfg_sts_remote_sources_valid [I14:I9]	31	3F			*I14 remote status*	*I13 remote status*	*I12 remote status*	*I11 remote status*	*I10 remote status*	*I9 remote status*
cnfg_operating_mode	32	00						*TO_DPLL_operating_mode*		
force_select_reference_source	33	0F					*forced_reference_source*			
cnfg_input_mode (bit 1 RO, otherwise R/W)	34	C2	*auto_ extsync_en*	*phalarm_ timeout*	*XO_ edge*	*man_ holdover*	*extsync_en*	*ip_sonsdhb*	*master_ slaveb*	*reversion_ mode*
cnfg_T4_path	35	40	*lock_T4_to_ T0*	*T4_dig_ feedback*		*T4_op_ from_T0*	*T4_forced_reference_source*			
cnfg_differential_inputs	36	02							*I6_LVPECL*	*I5_LVDS*
cnfg_uPsel_pins	37	05						*Microprocessor type*		
cnfg_dig_outputs_sonsdh	38	1F		*dig2_ sonsdh*	*dig1_ sonsdh*					
cnfg_digital_frequencies	39	08	*digital2_frequency*		*digital1_frequency*					
cnfg_differential_outputs	3A	C6					*T07_LVPECL_LVDS*		*T06_LVDS_LVPECL*	

Table 50 Register map

Register name	Address	Default	Bit significance 7 (MSB)	6	5	4	3	2	1	0 (LSB)
cnfg_auto_bw_sel	3B	FB	auto_BW_ sel				T0_lim_int			
cnfg_nominal_frequency [7:0]	3C	99	cnfg_nominal_frequency_value [7:0]							
cnfg_nominal_frequency [15:8]	3D	99	cnfg_nominal_frequency_value [15:8]							
cnfg_holdover_frequency [7:0]	3E	00	cnfg_nominal_frequency_value [7:0]							
cnfg_holdover_frequency [15:8]	3F	00	holdover_frequency_value [15:8]							
cnfg_holdover_modes	40	88	auto_ averaging	fast_ averaging	read_ average	mini_holdover_mode		holdover_frequency_ [18:16] (with registers 0x3E and 0x3F above)		
cnfg_DPLL_freq_limit [7:0]	41	76	DPLL_frequency_offset_limit [7:0]							
cnfg_DPLL_freq_limit [9:8]	42	00							DPLL_frequency_offset_ limit [9:8]	
cnfg_interrupt_mask [7:0]	43	00	I8 interrupt not masked	I7 interrupt not masked	I6 interrupt not masked	I5 interrupt not masked	I4 interrupt not masked	I3 interrupt not masked	I2 interrupt not masked	I1 interrupt not masked
cnfg_interrupt_mask [15:8]	44	40	operating_ mode_ interrupt_ not_ masked	main_ref_ failed_ interrupt_ not_ masked	I14 interrupt not masked	I13 interrupt not masked	I12 interrupt not masked	I11 interrupt not masked	I10 interrupt not masked	I9 interrupt not masked
cnfg_interrupt_mask [23:16]	45	00	Sync_ip_ alarm interrupt not masked	T4_status interrupt not masked		T4_inputs_ failed interrupt not masked	AMI2_Viol interrupt not masked	AMI2_LOS interrupt not masked	AMI1_Viol interrupt not masked	AMI1_LOS interrupt not masked
cnfg_freq_divn [7:0]	46	FF	divn_value [7:0]							
cnfg_freq_divn [13:8]	47	3F			divn_value [13:8]					
cnfg_monitors	48	05	freq_mon_ clk	los_flag_ on_TDO	ultra_fast_ switch	ext_ switch	PBO_freeze	PBO_en	freq_ monitor_ soft_enable	freq_ monitor_ hard_ enable
cnfg_freq_mon_threshold	49	23	soft_frequency_alarm_threshold [3:0]				hard_frequency_alarm_threshold [3:0]			
cnfg_current_freq_mon_threshold	4A	23	current_soft_frequency_alarm_threshold [3:0]				current_hard_frequency_alarm_threshold [3:0]			
cnfg_registers_source_select	4B	00				T4_T0_ select	frequency_measurement_channel_select [3:0]			
sts_freq_measurement	4C	00	freq_measurement_value [7:0]							
cnfg_DPLL_soft_limit	4D	8E	freq_lim_ phase_loss _enable	frequency alarm: DPLL_soft_limit_value [6:0] (resolution = 0.628 ppm)						
cnfg_upper_threshold_0	50	06	activity alarm: upper_threshold_0_value [7:0]							
cnfg_lower_threshold_0	51	04	activity alarm: lower_threshold_0_value [7:0]							
cnfg_bucket_size_0	52	08	activity alarm: bucket_size_0_value [7:0]							
cnfg_decay_rate_0	53	01							decay_rate_0_value [1:0]	
cnfg_upper_threshold_1	54	06	activity alarm: upper_threshold_1_value [7:0]							
cnfg_lower_threshold_1	55	04	activity alarm: lower_threshold_1_value [7:0]							
cnfg_bucket_size_1	56	08	activity alarm: bucket_size_1_value [7:0]							
cnfg_decay_rate_1	57	01							decay_rate_1_value [1:0]	
cnfg_upper_threshold_2	58	06	activity alarm: upper_threshold_2_value [7:0]							

Table 50 Register map

Register name	Address	Default	Bit significance							
			7 (MSB)	6	5	4	3	2	1	0 (LSB)
cnfg_lower_threshold_2	59	04	*activity alarm: lower_threshold_2_value [7:0]*							
cnfg_bucket_size_2	5A	08	*activity alarm: bucket_size_2_value [7:0]*							
cnfg_decay_rate_2	5B	01							*decay_rate_2_value [1:0]*	
cnfg_upper_threshold_3	5C	06	*activity alarm: upper_threshold_3_value [7:0]*							
cnfg_lower_threshold_3	5D	04	*activity alarm: lower_threshold_3_value [7:0]*							
cnfg_bucket_size_3	5E	08	*activity alarm: bucket_size_3_value [7:0]*							
cnfg_decay_rate_3	5F	01							*decay_rate_3_value [1:0]*	
cnfg_output_frequency (TO1 & TO2)	60	85	*output_freq_2 (TO2)*				*output_freq_1 (TO1)*			
cnfg_output_frequency (TO3 & TO4)	61	86	*output_freq_4 (TO4)*				*output_freq_3 (TO3)*			
cnfg_output_frequency (TO5 & TO6)	62	8A	*output_freq_6 (TO6)*				*output_freq_5 (TO5)*			
cnfg_output_frequency (TO7 to TO11)	63	F6	*MFrSyncen*	*FrSyncen*	*TO9_enable*	*TO8_enable*	*output_freq_7 [TO7]*			
cnfg_T4_DPLL_frequency	64	01		*auto_ disable_T4_ output*	*AMI_duty_ cycle*	*T4_SONET/ SDH_ selection*		*T4_DPLL_frequency*		
cnfg_T0_DPLL_frequency	65	01	*T4_meas_ T0_ph*	*T4 _APLL_ for_T0*	*T0 Freq to T4 APLL*			*T0_DPLL_frequency*		
cnfg_T4_DPLL_bw	66	00							*T4_DPLL_bandwidth [1:0]*	
cnfg_T0_DPLL_locked_bw	67	0B				*T0_DPLL_locked_bandwidth [5:0]*				
cnfg_T0_DPLL_acq_bw	69	0F				*T0_DPLL_acquisition_bandwidth [5:0]*				
cnfg_T4_DPLL_damping	6A	13		*T4_PD2_gain_alog_8K [6:4]*				*T4_damping [2:0]*		
cnfg_T0_DPLL_damping	6B	13		*T0_PD2_gain_alog_8K [6:4]*				*T0_damping [2:0]*		
cnfg_T4_DPLL_PD2_gain	6C	C2	*T4_PD2_ gain_ enable*	*T4_PD2_gain_alog [6:4]*				*T4_PD2_gain_digital [2:0]*		
cnfg_T0_DPLL_PD2_gain	6D	C2	*T0_PD2_ gain_ enable*	*T0_PD2_gain_alog [6:4]*				*T0_PD2_gain_digital [2:0]*		
cnfg_phase_offset [7:0]	70	00	*phase_offset_value[7:0]*							
cnfg_phase_offset [15:8]	71	00	*phase_offset_value[15:8]*							
cnfg_PBO_phase_offset	72	00			*PBO_phase_offset [5:0]*					
cnfg_phase_loss_fine_limit	73	A2	*fine_limit_ phase_loss _enable (1)*	*no_activity_ for_phase_ loss*	*test_bit set to 1*			*phase_loss_fine_limit [2:0]*		
cnfg_phase_loss_coarse_limit	74	85	*coarse_lim_ phase_loss _en*	*wide_range _en*	*enable_ multi_ph_ resp*		*phase_loss_coarse_limit [3:0] (in UI p-p)*			
cnfg_phasemon	76	06	*ip_noise_ window enable*							
sts_current_phase [7:0]	77	00	*current_phase [7:0]*							
sts_current_phase [15:8]	78	00	*current_phase [15:8]*							
cnfg_phase_alarm_timeout	79	32			*timeout_value [5:0] (in 2 second intervals)*					

Table 50 Register map

Register name	Address	Default	Bit significance							
			7 (MSB)	6	5	4	3	2	1	0 (LSB)
cnfg_sync_pulses	*7A*	*00*	*2k_8k_ from_T4*				*8k_invert*	*8k_pulse enable*	*2k_invert*	*2k_pulse enable*
cnfg_sync_phase	*7B*	*00*	*indep_FrSync/ MFrSync*	*sync_OC-N_ rates*					*sync_phase*	
cnfg_sync_monitor	*7C*	*2B*	*ph_offset_ ramp*	*sync_monitor_limit*			*sync_reference_source*			
cnfg_interrupt	*7D*	*02*						*GPO_en interrupt enable*	*tristate_en interrupt enable*	*int_polarity interrupt enable*
cnfg_protection	*7E*	*85*	*protection_value*							
cnfg_upsel	*7F*	*05 **						*Microprocessor type (*default value depends on value on UPSEL[2:0] pins).*		

TDM Block register descriptions

Chip ID register [7:0]

Software name	Address (0x0)	Access	Default value
chip_id	00	RO	0101 0010
Description	The 8 least significant bits of the chip ID word.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*chip_id*	Least significant byte of the 2-byte device ID.	-	0x52	-

Chip ID register [15:8]

Software name	Address (0x0)	Access	Default value
chip_id	01	RO	0010 0001
Description	The 8 most significant bits of the chip ID word.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*chip_id*	Most significant byte of the 2-byte device ID.	-	0x21	-

Chip revision register

Software name	Address (0x0)	Access	Default value
chip_revision	02	RO	0000 0100
Description	The silicon revision of the device.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*chip_revision*	Silicon revision of the device.	-	0x04	-

Test register #1

Software name	Address (0x0)	Access	Default value
test_register1	03	R/W	0001 0100
Description	A register containing various test controls (not normally used).		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*phase_alarm*	(phase alarm (RO)) Instantaneous result from T0 DPLL.	0 1	T0 DPLL reporting phase locked. T0 DPLL reporting phase lost.	0
6	*disable_180*	Normally when the DPLL locks to a new reference, it tries to lock to the nearest edge (±180°) for the first 2 seconds. If the DPLL does not determine that it is phase locked after this time, then the capture range reverts to ±360°, corresponding to frequency and phase locking. Forcing the DPLL into frequency locking mode may reduce the time taken to frequency lock to a new reference by up to 2 seconds. However, if the new and old reference signals are very close in frequency and phase, this may cause an unnecessary phase shift of up to 360°.	0 1	T0 DPLL automatically determines frequency lock enable. T0 DPLL forced to always frequency and phase lock.	0
5	*Not used*	Not used.	-	-	-
4	*resync_analog*	(analog dividers re-synchronization) The analog output dividers include a synchronization mechanism to ensure phase lock at low frequencies between the input and the output.	0 1	Analog divider is only synchronized during the first 2 seconds after power-up. Analog dividers are always synchronized.This keeps the clocks that have been divided down from the APLL output, synchronised with equivalent frequency digital clocks in the DPLL. This ensures that output clocks of 6.48 MHz and above, are synchronised with the DPLL, even though the APLL is driven by a 77.76 MHz clock.	1
3	*Set to 0*	Test Control. Leave unchanged or set to 0.	0	Set to 0.	0
2	*8k Edge Polarity*	When Lock8k mode is selected for the current input reference source, this bit allows the system to lock onto either the rising or the falling edge of the input clock.	0 1	Lock to falling clock edge. Lock to rising clock edge.	1
1	*Set to 0*	Test Control. Leave unchanged or set to 0.	0	Set to 0.	0
0	*Set to 0*	Test Control. Leave unchanged or set to 0.	0	Set to 0.	0

STS interrupts register [7:0]

Software name	Address (0x0)	Access	Default value
sts_interrupts	05	R/W	1111 1111
Description	Bits [7:0] of the interrupt status register.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*input channel I8 validity changed*	Interrupt indicating that input channel I8 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input channel I8 has not changed status (valid/invalid). Input channel I8 has changed status (valid/invalid). Writing 1 resets the status to 0.	1
6	*input channel I7 validity changed*	Interrupt indicating that input channel I7 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input channel I7 has not changed status (valid/invalid). Input channel I7 has changed status (valid/invalid). Writing 1 resets the status to 0.	1
5	*input channel I6 validity changed*	Interrupt indicating that input channel I6 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input channel I6 has not changed status (valid/invalid). Input channel I6 has changed status (valid/invalid). Writing 1 resets the status to 0.	1
4	*input channel I5 validity changed*	Interrupt indicating that input channel I5 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input channel I5 has not changed status (valid/invalid). Input channel I5 has changed status (valid/invalid). Writing 1 resets the status to 0.	1
3	*input channel I4 validity changed*	Interrupt indicating that input channel I4 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input channel I4 has not changed status (valid/invalid). Input channel I4 has changed status (valid/invalid). Writing 1 resets the status to 0.	1
2	*input channel I3 validity changed*	Interrupt indicating that input channel I3 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input channel I3 has not changed status (valid/invalid). Input channel I3 has changed status (valid/invalid). Writing 1 resets the status to 0.	1
1	*input channel I2 validity changed*	Interrupt indicating that input channel I2 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input channel I2 has not changed status (valid/invalid). Input channel I2 has changed status (valid/invalid). Writing 1 resets the status to 0.	1
0	*input channel I1 validity changed*	Interrupt indicating that input channel I1 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input channel I1 has not changed status (valid/invalid). Input channel I1 has changed status (valid/invalid). Writing 1 resets the status to 0.	1

STS interrupts register [15:8]

Software name	Address (0x0)	Access	Default value
sts_interrupts	06	R/W	0011 1111
Description	Bits [15:8] of the interrupt status register.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*operating_ mode*	Interrupt indicating that the operating mode has changed. Latched until reset by software writing a 1 to this bit.	0 1	Operating mode has not changed. Operating mode has changed. Writing 1 resets the status to 0.	0
6	*main_ref_failed*	Interrupt indicating that the input to the T0 DPLL has failed. This interrupt is raised after 2 missing input cycles, which is much quicker than waiting for the input to become invalid. This input is not generated in free-run or holdover modes. Latched until reset by the software writing a 1 to this bit.	0 1	Input to the T0 DPLL is valid. Input to the T0 DPLL has failed. Writing 1 resets the status to 0.	0
5	*input channel I14 validity changed*	Interrupt indicating that input channel I14 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by the software writing a 1 to this bit.	0 1	Input channel I14 has not changed status (valid/invalid). Input channel I14 has changed status (valid/invalid). Writing 1 resets the status to 0.	1
4	*input channel I13 validity changed*	Interrupt indicating that input channel I13 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by the software writing a 1 to this bit.	0 1	Input channel I13 has not changed status (valid/invalid). Input channel I13 has changed status (valid/invalid). Writing 1 resets the status to 0.	1
3	*input channel I12 validity changed*	Interrupt indicating that input channel I12 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by the software writing a 1 to this bit.	0 1	Input channel I12 has not changed status (valid/invalid). Input channel I12 has changed status (valid/invalid). Writing 1 resets the status to 0.	1
2	*input channel I11 validity changed*	Interrupt indicating that input channel I11 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by the software writing a 1 to this bit.	0 1	Input channel I11 has not changed status (valid/invalid). Input channel I11 has changed status (valid/invalid). Writing 1 resets the status to 0.	1
1	*input channel I10 validity changed*	Interrupt indicating that input channel I10 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by the software writing a 1 to this bit.	0 1	Input channel I10 has not changed status (valid/invalid). Input channel I10 has changed status (valid/invalid). Writing 1 resets the status to 0.	1
0	*input channel I9 validity changed*	Interrupt indicating that input channel I9 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by the software writing a 1 to this bit.	0 1	Input channel I9 has not changed status (valid/invalid). Input channel I9 has changed status (valid/invalid). Writing 1 resets the status to 0.	1

STS current DPLL frequency register [18:16]

Software name			Address (0x0)	Access	Default value
sts_current_DPLL_frequency [18:16]			07	RO	0000 0000
Description	Bits [18:16] of the current DPLL frequency.				

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:3]	*Not used*	Not used.	-	-	-
[2:0]	*sts_current_ DPLL_ frequency [18:16]*	When the *T4_T0_select* bit of cnfg_registers_source_select = 0, the frequency for the T0 path is reported. When *T4_T0_select* =1, the frequency for the T4 path is reported.		See register description of sts_current_DPLL_frequency [15:8].	

STS interrupts register [23:16]

Software name			Address (0x0)	Access	Default value
sts_interrupts			08	R/W	0101 0000
Description	Bits [23:16] of the interrupt status register.				

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*Sync_ip_alarm*	Interrupt indicating that the frame sync input monitor has hit its alarm limit. Latched until reset by the software writing a 1 to this bit.	0 1	Input frame sync alarm has not occurred. Input frame sync alarm has occurred. Writing 1 resets the status to 0.	0
6	*T4_status*	Interrupt indicating that the T4 DPLL has lost lock (if it was locked) or gained lock (if it was not locked). Latched until reset by the software writing a 1 to this bit.	0 1	Input to the T4 DPLL has not changed. Input to the T4 DPLL has lost/ gained lock. Writing 1 resets the status to 0.	1
5	*Not used*	Not used.	-	-	0
4	*T4_inputs_ failed*	Interrupt indicating that no valid inputs are available to the T4 DPLL. Latched until reset by the software writing a 1 to this bit.	0 1	T4 DPLL has valid inputs. T4 DPLL has no valid inputs. Writing 1 resets the status to 0.	1
3	*AMI2_Viol*	Interrupt indicating that an AMI violation error has occurred on input channel I2. Latched until reset by the software writing a 1 to this bit.	0 1	Input channel I2 has had no LOS error. Input channel I2 has had a LOS error. Writing 1 resets the status to 0.	0
2	*AMI2_LOS*	Interrupt indicating that an AMI LOS error has occurred on input channel I2. Latched until reset by the software writing a 1 to this bit.	0 1	Input channel I2 has had no LOS error. Input channel I2 has had a LOS error. Writing 1 resets the status to 0.	0

continued...

STS interrupts register [23:16] (continued)

Bit	Bit name	Bit description	Value	Bit settings	Reset
1	*AMI1_Viol*	Interrupt indicating that an AMI violation error has occurred on input channel I1. Latched until reset by the software writing a 1 to this bit.	0 1	Input channel I1 has had no violation error. Input channel I1 has had a violation error. Writing 1 resets the status to 0.	0
0	*AMI1_LOS*	Interrupt indicating that an AMI LOS error has occurred on input channel I1. Latched until reset by the software writing a 1 to this bit.	0 1	Input channel I1 has had no LOS error. Input channel I1 has had a LOS error. Writing 1 resets the status to 0.	0

STS operating register

Software name	Address (0x0)	Access	Default value
sts_operating	09	RO	0100 0001
Description	Current operating state of the device's internal state machine.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*SYNC2K_alarm*	Reports the current status of the external Sync monitor alarm.	0 1	External Sync monitor not in alarm condition. External Sync monitor in alarm condition.	0
6	*T4_DPLL_Lock*	Reports the current phase lock status of the T4 DPLL. The T4 DPLL does not have the same state machine as the T0 DPLL, as it does not support all the features of the T0 DPLL. It can only report its state as locked or unlocked. This bit indicates that the T4 DPLL is locked by monitoring the T4 DPLL phase loss indicators, which potentially come from four sources. The four phase loss indicators are enabled by the same registers that enable them for the T0 DPLL, as follows: The fine phase loss detector is enabled by the *fine_limit_en* bit in the cnfg_phase_loss_fine_limit register. The coarse phase loss detector is enabled by the *coarse_lim_phaseloss_en* bit in the cnfg_phase_loss_coarse_limit. The phase loss indication from no activity on the input is enabled by the *noact_ph_loss* bit in the cnfg_phase_loss_fine_limit register. Phase loss indication from the DPLL reaching its minimum or maximum frequency limits is enabled by the *freq_lim_ph_loss* bit in the cnfg_DPLL_soft_limit register. Once the *T4_DPLL_Lock* bit is set = 0, indicating a loss of phase lock or cycle slips, it latches in that state. To clear the latched condition, the coarse phase loss detector should be temporarily disabled. To do this, set the *coarse_lim_phaseloss_en* bit in the cnfg_phase_loss_coarse_limit register =0. Then read this *T4_DPLL_Lock* bit to reset it. Finally re-enable the coarse phase loss detector by setting the *coarse_lim_phaseloss_en* bit of the cnfg_phase_loss_coarse_limit register =1. If this bit is indicating "locked" (*T4_DPLL_lock* bit in the sts_operating register =1), it is always a correct indication and no change to the coarse phase loss detector enable is required.	0 1	T4 DPLL is not phase locked to the reference source. T4 DPLL is phase locked to the reference source.	1
5	*T0_DPLL_freq_ soft_alarm*	The T0 DPLL has a programmable frequency limit and soft alarm limit. The DPLL tracks a reference input until its frequency reaches the frequency limit. However, if the frequency exceeds the soft limit value, it triggers an alarm. This bit reports the status of the soft alarm.	0 1	T0 DPLL tracking its reference within the limits of the programmed soft alarm. T0 DPLL tracking its reference beyond the limits of the programmed *soft* alarm.	0

continued...

STS operating register (continued)

Bit	Bit name	Bit description	Value	Bit settings	Reset
4	*T4_DPLL_freq_ soft_alarm*	The T4 DPLL has a programmable frequency limit and soft alarm limit. The DPLL tracks a reference input until its frequency reaches the frequency limit. However, if the frequency exceeds the soft limit value, it triggers an alarm. This bit reports the status of the soft alarm.	0 1	T4 DPLL tracking its reference within the limits of the programmed soft alarm. T4 DPLL tracking its reference beyond the limits of the programmed soft alarm.	0
3	*Not used*	Not used.	-	-	0
[2:0]	*T0_DPLL_ operating_ mode*	This field is used to report the state of the internal finite state machine controlling the T0 DPLL.	000 001 010 011 100 101 110 111	Not used. Free run mode. Holdover mode. Not used. Locked mode. Pre-locked2 mode. Pre-locked mode. Phase lost mode.	001

STS priority table register [7:0]

Software name	Address (0x0)	Access	Default value
sts_priority_table	0A	RO	0000 0000
Description	Bits [7:0] of the validated priority table.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:4]	*highest priority validated source*	Reports the input channel number of the highest priority validated source. If an input channel has been disallowed in the Configure STS remote sources valid register [7:0] and Configure STS remote sources valid register [13:8] registers, it does not appear in this list, even if it is valid. *When the *T4_T0_select* bit in the cnfg_registers_source_select register =0, the highest priority validated source for the T0 path is reported. When *T4_T0_select* =1, the highest priority validated source for the T4 path is reported.	0000	No valid source available.	0000
			0001	Input channel I1 is the highest priority valid source.	
			0010	Input channel I2 is the highest priority valid source.	
			0011	Input channel I3 is the highest priority valid source.	
			0100	Input channel I4 is the highest priority valid source.	
			0101	Input channel I5 is the highest priority valid source.	
			0110	Input channel I6 is the highest priority valid source.	
			0111	Input channel I7 is the highest priority valid source.	
			1000	Input channel I8 is the highest priority valid source.	
			1001	Input channel I9 is the highest priority valid source.	
			1010	Input channel I10 is the highest priority valid source.	
			1011	Input channel I11 is the highest priority valid source.	
			1100	Input channel I12 is the highest priority valid source.	
			1101	Input channel I13 is the highest priority valid source.	
			1110	Input channel I14 is the highest priority valid source.	
			1111	Not used.	

continued...

STS priority table register [7:0] (continued)

Bit	Bit name	Bit description	Value	Bit settings	Reset
[3:0]	*currently selected source*	Reports the input channel number of the currently selected source. When in non-revertive mode, this is not necessarily the same as the highest priority validated source. (See Selection of input reference clock sources for details). If an input channel has been disallowed in the Configure STS remote sources valid register [7:0] and Configure STS remote sources valid register [13:8] registers, it does not appear in this list, even if it is valid. *When the *T4_T0_select* bit in cnfg_registers_source_select =0, the currently selected source for the T0 path is reported. When *T4_T0_select* =1, the currently selected source for the T4 path is reported. The T4 path does not have a non-revertive mode so this is always the same as the highest priority validated source.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	No source currently selected. Input channel I1 is the currently selected source. Input channel I2 is the currently selected source. Input channel I3 is the currently selected source. Input channel I4 is the currently selected source. Input channel I5 is the currently selected source. Input channel I6 is the currently selected source. Input channel I7 is the currently selected source. Input channel I8 is the currently selected source. Input channel I9 is the currently selected source. Input channel I10 is the currently selected source. Input channel I11 is the currently selected source. Input channel I12 is the currently selected source. Input channel I13 is the currently selected source. Input channel I14 is the currently selected source. Not used.	0000

STS priority table register [15:8]

Software name	Address (0x0)	Access	Default value
sts_priority_table	0B	RO	0000 0000
Description	Bits [15:8] of the validated priority table.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:4]	*3rd highest priority validated source*	Reports the input channel number of the 3rd highest priority validated source. If an input channel has been disallowed in the Configure STS remote sources valid register [7:0] and Configure STS remote sources valid register [13:8] registers, it does not appear in this list, even if it is valid. *When the *T4_T0_select* bit in cnfg_registers_source_select =0, the 3rd highest priority validated source for the T0 path is reported. When *T4_T0_select* =1, the value of this register is always zero, as the T4 path does not maintain the 3rd highest priority validated source.	0000	Less than 3 valid sources available.	0000
			0001	Input channel I1 is the third highest priority valid source.	
			0010	Input channel I2 is the third highest priority valid source.	
			0011	Input channel I3 is the third highest priority valid source.	
			0100	Input channel I4 is the third highest priority valid source.	
			0101	Input channel I5 is the third highest priority valid source.	
			0110	Input channel I6 is the third highest priority valid source.	
			0111	Input channel I7 is the third highest priority valid source.	
			1000	Input channel I8 is the third highest priority valid source.	
			1001	Input channel I9 is the third highest priority valid source.	
			1010	Input channel I10 is the third highest priority valid source.	
			1011	Input channel I11 is the third highest priority valid source.	
			1100	Input channel I12 is the third highest priority valid source.	
			1101	Input channel I13 is the third highest priority valid source.	
			1110	Input channel I14 is the third highest priority valid source.	
			1111	Not used.	

continued...

STS priority table register [15:] (continued)

Bit	Bit name	Bit description	Value	Bit settings	Reset
[3:0]	*2nd highest priority validated source*	Reports the input channel number of the 2nd highest priority validated source. If an input channel has been disallowed in the Configure STS remote sources valid register [7:0] and Configure STS remote sources valid register [13:8] registers, it does not appear in this list, even if it is valid. *When the *T4_T0_select* bit in cnfg_registers_source_select =0, the 2nd highest priority validated source for the T0 path is reported. When *T4_T0_select* =1, the 2nd highest priority validated source for the T4 path is reported.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	Less than 2 valid sources available. Input channel I1 is the second highest priority valid source. Input channel I2 is the second highest priority valid source. Input channel I3 is the second highest priority valid source. Input channel I4 is the second highest priority valid source. Input channel I5 is the second highest priority valid source. Input channel I6 is the second highest priority valid source. Input channel I7 is the second highest priority valid source. Input channel I8 is the second highest priority valid source. Input channel I9 is the second highest priority valid source. Input channel I10 is the second highest priority valid source. Input channel I11 is the second highest priority valid source. Input channel I12 is the second highest priority valid source. Input channel I13 is the second highest priority valid source. Input channel I14 is the second highest priority valid source. Not used.	0000

STS current DPLL frequency register [7:0]

Software name	Address (0x0)	Access	Default value
sts_current_DPLL_frequency [7:0]	0C	RO	0000 0000
Description	Bits [7:0] of the current DPLL frequency.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*bits [7:0] of sts_current_ DPLL_ frequency*	*When the *T4_T0_select* bit in cnfg_registers_source_select =0, the frequency for the T0 path is reported. When *T4_T0_select* =1 the frequency for the T4 path is reported.	-	See register description of sts_current_DPLL_frequency [15:8].	0000 0000

STS current DPLL frequency register [15:8]

Software name	Address (0x0)	Access	Default value
sts_current_DPLL_frequency [15:8]	0D	RO	0000 0000
Description	Bits [15:8] of the current DPLL frequency.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*sts_current_ DPLL_ frequency[15:8]*	This value in this register is combined with the value in sts_current_DPLL_frequency [7:0] and sts_current_DPLL_frequency [15:8] to represent the current frequency offset of the DPLL. *When the *T4_T0_select* bit in cnfg_registers_source_select =0, the frequency for the T0 path is reported. When *T4_T0_select* =1, the frequency for the T4 path is reported.	-	In order to calculate the ppm offset of the DPLL with respect to the crystal oscillator frequency, concatenate the values in the sts_current_DPLL_frequency [18:16], sts_current_DPLL_frequency [15:8] and sts_current_DPLL_frequency [7:0] registers. This value is a 2's complement signed integer. The value multiplied by 0.0003068 dec gives the value in ppm offset with respect to the XO frequency, allowing for any crystal calibration that has been performed, via cnfg_nominal_frequency [7:0] and cnfg_nominal_frequency [15:8]. The value is actually the DPLL integral path value so it can be viewed as an average frequency, where the rate of change is related to the DPLL bandwidth. If the *T0_lim_int* bit in cnfg_auto_bw_sel is high then this value freezes if the DPLL has been pulled to its minimum or maximum frequency.	0000 0000

STS current DPLL frequency register [18:16]

Software name	Address (0x0)	Access	Default value
sts_current_DPLL_frequency [18:16]	07	RO	0000 0000
Description	Bits [18:16] of the current DPLL frequency.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:3]	*Not used*	Not used.	-	-	0000 0
[2:0]	*sts_current_ DPLL_ frequency [18:16]*	This value in this register is combined with the value in sts_current_DPLL_frequency [7:0] and sts_current_DPLL_frequency [15:8] to represent the current frequency offset of the DPLL. *When the *T4_T0_select* bit in cnfg_registers_source_select =0, the frequency for the T0 path is reported. When *T4_T0_select* =1, the frequency for the T4 path is reported.	-	In order to calculate the ppm offset of the DPLL with respect to the crystal oscillator frequency, concatenate the values in the sts_current_DPLL_frequency [18:16], sts_current_DPLL_frequency [15:8] and sts_current_DPLL_frequency [7:0] registers. This value is a 2's complement signed integer. The value multiplied by 0.0003068 dec gives the value in ppm offset with respect to the XO frequency, allowing for any crystal calibration that has been performed, via cnfg_nominal_frequency [7:0] and cnfg_nominal_frequency [15:8]. The value is actually the DPLL integral path value so it can be viewed as an average frequency, where the rate of change is related to the DPLL bandwidth. If the *T0_lim_int* bit in cnfg_auto_bw_sel is high then this value freezes if the DPLL has been pulled to its minimum or maximum frequency.	000

STS sources valid register [7:0]

Software name		Address (0x0)	Access	Default value
sts_sources_valid		0E	RO	0000 0000
Description	8 least significant bits of the *sts_sources_valid* register.			

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*I8*	Bit indicating if input channel I8 is valid. The input is valid if it has no outstanding alarms or a soft frequency alarm only.	0 1	Input channel I8 is invalid. Input channel I8 is valid.	0
6	*I7*	Bit indicating if input channel I7 is valid. The input is valid if it has no outstanding alarms or a soft frequency alarm only.	0 1	Input channel I7 is invalid. Input channel I7 is valid.	0
5	*I6*	Bit indicating if input channel I6 is valid. The input is valid if it has no outstanding alarms or has a soft frequency alarm only.	0 1	Input channel I6 is invalid. Input channel I6 is valid.	0
4	*I5*	Bit indicating if input channel I5 is valid. The input is valid if it has no outstanding alarms or a soft frequency alarm only.	0 1	Input channel I5 is invalid. Input channel I5 is valid.	0
3	*I4*	Bit indicating if input channel I4 is valid. The input is valid if it has no outstanding alarms or a soft frequency alarm only.	0 1	Input channel I4 is invalid. Input channel I4 is valid.	0
2	*I3*	Bit indicating if input channel I3 is valid. The input is valid if it has no outstanding alarms or a soft frequency alarm only.	0 1	Input channel I3 is invalid. Input channel I3 is valid.	0
1	*I2*	Bit indicating if input channel I2 is valid. The input is valid if it has no outstanding alarms or a soft frequency alarm only.	0 1	Input channel I2 is invalid. Input channel I2 is valid.	0
0	*I1*	Bit indicating if input channel I1 is valid. The input is valid if it has no outstanding alarms or a soft frequency alarm only.	0 1	Input channel I1 is invalid. Input channel I1 is valid.	0

STS sources valid register [15:8]

Software name		Address (0x0)	Access	Default value
sts_sources_valid		0F	RO	0000 0000
Description	8 most significant bits of the *sts_sources_valid* register.			

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:6]	*Not used*	Not used	-	-	-
5	*I14*	Bit indicating if input channel I14 is valid. The input is valid if it has no outstanding alarms or a soft frequency alarm only.	0 1	Input channel I14 is invalid. Input channel I14 is valid.	0
4	*I13*	Bit indicating if input channel I13 is valid. The input is valid if it has no outstanding alarms or a soft frequency alarm only.	0 1	Input channel I13 is invalid. Input channel I13 is valid.	0
3	*I12*	Bit indicating if input channel I12 is valid. The input is valid if it has no outstanding alarms or a soft frequency alarm only.	0 1	Input channel I12 is invalid. Input channel I12 is valid.	0
2	*I11*	Bit indicating if input channel I11 is valid. The input is valid if it has no outstanding alarms or a soft frequency alarm only.	0 1	Input channel I11 is invalid. Input channel I11 is valid.	0
1	*I10*	Bit indicating if input channel I10 is valid. The input is valid if it has no outstanding alarms or a soft frequency alarm only.	0 1	Input channel I10 is invalid. Input channel I10 is valid.	0
0	*I9*	Bit indicating if input channel I9 is valid. The input is valid if it has no outstanding alarms or a soft frequency alarm only.	0 1	Input channel I9 is invalid. Input channel I9 is valid.	0

STS reference sources register (input pairs 1 & 2)

Software name	Address (0x0)	Access	Default value
sts_reference_sources Input pairs (1 & 2)	10	RO except for test when R/W	0110 0110
Description	Reports any alarms active on input channels.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7&3	*Out-of-band alarm (soft)*	Soft, out of band alarm bit for the input channel. A soft alarm does not invalidate an input channel.	0 1	No alarm. The alarm is active. The alarm threshold (range) is set by the *current_soft_frequency_alarm_threshold* bits in cnfg_current_freq_mon_threshold, if the input channel is currently selected.	0
6&2	*Out-of-band alarm (hard)*	Hard out of band alarm bit for the input channel. A hard alarm invalidates an input channel.	0 1	No alarm. Alarm is active. The alarm threshold is set by the *current_hard_frequency_alarm_threshold* bits in cnfg_current_freq_mon_threshold, if the input channel is currently selected.	1
5&1	*No activity alarm*	Alarm indication from the activity monitors.	0 1	No alarm. The input has its no activity alarm active.	1
4&0	*Phase lock alarm*	This alarm is raised if the DPLL cannot indicate that it is phase locked on to the current source within 100 seconds.	0 1	No alarm. The phase lock alarm is active.	0

STS reference sources register (input channel pairs 3 & 4)

Software name		Address (0x0)	Access	Default value
sts_reference_sources Input pairs (3 & 4)		11	RO	0110 0110
Description	This register is the same as register 0x10 but using input channel pairs 3 & 4.			

STS reference sources register (input channel pairs 5 & 6)

Software name		Address (0x0)	Access	Default value
sts_reference_sources Input pairs (5 & 6)		12	RO	0110 0110
Description	This register is the same as register 0x10 but using input channel pairs 5 & 6.			

STS reference sources register (input channel pairs 7 & 8)

Software name		Address (0x0)	Access	Default value
sts_reference_sources Input pairs (7 & 8)		13	RO	0110 0110
Description	This register is the same as register 0x10 but using input channel pairs 7 & 8.			

STS reference sources register (input channel pairs 9 & 10)

Software name		Address (0x0)	Access	Default value
sts_reference_sources Input pairs (9 & 10)		14	RO	0110 0110
Description	This register is the same as register 0x10 but using input channel pairs 9 & 10.			

STS reference sources register (input channel pairs 11 & 12)

Software name		Address (0x0)	Access	Default value
sts_reference_sources Input pairs (11 & 12)		15	RO	0110 0110
Description	This register is the same as register 0x10 but using input channel pairs 11 & 12.			

STS reference sources register (input channel pairs 13&14)

Software name		Address (0x0)	Access	Default value
sts_reference_sources Input pairs (13 & 14)		16	RO	0110 0110
Description	This register is the same as register 0x10 but using input channel pairs 13 & 14.			

Configure reference selection priority register (1 & 2)

Software name	Address (0x0)	Access	Default value
cnfg_ref_selection_priority (1 & 2)	18	R/W	(T0) 0011 0010 (T4) 0000 0000
Description	Configures the relative priority of input channels I1 and I2.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:4]	*cnfg_ref_ selection_ priority_2*	This 4-bit value represents the relative priority of input channel I2. The smaller the number, the higher the priority. Setting a priority of zero disables the input channel. *When the *T4_T0_select* bit in cnfg_registers_source_select =0, the priority for the T0 path is configured. When *T4_T0_select* =1, the priority for the T4 path is configured.	0000 0001 to 1111	Input channel I2 is unavailable for automatic selection. Input channel I2 priority value.	See default value above.
[3:0]	*cnfg_ref_ selection_ priority_1*	This 4-bit value represents the relative priority of input channel I1. The smaller the number, the higher the priority. Setting a priority of zero disables the input channel. *When the *T4_T0_select* bit in cnfg_registers_source_select =0, the priority for the T0 path is configured. When *T4_T0_select* =1, the priority for the T4 path is configured.	0000 0001 to 1111	Input channel I1 is unavailable for automatic selection. Input channel I1 priority value.	See default value above.

Configure reference selection priority register (3 & 4)

Software name	Address (0x0)	Access	Default value
cnfg_ref_selection_priority (3 & 4)	19	R/W	(T0) 0101 0100 (T4) 0000 0000
Description	Configures the relative priority of input channels I3 and I4.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:4]	*cnfg_ref_ selection_ priority_4*	This 4-bit value represents the relative priority of input channel I4. The smaller the number, the higher the priority. Setting a priority of zero disables the input channel. *When the *T4_T0_select* bit in cnfg_registers_source_select =0, the priority for the T0 path is configured. When *T4_T0_select* =1, the priority for the T4 path is configured.	0000 0001 to 1111	Input channel I4 is unavailable for automatic selection. Input channel I4 priority value.	See default value above.
[3:0]	*cnfg_ref_ selection_ priority_3*	This 4-bit value represents the relative priority of input channel I3. The smaller the number, the higher the priority. Setting a priority of zero disables the input channel. *When the *T4_T0_select* bit in cnfg_registers_source_select =0, the priority for the T0 path is configured. When *T4_T0_select* =1, the priority for the T4 path is configured.	0000 0001 to 1111	Input channel I3 is unavailable for automatic selection. Input channel I3 priority value.	See default value above.

Configure reference selection priority register (5 & 6)

Software name	Address (0x0)	Access	Default value
cnfg_ref_selection_priority (5 & 6)	1A	R/W	(T0) 0111 0110 (T4) 0000 0000
Description	Configures the relative priority of input channels I5 and I6.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:4]	*cnfg_ref_ selection_ priority_6*	This 4-bit value represents the relative priority of input channel I6. The smaller the number, the higher the priority. Setting a priority of zero disables the input channel. *When the *T4_T0_select* bit in cnfg_registers_source_select =0, the priority for the T0 path is configured. When *T4_T0_select* =1, the priority for the T4 path is configured.	0000 0001 to 1111	Input channel I6 is unavailable for automatic selection. Input channel I6 priority value.	See default value above.
[3:0]	*cnfg_ref_ selection_ priority_5*	This 4-bit value represents the relative priority of input channel I5. The smaller the number, the higher the priority. Setting a priority of zero disables the input channel. *When the *T4_T0_select* bit in cnfg_registers_source_select =0, the priority for the T0 path is configured. When *T4_T0_select* =1, the priority for the T4 path is configured.	0000 0001 to 1111	Input channel I5 is unavailable for automatic selection. Input channel I5 priority value.	See default value above.

Configure reference selection priority register (7 & 8)

Software name	Address (0x0)	Access	Default value
cnfg_ref_selection_priority (7 & 8)	1B	R/W	(T0) 1001 1000 (T4) 1001 1000
Description	Configures the relative priority of input channels I7 and I8.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:4]	*cnfg_ref_ selection_ priority_8*	This 4-bit value represents the relative priority of input channel I8. The smaller the number, the higher the priority. Setting a priority of zero disables the input channel. *When the *T4_T0_select* bit in cnfg_registers_source_select =0, the priority for the T0 path is configured. When *T4_T0_select* =1, the priority for the T4 path is configured.	0000 0001 to 1111	Input channel I8 is unavailable for automatic selection. Input channel I8 priority value.	See default value above.
[3:0]	*cnfg_ref_ selection_ priority_7*	This 4-bit value represents the relative priority of input channel I7. The smaller the number, the higher the priority. Setting a priority of zero disables the input channel. *When the *T4_T0_select* bit in cnfg_registers_source_select =0, the priority for the T0 path is configured. When *T4_T0_select* =1, the priority for the T4 path is configured.	0000 0001 to 1111	Input channel I7 is unavailable for automatic selection. Input channel I7 priority value.	See default value above.

Configure reference selection priority register (9 & 10)

Software name	Address (0x0)	Access	Default value
cnfg_ref_selection_priority (9 & 10)	1C	R/W	(T0) 1011 1010 (T4) 1011 1010
Description	Configures the relative priority of input channels I9 and I10.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:4]	*cnfg_ref_selection_priority_10*	This 4-bit value represents the relative priority of input channel I10. The smaller the number, the higher the priority. Setting a priority of zero disables the input channel. *When the *T4_T0_select* bit in cnfg_registers_source_select =0, the priority for the T0 path is configured. When *T4_T0_select* =1, the priority for the T4 path is configured.	0000 0001 to 1111	Input channel I10 is unavailable for automatic selection. Input channel I10 priority value.	See default value above.
[3:0]	*cnfg_ref_selection_priority_9*	This 4-bit value represents the relative priority of input channel I9. The smaller the number, the higher the priority. Setting a priority of zero disables the input channel. *When the *T4_T0_select* bit in cnfg_registers_source_select =0, the priority for the T0 path is configured. When *T4_T0_select* =1, the priority for the T4 path is configured.	0000 0001 to 1111	Input channel I9 is unavailable for automatic selection. Input channel I9 priority value.	See default value above.

Configure reference selection priority register (11 & 12)

Software name	Address (0x0)	Access	Default value
cnfg_ref_selection_priority (11 & 12)	1D	R/W	(T0) 1101 1100 (T4) 0000 0000
Description	Configures the relative priority of input channels I11 and I12.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:4]	*cnfg_ref_ selection_ priority_12*	This 4-bit value represents the relative priority of input channel I12. The smaller the number, the higher the priority. Setting a priority of zero disables the input channel. *When the *T4_T0_select* bit in cnfg_registers_source_select =0, the priority for the T0 path is configured. When *T4_T0_select* =1, the priority for the T4 path is configured.	0000 0001 to 1111	Input channel I12 is unavailable for automatic selection. Input channel I12 priority value.	See default value above.
[3:0]	*cnfg_ref_ selection_ priority_11*	This 4-bit value represents the relative priority of input channel I11. The smaller the number, the higher the priority. Setting a priority of zero disables the input channel. *The priority of input channel I11 depends on the value of the MASTSLVB pin at power-up. If MASTSLVB is high (master) at power-up, then the priority defaults to input channel 11. If MASTSLVB is low (slave) at power-up, then the priority defaults to 1. *When the *T4_T0_select* bit in cnfg_registers_source_select =0, the priority for the T0 path is configured. When *T4_T0_select* =1, the priority for the T4 path is configured.	0000 0001 to 1111	Input channel I11 is unavailable for automatic selection. Input channel I11 priority value.	See default value above.

Configure reference selection priority register (13 & 14)

Software name	Address (0x0)	Access	Default value
cnfg_ref_selection_priority (13 & 14)	1E	R/W	(T0) 1111 1110 (T4) 0000 0000
Description	Configures the relative priority of input channels I13 and I14.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:4]	*cnfg_ref_ selection_ priority_14*	This 4-bit value represents the relative priority of input channel I14. The smaller the number, the higher the priority. Setting a priority of zero disables the input channel. *When the *T4_T0_select* bit in cnfg_registers_source_select = 0, the priority for the T0 path is configured. When *T4_T0_select* = 1, the priority for the T4 path is configured.	0000 0001 to 1111	Input channel I14 is unavailable for automatic selection. Input channel I14 priority value.	See default value above.
[3:0]	*cnfg_ref_ selection_ priority_13*	This 4-bit value represents the relative priority of input channel I13. The smaller the number, the higher the priority. Setting a priority of zero disables the input channel. *When the *T4_T0_select* bit in cnfg_registers_source_select =0, the priority for the T0 path is configured. When *T4_T0_select* =1, the priority for the T4 path is configured.	0000 0001 to 1111	Input channel I13 is unavailable for automatic selection. Input channel I13 priority value.	See default value above.

Configure Ethernet frequency register

Software name	Address (0x0)	Access	Default value
cnfg_enet_freq	20	R/W	0000 0000
Description	Register to enable Ethernet frequencies on outputs TO1 to TO6.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7]	*enet_2k_ enable*	Enables or disables sync2k alignment of Ethernet clocks.	0 1	Sync2k alignment disabled. Sync2k alignment enabled.	0
[6]	*enet_PLL_ enable*	Enables or disables Ethernet frequencies on the PLL.	0 1	Ethernet frequencies PLL enabled. Ethernet frequencies PLL disabled.	0
[5]	*TO6_enet*	Enables or disables Ethernet frequencies on output TO6.	0 1	TO6 output is a non-Ethernet frequency, as described in the cnfg_output_frequency (TO5 & TO6) register. TO6 output is Ethernet derived, as described in the cnfg_output_frequency (TO5 & TO6) register.	0
[4]	*TO5_enet*	Enables or disables Ethernet frequencies on output TO5.	0 1	TO6 output is a non-Ethernet frequency, as described in the cnfg_output_frequency (TO5 & TO6) register. TO6 output is Ethernet derived, as described in the cnfg_output_frequency (TO5 & TO6) register.	0
[3]	*TO4_enet*	Enables or disables Ethernet frequencies on output TO4.	0 1	TO6 output is a non-Ethernet frequency, as described in the cnfg_output_frequency (TO3 & TO4) register. TO6 output is Ethernet derived, as described in the cnfg_output_frequency (TO3 & TO4) register.	0
[2]	*TO3_enet*	Enables or disables Ethernet frequencies on output TO3.	0 1	TO6 output is a non-Ethernet frequency, as described in the cnfg_output_frequency (TO3 & TO4) register. TO6 output is Ethernet derived, as described in the cnfg_output_frequency (TO3 & TO4) register.	0

continued ...

Configure Ethernet frequency register (continued)

Bit	Bit name	Bit description	Value	Bit settings	Reset
[1]	*TO2_enet*	Enables or disables Ethernet frequencies on output TO2.	0 1	TO6 output is a non-Ethernet frequency, as described in the cnfg_output_frequency (TO1 & TO2) register. TO6 output is Ethernet derived, as described in the cnfg_output_frequency (TO1 & TO2) register.	0
[0]	*TO1_enet*	Enables or disables Ethernet frequencies on output TO1.	0 1	TO6 output is a non-Ethernet frequency, as described in the cnfg_output_frequency (TO1 & TO2) register. TO6 output is Ethernet derived, as described in the cnfg_output_frequency (TO1 & TO2) register.	0

Configure reference source frequency 2 register

Software name	Address (0x0)	Access	Default value
cnfg_ref_source_frequency_2	21	R/W	0000 0000
Description	Configuration of the frequency and input monitoring for input channel I2.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:6]		Set to 0	00	Set to 0	00
[5:4]	*bucket_id_2*	Each input channel has its own leaky bucket accumulator, which is used for activity monitoring. There are four possible configurations for each leaky bucket - see register cnfg_upper_threshold_0 to cnfg_decay_rate_3. This 2-bit field selects the configuration used for input channel I2.	00 01 10 11	Input channel I2 activity monitor uses leaky bucket configuration 0. Input channel I2 activity monitor uses leaky bucket configuration 1. Input channel I2 activity monitor uses leaky bucket configuration 2. Input channel I2 activity monitor uses leaky bucket configuration 3.	00
[3:0]		Set to 0.	0000	Set to 0.	0000

Configure reference source frequency 3 register

Software name			Address (0x0)	Access	Default value
cnfg_ref_source_frequency_3			22	RW	0000 0000
Description	Configuration of the frequency and input monitoring for input channel I3.				

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*divn_3*	This bit selects whether input channel I3 is routed through the programmable pre-divider before being input to the DPLL and frequency monitor - see cnfg_freq_divn [7:0] and cnfg_freq_divn [13:8].	0 1	Input channel I3 is fed directly to the DPLL and monitor. Input channel I3 is fed to the DPLL and monitor via the pre-divider.	0
6	*lock8k_3*	This bit selects whether input channel I3 is routed through the preset pre-divider before being input to the DPLL. The preset divider reduces the input frequency to 8 kHz, which means that the DPLL input is 8 kHz. This bit is ignored when *divn_3* is set (bit =1).	0 1	Input channel I3 is fed directly to the DPLL. Input channel I3 is fed to the DPLL via the preset pre-divider.	0
[5:4]	*bucket_id_3*	Each input channel has its own leaky bucket accumulator, which is used for activity monitoring. There are four possible configurations for each leaky bucket - see register cnfg_upper_threshold_0 to cnfg_decay_rate_3. This 2-bit field selects the configuration used for input channel I3.	00 01 10 11	Input channel I3 activity monitor uses leaky bucket configuration 0. Input channel I3 activity monitor uses leaky bucket configuration 1. Input channel I3 activity monitor uses leaky bucket configuration 2. Input channel I3 activity monitor uses leaky bucket configuration 3.	00
[3:0]	*reference_source_frequency_3*	Programs the frequency of the reference source that is connected to input channel I3. If *divn_3* is set, then this value should be set to 0000 (8 kHz).	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1111	8 kHz. 1544/2048 kHz (depends on the ip_sonsdhb bit in the cnfg_input_mode register.) 6.48 MHz. 19.44 MHz. 25.92 MHz. 38.88 MHz. 51.84 MHz. 77.76 MHz. 155.52 MHz. 2 kHz. 4 kHz. Not used. Not used.	0000

Configure reference source frequency 4 register

Software name	Address (0x0)	Access	Default value
cnfg_ref_source_frequency_4	23	RW	0000 0000
Description	Configuration of the frequency and input monitoring for input channel I4.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*divn_4*	This bit selects whether input channel I4 is routed through the programmable pre-divider before being input to the DPLL and frequency monitor - see the cnfg_freq_divn [7:0] and cnfg_freq_divn [13:8] registers.	0 1	Input channel I4 is fed directly to the DPLL and monitor. Input channel I4 is fed to the DPLL and monitor via the pre-divider.	0
6	*lock8k_4*	This bit selects whether input channel I4 is routed through the preset pre-divider before being input to the DPLL. The preset divider reduces the input frequency to 8 kHz, which means that the DPLL input is 8 kHz. This bit is ignored when *divn_4* is set (bit =1).	0 1	Input channel I4 is fed directly to the DPLL. Input channel I4 is fed to the DPLL via the preset pre-divider.	0
[5:4]	*bucket_id_4*	Each input channel has its own leaky bucket accumulator, which is used for activity monitoring. There are four possible configurations for each leaky bucket - see register cnfg_upper_threshold_0 to cnfg_decay_rate_3. This 2-bit field selects the configuration used for input channel I4.	00 01 10 11	Input channel I4 activity monitor uses leaky bucket configuration 0. Input channel I4 activity monitor uses leaky bucket configuration 1. Input channel I4 activity monitor uses leaky bucket configuration 2. Input channel I4 activity monitor uses leaky bucket configuration 3.	00
[3:0]	*reference_ source_ frequency_4*	Programs the frequency of the reference source that is connected to input channel I4. If *divn_4* is set, then this value should be set to 0000 (8 kHz).	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1111	8 kHz. 1544/2048 kHz (depends on the *ip_sonsdhb* bit in the cnfg_input_mode register.) 6.48 MHz. 19.44 MHz. 25.92 MHz. 38.88 MHz. 51.84 MHz. 77.76 MHz. 155.52 MHz. 2 kHz. 4 kHz. Not used. Not used.	0000

Configure reference source frequency 5 register

Software name	Address (0x0)	Access	Default value
cnfg_ref_source_frequency_5	24	RW	0000 0011
Description	Configuration of the frequency and input monitoring for input channel I5.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*divn_5*	This bit selects whether input channel I5 is routed through the programmable pre-divider before being input to the DPLL and frequency monitor - see the cnfg_freq_divn [7:0] and cnfg_freq_divn [13:8] registers.	0 1	Input channel I5 is fed directly to the DPLL and monitor. Input channel I5 fed to the DPLL and monitor via the pre-divider.	0
6	*lock8k_5*	This bit selects whether input channel I5 is routed through the preset pre-divider before being input to the DPLL. The preset divider reduces the input frequency to 8 kHz, which means that the DPLL input is 8 kHz. This bit is ignored when *divn_5* is set (bit =1).	0 1	Input channel I5 is fed directly to the DPLL. Input channel I5 is fed to the DPLL via the preset pre-divider.	0
[5:4]	*bucket_id_5*	Each input channel has its own leaky bucket accumulator, which is used for activity monitoring. There are four possible configurations for each leaky bucket - see register cnfg_upper_threshold_0 to cnfg_decay_rate_3. This 2-bit field selects the configuration used for input channel I5.	00 01 10 11	Input channel I5 activity monitor uses leaky bucket configuration 0. Input channel I5 activity monitor uses leaky bucket configuration 1. Input channel I5 activity monitor uses leaky bucket configuration 2. Input channel I5 activity monitor uses leaky bucket configuration 3.	00
[3:0]	*reference_ source_ frequency_5*	Programs the frequency of the reference source that is connected to input channel I5. If *divn_5* is set, then this value should be set to 0000 (8 kHz).	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1111	8 kHz. 1544/2048 kHz (depends on the *ip_sonsdhb* bit in the cnfg_input_mode register.) 6.48 MHz. 19.44 MHz. 25.92 MHz. 38.88 MHz. 51.84 MHz. 77.76 MHz. 155.52 MHz. 2 kHz. 4 kHz. Not used. Not used.	0011

Configure reference source frequency 6 register

Software name	Address (0x0)	Access	Default value
cnfg_ref_source_frequency_6	25	RW	0000 0011
Description	Configuration of the frequency and input monitoring for input channel I6.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*divn_6*	This bit selects whether input channel I6 is routed through the programmable pre-divider before being input to the DPLL and frequency monitor - see the cnfg_freq_divn [7:0] and cnfg_freq_divn [13:8] registers.	0 1	Input channel I6 is fed directly to the DPLL and monitor. Input channel I6 is fed to the DPLL and monitor via the pre-divider.	0
6	*lock8k_6*	This bit selects whether input channel I6 is routed through the preset pre-divider before being input to the DPLL. The preset divider reduces the input frequency to 8 kHz, which means that the DPLL input is 8 kHz. This bit is ignored when *divn_6* is set (bit =1).	0 1	Input channel I6 is fed directly to the DPLL. Input channel I6 is fed to the DPLL via the preset pre-divider.	0
[5:4]	*bucket_id_6*	Each input channel has its own leaky bucket accumulator, which is used for activity monitoring. There are four possible configurations for each leaky bucket - see register cnfg_upper_threshold_0 to cnfg_decay_rate_3. This 2-bit field selects the configuration used for input channel I6.	00 01 10 11	Input channel I6 activity monitor uses leaky bucket configuration 0. Input channel I6 activity monitor uses leaky bucket configuration 1. Input channel I6 activity monitor uses leaky bucket configuration 2. Input channel I6 activity monitor uses leaky bucket configuration 3.	00
[3:0]	*reference_ source_ frequency_6*	Programs the frequency of the reference source that is connected to input channel I6. If *divn_6* is set, then this value should be set to 0000 (8 kHz).	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1111	8 kHz. 1544/2048 kHz (depends on the *ip_sonsdhb* bit in the cnfg_input_mode register.) 6.48 MHz. 19.44 MHz. 25.92 MHz. 38.88 MHz. 51.84 MHz. 77.76 MHz. 155.52 MHz. 2 kHz. 4 kHz. Not used. Not used.	0011

Configure reference source frequency 7 register

Software name		Address (0x0)	Access	Default value
cnfg_ref_source_frequency_7		26	RW	0000 0011
Description	Configuration of the frequency and input monitoring for input channel I7.			

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*divn_7*	This bit selects whether input channel I7 is routed through the programmable pre-divider before being input to the DPLL and frequency monitor - see the cnfg_freq_divn [7:0] and cnfg_freq_divn [13:8] registers.	0 1	Input channel I7 is fed directly to the DPLL and monitor. Input channel I7 is fed to the DPLL and monitor via the pre-divider.	0
6	*lock8k_7*	This bit selects whether input channel I7 is routed through the preset pre-divider before being input to the DPLL. The preset divider reduces the input frequency to 8 kHz, which means that the DPLL input is 8 kHz. This bit is ignored when *divn_7* is set (bit =1).	0 1	Input channel I7 is fed directly to the DPLL. Input channel I7 is fed to the DPLL via the preset pre-divider.	0
[5:4]	*bucket_id_7*	Each input channel has its own leaky bucket accumulator, which is used for activity monitoring. There are four possible configurations for each leaky bucket - see register cnfg_upper_threshold_0 to cnfg_decay_rate_3. This 2-bit field selects the configuration used for input channel I7.	00 01 10 11	Input channel I7 activity monitor uses leaky bucket configuration 0. Input channel I7 activity monitor uses leaky bucket configuration 1. Input channel I7 activity monitor uses leaky bucket configuration 2. Input channel I7 activity monitor uses leaky bucket configuration 3.	00
[3:0]	*reference_ source_ frequency_7*	Programs the frequency of the reference source that is connected to input channel I7. If *divn_7* is set, then this value should be set to 0000 (8 kHz).	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1111	8 kHz. 1544/2048 kHz (depends on the *ip_sonsdhb* bit in the cnfg_input_mode register.) 6.48 MHz. 19.44 MHz. 25.92 MHz. 38.88 MHz. 51.84 MHz. 77.76 MHz. 155.52 MHz. 2 kHz. 4 kHz. Not used. Not used.	0011

Configure reference source frequency 8 register

Software name	Address (0x0)	Access	Default value
cnfg_ref_source_frequency_8	27	RW	0000 0011
Description	Configuration of the frequency and input monitoring for input channel I8.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*divn_8*	This bit selects whether input channel I8 is routed through the programmable pre-divider before being input to the DPLL and frequency monitor - see the cnfg_freq_divn [7:0] and cnfg_freq_divn [13:8] registers.	0 1	Input channel I8 is fed directly to the DPLL and monitor. Input channel I8 is fed to the DPLL and monitor via the pre-divider.	0
6	*lock8k_8*	This bit selects whether input channel I8 is routed through the preset pre-divider before being input to the DPLL. The preset divider reduces the input frequency to 8 kHz, which means that the DPLL input is 8 kHz. This bit is ignored when *divn_8* is set (bit =1).	0 1	Input channel I8 is fed directly to the DPLL. Input channel I8 is fed to the DPLL via the preset pre-divider.	0
[5:4]	*bucket_id_8*	Each input channel has its own leaky bucket accumulator, which is used for activity monitoring. There are four possible configurations for each leaky bucket - see register cnfg_upper_threshold_0 to cnfg_decay_rate_3. This 2-bit field selects the configuration used for input channel I8.	00 01 10 11	Input channel I8 activity monitor uses leaky bucket configuration 0. Input channel I8 activity monitor uses leaky bucket configuration 1. Input channel I8 activity monitor uses leaky bucket configuration 2. Input channel I8 activity monitor uses leaky bucket configuration 3.	00
[3:0]	*reference_ source_ frequency_8*	Programs the frequency of the reference source that is connected to input channel I8. If *divn_8* is set, then this value should be set to 0000 (8 kHz).	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1111	8 kHz. 1544/2048 kHz (depends on the *ip_sonsdhb* bit in the cnfg_input_mode register.) 6.48 MHz. 19.44 MHz. 25.92 MHz. 38.88 MHz. 51.84 MHz. 77.76 MHz. 155.52 MHz. 2 kHz. 4 kHz. Not used. Not used.	0011

Configure reference source frequency 9 register

Software name	Address (0x0)	Access	Default value
cnfg_ref_source_frequency_9	28	RW	0000 0011
Description	Configuration of the frequency and input monitoring for input channel I9.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*divn_9*	This bit selects whether input channel I9 is routed through the programmable pre-divider before being input to the DPLL and frequency monitor - see the cnfg_freq_divn [7:0] and cnfg_freq_divn [13:8] registers.	0 1	Input channel I9 is fed directly to the DPLL and monitor. Input channel I9 is fed to the DPLL and monitor via the pre-divider.	0
6	*lock8k_9*	This bit selects whether input channel I9 is routed through the preset pre-divider before being input to the DPLL. The preset divider reduces the input frequency to 8 kHz, which means that the DPLL input is 8 kHz. This bit is ignored when *divn_9* is set (bit =1).	0 1	Input channel I9 is fed directly to the DPLL. Input channel I9 is fed to the DPLL via the preset pre-divider.	0
[5:4]	*bucket_id_9*	Each input channel has its own leaky bucket accumulator, which is used for activity monitoring. There are four possible configurations for each leaky bucket - see register cnfg_upper_threshold_0 to cnfg_decay_rate_3. This 2-bit field selects the configuration used for input channel I9.	00 01 10 11	Input channel I9 activity monitor uses leaky bucket configuration 0. Input channel I9 activity monitor uses leaky bucket configuration 1. Input channel I9 activity monitor uses leaky bucket configuration 2. Input channel I9 activity monitor uses leaky bucket configuration 3.	00
[3:0]	*reference_ source_ frequency_9*	Programs the frequency of the reference source that is connected to input channel I9. If *divn_9* is set, then this value should be set to 0000 (8 kHz).	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1111	8 kHz. 1544/2048 kHz (depends on the *ip_sonsdhb* bit in the cnfg_input_mode register.) 6.48 MHz. 19.44 MHz. 25.92 MHz. 38.88 MHz. 51.84 MHz. 77.76 MHz. 155.52 MHz. 2 kHz. 4 kHz. Not used. Not used.	0011

Configure reference source frequency 10 register

Software name	Address (0x0)	Access	Default value
cnfg_ref_source_frequency_10	29	RW	0000 0011
Description	Configuration of the frequency and input monitoring for input channel I10.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*divn_10*	This bit selects whether input channel I10 is routed through the programmable pre-divider before being input to the DPLL and frequency monitor - see the cnfg_freq_divn [7:0] and cnfg_freq_divn [13:8] registers.	0 1	Input channel I10 is fed directly to the DPLL and monitor. Input channel I10 is fed to the DPLL and monitor via the pre-divider.	0
6	*lock8k_10*	This bit selects whether input channel I10 is routed through the preset pre-divider before being input to the DPLL. The preset divider reduces the input frequency to 8 kHz, which means that the DPLL input is 8 kHz. This bit is ignored when *divn_10* is set (bit =1).	0 1	Input channel I10 is fed directly to the DPLL. Input channel I10 is fed to the DPLL via the preset pre-divider.	0
[5:4]	*bucket_id_10*	Each input channel has its own leaky bucket accumulator, which is used for activity monitoring. There are four possible configurations for each leaky bucket - see register cnfg_upper_threshold_0 to cnfg_decay_rate_3. This 2-bit field selects the configuration used for input channel I10.	00 01 10 11	Input channel I10 activity monitor uses leaky bucket configuration 0. Input channel I10 activity monitor uses leaky bucket configuration 1. Input channel I10 activity monitor uses leaky bucket configuration 2. Input channel I10 activity monitor uses leaky bucket configuration 3.	00
[3:0]	*reference_ source_ frequency_10*	Programs the frequency of the reference source that is connected to input channel I10. If *divn_10* is set, then this value should be set to 0000 (8 kHz).	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1111	8 kHz. 1544/2048 kHz (depends on the *ip_sonsdhb* bit in the cnfg_input_mode register.) 6.48 MHz. 19.44 MHz. 25.92 MHz. 38.88 MHz. 51.84 MHz. 77.76 MHz. 155.52 MHz. 2 kHz. 4 kHz. Not used. Not used.	0011

Configure reference source frequency 11 register

Software name	Address (0x0)	Access	Default value
cnfg_ref_source_frequency_11	2A	RW	0000 0011
Description	Configuration of the frequency and input monitoring for input channel I11.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*divn_11*	This bit selects whether input channel I11 is routed through the programmable pre-divider before being input to the DPLL and frequency monitor- see the cnfg_freq_divn [7:0] and cnfg_freq_divn [13:8] registers.	0 1	Input channel I11 is fed directly to the DPLL and monitor. Input channel I11 is fed to the DPLL and monitor via the pre-divider.	0
6	*lock8k_11*	This bit selects whether input channel I11 is routed through the preset pre-divider before being input to the DPLL. The preset divider reduces the input frequency to 8 kHz, which means that the DPLL input is 8 kHz. This bit is ignored when *divn_11* is set (bit =1).	0 1	Input channel I11 is fed directly to the DPLL. Input channel I11 is fed to the DPLL via the preset pre-divider.	0
[5:4]	*bucket_id_11*	Each input channel has its own leaky bucket accumulator, which is used for activity monitoring. There are four possible configurations for each leaky bucket - see register cnfg_upper_threshold_0 to cnfg_decay_rate_3. This 2-bit field selects the configuration used for input channel I11.	00 01 10 11	Input channel I11 activity monitor uses leaky bucket configuration 0. Input channel I11 activity monitor uses leaky bucket configuration 1. Input channel I11 activity monitor uses leaky bucket configuration 2. Input channel I11 activity monitor uses leaky bucket configuration 3.	00
[3:0]	*reference_ source_ frequency_11*	Programs the frequency of the reference source that is connected to input channel I11. If *divn_11* is set, then this value should be set to 0000 (8 kHz).	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1111	8 kHz. 1544/2048 kHz (depends on the *ip_sonsdhb* bit in the cnfg_input_mode register.) 6.48 MHz. 19.44 MHz. 25.92 MHz. 38.88 MHz. 51.84 MHz. 77.76 MHz. 155.52 MHz. 2 kHz. 4 kHz. Not used. Not used.	0011

Configure reference source frequency 12 register

Software name	Address (0x0)	Access	Default value
cnfg_ref_source_frequency_12	2B	RW	0000 0001
Description	Configuration of the frequency and input monitoring for input channel I12.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*divn_12*	This bit selects whether input channel I12 is routed through the programmable pre-divider before being input to the DPLL and frequency monitor - see the cnfg_freq_divn [7:0] and cnfg_freq_divn [13:8] registers.	0 1	Input channel I12 is fed directly to the DPLL and monitor. Input channel I12 is fed to the DPLL and monitor via the pre-divider.	0
6	*lock8k_12*	This bit selects whether input channel I12 is routed through the preset pre-divider before being input to the DPLL. The preset divider reduces the input frequency to 8 kHz, which means that the DPLL input is 8 kHz. This bit is ignored when *divn_12* is set (bit =1).	0 1	Input channel I12 is fed directly to the DPLL. Input channel I12 is fed to the DPLL via the preset pre-divider.	0
[5:4]	*bucket_id_12*	Each input channel has its own leaky bucket accumulator, which is used for activity monitoring. There are four possible configurations for each leaky bucket - see register cnfg_upper_threshold_0 to cnfg_decay_rate_3. This 2-bit field selects the configuration used for input channel I12.	00 01 10 11	Input channel I12 activity monitor uses leaky bucket configuration 0. Input channel I12 activity monitor uses leaky bucket configuration 1. Input channel I12 activity monitor uses leaky bucket configuration 2. Input channel I12 activity monitor uses leaky bucket configuration 3.	00
[3:0]	*reference_ source_ frequency_12*	Programs the frequency of the reference source that is connected to input channel I12. If *divn_12* is set, then this value should be set to 0000 (8 kHz).	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1111	8 kHz. 1544/2048 kHz (depends on the *ip_sonsdhb* bit in the cnfg_input_mode register.) 6.48 MHz. 19.44 MHz. 25.92 MHz. 38.88 MHz. 51.84 MHz. 77.76 MHz. 155.52 MHz. 2 kHz. 4 kHz. Not used. Not used.	0001

Configure reference source frequency 13 register

Software name	Address (0x0)	Access	Default value
cnfg_ref_source_frequency_13	2C	RW	0000 0001
Description	Configuration of the frequency and input monitoring for input channel I3.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*divn_13*	This bit selects whether input channel I13 is routed through the programmable pre-divider before being input to the DPLL and frequency monito r- see the cnfg_freq_divn [7:0] and cnfg_freq_divn [13:8] registers.	0 1	Input channel I13 is fed directly to the DPLL and monitor. Input channel I13 is fed to the DPLL and monitor via the pre-divider.	0
6	*lock8k_13*	This bit selects whether input channel I13 is routed through the preset pre-divider before being input to the DPLL. The preset divider reduces the input frequency to 8 kHz, which means that the DPLL input is 8 kHz. This bit is ignored when *divn_13* is set (bit =1).	0 1	Input channel I13 is fed directly to the DPLL. Input channel I13 is fed to the DPLL via the preset pre-divider.	0
[5:4]	*bucket_id_13*	Each input channel has its own leaky bucket accumulator, which is used for activity monitoring. There are four possible configurations for each leaky bucket - see register cnfg_upper_threshold_0 to cnfg_decay_rate_3. This 2-bit field selects the configuration used for input channel I13.	00 01 10 11	Input channel I13 activity monitor uses leaky bucket configuration 0. Input channel I13 activity monitor uses leaky bucket configuration 1. Input channel I13 activity monitor uses leaky bucket configuration 2. Input channel I13 activity monitor uses leaky bucket configuration 3.	00
[3:0]	*reference_source_frequency_13*	Programs the frequency of the reference source that is connected to input channel I13. If *divn_13* is set, then this value should be set to 0000 (8 kHz).	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1111	8 kHz. 1544/2048 kHz (depends on the *ip_sonsdhb* bit in the cnfg_input_mode register.) 6.48 MHz. 19.44 MHz. 25.92 MHz. 38.88 MHz. 51.84 MHz. 77.76 MHz. 155.52 MHz. 2 kHz. 4 kHz. Not used. Not used.	0001

Configure reference source frequency 14 register

Software name	Address (0x0)	Access	Default value
cnfg_ref_source_frequency_14	2D	RW	0000 0001
Description	Configuration of the frequency and input monitoring for input channel I14.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*divn_14*	This bit selects whether input channel I14 is routed through the programmable pre-divider before being input to the DPLL and frequency monitor - see the cnfg_freq_divn [7:0] and cnfg_freq_divn [13:8] registers.	0 1	Input channel I14 is fed directly to the DPLL and monitor. Input channel I14 is fed to the DPLL and monitor via the pre-divider.	0
6	*lock8k_14*	This bit selects whether input channel I14 is routed through the preset pre-divider before being input to the DPLL. The preset divider reduces the input frequency to 8 kHz, which means that the DPLL input is 8 kHz. This bit is ignored when *divn_14* is set (bit =1).	0 1	Input channel I14 is fed directly to the DPLL. Input channel I14 is fed to the DPLL via the preset pre-divider.	0
[5:4]	*bucket_id_14*	Each input channel has its own leaky bucket accumulator, which is used for activity monitoring. There are four possible configurations for each leaky bucket - see register cnfg_upper_threshold_0 to cnfg_decay_rate_3. This 2-bit field selects the configuration used for input channel I14.	00 01 10 11	Input channel I14 activity monitor uses leaky bucket configuration 0. Input channel I14 activity monitor uses leaky bucket configuration 1. Input channel I14 activity monitor uses leaky bucket configuration 2. Input channel I14 activity monitor uses leaky bucket configuration 3.	00
[3:0]	*reference_ source_ frequency_14*	Programs the frequency of the reference source that is connected to input channel I14. If *divn_14* is set, then this value should be set to 0000 (8 kHz).	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1111	8 kHz. 1544/2048 kHz (depends on the *ip_sonsdhb* bit in the cnfg_input_mode register.) 6.48 MHz. 19.44 MHz. 25.92 MHz. 38.88 MHz. 51.84 MHz. 77.76 MHz. 155.52 MHz. 2 kHz. 4 kHz. Not used. Not used.	0001

Configure STS remote sources valid register [7:0]

Software name	Address (0x0)	Access	Default value
cnfg_sts_remote_sources_valid [I8:I1]	30	RW	1111 1111
Description	Bits [7:0] of the remote sources valid register. This register is used to disable input channels that another device has deemed invalid. The other device is usually half of a master/slave redundancy pair.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*I8*	Bit enabling input channel I8 to be prioritized as a reference source. If this bit =0, then input channel I8 does not appear in the priority table, even if it is valid (registers STS priority table register [7:0] and STS priority table register [15:8]).	0 1	Locking to input channel I8 disallowed. Locking to input channel I8 allowed.	1
6	*I7*	Bit enabling input channel I7 to be prioritized as a reference source. If this bit =0, then input channel I7 does not appear in the priority table, even if it is valid (registers STS priority table register [7:0] and STS priority table register [15:8]).	0 1	Locking to input channel I7 disallowed. Locking to input channel I7 allowed.	1
5	*I6*	Bit enabling input channel I6 to be prioritized as a reference source. If this bit =0, then input channel I6 does not appear in the priority table, even if it is valid (registers STS priority table register [7:0] and STS priority table register [15:8]).	0 1	Locking to input channel I6 disallowed. Locking to input channel I6 allowed.	1
4	*I5*	Bit enabling input channel I5 to be prioritized as a reference source. If this bit =0, then input channel I5 does not appear in the priority table, even if it is valid (registers STS priority table register [7:0] and STS priority table register [15:8]).	0 1	Locking to input channel I5 disallowed. Locking to input channel I5 allowed.	1
3	*I4*	Bit enabling input channel I4 to be prioritized as a reference source. If this bit =0, then input channel I4 does not appear in the priority table, even if it is valid (registers STS priority table register [7:0] and STS priority table register [15:8]).	0 1	Locking to input channel I4 disallowed. Locking to input channel I4 allowed.	1
2	*I3*	Bit enabling input channel I3 to be prioritized as a reference source. If this bit =0, then input channel I3 does not appear in the priority table, even if it is valid (registers STS priority table register [7:0] and STS priority table register [15:8]).	0 1	Locking to input channel I3 disallowed. Locking to input channel I3 allowed.	1
1	*I2*	Bit enabling input channel I2 to be prioritized as a reference source. If this bit =0, then input channel I2 does not appear in the priority table, even if it is valid (registers STS priority table register [7:0] and STS priority table register [15:8]).	0 1	Locking to input channel I2 disallowed. Locking to input channel I2 allowed.	1
0	*I1*	Bit enabling input channel I1 to be prioritized as a reference source. If this bit =0, then input channel I1 does not appear in the priority table, even if it is valid (registers STS priority table register [7:0] and STS priority table register [15:8]).	0 1	Locking to input channel I1 disallowed. Locking to input channel I1 allowed.	1

Configure STS remote sources valid register [13:8]

Software name	Address (0x0)	Access	Default value
cnfg_sts_remote_sources_valid [I14:I9]	31	RW	0011 1111
Description	Bits [13:8] of the remote sources valid register. This register is used to disable input channels that another device has deemed invalid. The other device is usually half of a master / slave redundancy pair.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:6]	*Not used*	Not used.	-	-	-
5	*I14*	Bit enabling input channel I14 to be prioritized as a reference source. If this bit =0, then input channel I14 does not appear in the priority table, even if it is valid (registers STS priority table register [7:0] and STS priority table register [15:8]).	0 1	Locking to input channel I14 disallowed. Locking to input channel I14 allowed.	1
4	*I13*	Bit enabling input channel I13 to be prioritized as a reference source. If this bit =0, then input channel I13 does not appear in the priority table, even if it is valid (registers STS priority table register [7:0] and STS priority table register [15:8]).	0 1	Locking to input channel I13 disallowed. Locking to input channel I13 allowed.	1
3	*I12*	Bit enabling input channel I12 to be prioritized as a reference source. If this bit =0, then input channel I12 does not appear in the priority table, even if it is valid (registers STS priority table register [7:0] and STS priority table register [15:8]).	0 1	Locking to input channel I12 disallowed. Locking to input channel I12 allowed.	1
2	*I11*	Bit enabling input channel I11 to be prioritized as a reference source. If this bit =0, then input channel I11 does not appear in the priority table, even if it is valid (registers STS priority table register [7:0] and STS priority table register [15:8]).	0 1	Locking to input channel I11 disallowed. Locking to input channel I11 allowed.	1
1	*I10*	Bit enabling input channel I10 to be prioritized as a reference source. If this bit =0, then input channel I10 does not appear in the priority table, even if it is valid (registers STS priority table register [7:0] and STS priority table register [15:8]).	0 1	Locking to input channel I10 disallowed. Locking to input channel I10 allowed.	1
0	*I9*	Bit enabling input channel I9 to be prioritized as a reference source. If this bit =0, then input channel I9 does not appear in the priority table, even if it is valid (registers STS priority table register [7:0] and STS priority table register [15:8]).	0 1	Locking to input channel I9 disallowed. Locking to input channel I9 allowed.	1

Configure operating mode register

Software name	Address (0x0)	Access	Default value
cnfg_operating_mode	32	R/W	0000 0000
Description	Register to force the state of the T0 DPLL controlling state machine.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:3]	*Not used*	Not used.	-	-	-
[2:0]	*T0_DPLL_ operating_ mode*	This field is used to control the state of the internal finite state machine controlling the T0 DPLL. A value of zero is used to allow the finite state machine to control itself. Any other value forces the state machine to jump into that state. Care should be taken when forcing the state machine. While it is forced, the internal monitoring functions cannot affect the internal state machine, therefore the user is responsible for all monitoring and control functions required to achieve the desired functionality.	000 001 010 011 100 101 110 111	Automatic (internal state machine controlled). Free run mode. Holdover mode. Not used. Locked mode. Pre-locked2 mode. Pre-locked mode. Phase lost mode.	000

Force select reference source register

Software name	Address (0x0)	Access	Default value
force_select_reference_source	33	R/W	0000 1111
Description	Register used to force the selection of a particular reference source for the T0 DPLL.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:4]	*Not used*	Not used.	-	-	0
[3:0]	*forced_ reference_ source*	Value representing the source to be selected by the T0 DPLL. A value of 0x0 leaves the selection to the automatic control mechanism within the device. Forcing an input channel to be selected bypasses all the input monitoring functions. If the device is not in the locked state, then it progresses to the locked state in the usual manner. If the input channel fails, the device does not change state to holdover because it is not allowed to disqualify the source. The effect of this register is simply to raise the priority of the selected input channel to "1" (highest). To ensure selection of the programmed input channel under all circumstances, revertive mode should be enabled (the reversion_mode bit in the cnfg_input_mode register set =1).	0000	Automatic state machine source selection.	1111
			0001	T0 DPLL forced to select input channel I1.	
			0010	T0 DPLL forced to select input channel I2.	
			0011	T0 DPLL forced to select input channel I3.	
			0100	T0 DPLL forced to select input channel I4.	
			0101	T0 DPLL forced to select input channel I5.	
			0110	T0 DPLL forced to select input channel I6.	
			0111	T0 DPLL forced to select input channel I7.	
			1000	T0 DPLL forced to select input channel I8.	
			1001	T0 DPLL forced to select input channel I9.	
			1010	T0 DPLL forced to select input channel I10.	
			1011	T0 DPLL forced to select input channel I11.	
			1100	T0 DPLL forced to select input channel I12.	
			1101	T0 DPLL forced to select input channel I13.	
			1110	T0 DPLL forced to select input channel I14.	
			1111	Not used.	

Configure input mode register

Software name	Address (0x0)	Access	Default value
cnfg_input_mode	34	(Bit 1 RO, otherwise R/W)	1100 0010*
Description	Register controlling various input modes of the device.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*auto_extsync_en*	The external sync reference can only be associated with a particular input reference. Enabling this bit allows the external frame sync input to be automatically enabled, when T0 DPLL is locked to that particular reference source. The reference source that triggers the automatic frame sync input is defined in the *Sync_reference_source* bits in the cnfg_sync_monitor register.	0 1	The external frame sync input is disabled. The external frame sync input is automatically enabled only if T0 DPLL is locked to the specified source, and bit *extsync_en* =1.	1
6	*phalarm_timeout*	This bit enables the automatic time-out facility on phase alarms. When this feature is enabled, a phase alarm on any source is automatically cancelled after 128 seconds.	0 1	Phase alarms on sources can only be cancelled by software. Phase alarms on sources cancel automatically after 128 seconds.	1
5	*XO_edge*	This bit allows either the rising edge or the falling edge of the local oscillator, connected to the REFCLK pin, to be selected for reference. The faster of the two edges should be selected for optimum jitter performance.	0 1	Device uses the rising edge of the external oscillator. Device uses the falling edge of the external oscillator.	0
4	*man_holdover*	Bit to select whether or not the holdover frequency is taken directly from registers cnfg_holdover_frequency [7:0], cnfg_holdover_frequency [15:8] and cnfg_holdover_modes. If this bit is set then it overrides any other holdover control bits.	0 1	Holdover frequency is determined automatically. Holdover frequency is taken from the *cnfg_holdover_frequency* registers.	0
3	*extsync_en*[1]	Bit to reset the PLL used to generate Synchronous Ethernet spot frequencies	0 1	SyncE PLL normal running. Reset SyncE PLL.	0
2	*ip_sonsdhb*	This bit sets the network type to be either SONET or SDH. This is useful because SONET and SDH use different default frequencies. This bit only has an effect if bit pattern 0001 (bin) is set in the appropriate input frequency register (cnfg_ref_source_frequency_2 to cnfg_ref_source_frequency_14), when the input frequency is either 1544 kHz or 2048 kHz. This bit also affects the SONET/SDH output on T09 when the *T4_op_from_T0* bit in the cnfg_T4_path register =0. Also refer to the description of the *T4_op_SONSDH* bit in the cnfg_T4_DPLL_frequency register. *The default value of this bit is determined by the state of the SONSDHB pin at power-up.	0 1	SDH network. The input frequency registers should be set to 0001 and the input frequency should be 2048 kHz. SONET network. The input frequency registers should be set to 0001 and the input frequency should be 1544 kHz.	0

1. If the EPLL is disabled after start-up, and subsequently re-enabled, the extsync_en bit must be manually toggled to ensure Ethernet frequencies on any output.

continued...

Configure input mode register (continued)

Bit	Bit name	Bit description	Value	Bit settings	Reset
1	*master_slaveb*	This read only bit reflects the state of the MSTSLVB pin. If software control over master/slave status is required, set the MSTSLVB pin to the master state at all times. Master or slave functionality can then be set by programming individual registers.	0 1	Slave state. Input channel I11 is set to the highest priority value. T0 DPLL is set to acquisition bandwidth. Revertive mode is enabled. Phase build-out is disabled. These settings override any register values. Master state. Input channel I11 priority, T0 DPLL bandwidth, revertive mode, phase build-out are all set by the respective register values.	1
0	*reversion_mode*	Bit to select either revertive or non-revertive mode. When in revertive mode, the device always selects the highest priority valid input source. When in non-revertive mode, the device maintains the currently selected source, even if a higher priority source is available, unless the current source fails.	0 1	Non-revertive mode. Revertive mode.	0

Configure T4 path register

Software name	Address (0x0)	Access	Default value
cnfg_T4_path	35	R/W	0100 0000
Description	Register to configure the input channels and other features in the T4 path.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*lock_T4_to_T0*	Bit selects whether the T4 DPLL uses its own independent inputs or locks to the T0 DPLL.	0 1	T4 path locks independently from the T0 path. T4 DPLL locks to the output of the T0 DPLL.	0
6	*T4_dig_ feedback*	Bit to select digital or analog feedback mode for the T4 DPLL.	0 1	T4 DPLL in analog feedback mode. T4 DPLL in digital feedback mode.	1
5	*Not used*	Not used.	-	-	0
4	*T4_op_from_T0*	Bit selects whether the T08 and T09 outputs are generated from the T0 DPLL or the T4 DPLL.	0 1	T08 and T09 are generated from T4 DPLL. T08 and T09 are generated from T0 DPLL.	0
[3:0]	*T4_forced_ reference_ source*	This field can be used to force the T4 DPLL to select a particular input channel. A value of zero in this field allows the T4 input to be selected automatically via the usual priority and input monitoring functions.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	T4 DPLL automatic source selection. T4 DPLL forced to select input channel I1. T4 DPLL forced to select input channel I2. T4 DPLL forced to select input channel I3. T4 DPLL forced to select input channel I4. T4 DPLL forced to select input channel I5. T4 DPLL forced to select input channel I6. T4 DPLL forced to select input channel I7. T4 DPLL forced to select input channel I8. T4 DPLL forced to select input channel I9. T4 DPLL forced to select input channel I10. T4 DPLL forced to select input channel I11. T4 DPLL forced to select input channel I12. T4 DPLL forced to select input channel I13. T4 DPLL forced to select input channel I14. Not used.	0000

Configure differential inputs register

Software name	Address (0x0)	Access	Default value
cnfg_differential_inputs	36	R/W	0000 0101
Description	Configures the differential input channels to be LVPECL or LVDS type inputs.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:2]	*Not used*	Not used.	-	-	0000 01
1	*I6_LVPECL*	Configures the I6 input channel to be compatible with either 3 V LVDS or 3 V LVPECL electrical levels.	0 1	I6 input channel LVDS compatible. I6 input channel LVPECL compatible (default).	0
0	*I5_LVDS*	Configures the I5 input channel to be compatible with either 3 V LVDS or 3 V LVPECL electrical levels.	0 1	I5 input channel LVDS compatible (default). I5 input channel LVPECL compatible.	1

Configure UPSEL device pins register

Software name	Address (0x0)	Access	Default value
cnfg_uPsel_pins	37	RO	0000 0101*
Description	Register reflecting the value on the UPSEL device pins.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:3]	*Not used*	Not used.	-	-	0000 0
[2:0]	*upsel_pins_ value*	Set by DPSync code. Read only.	100		010

Configure digital outputs SONET or SDH register

Software name	Address (0x0)	Access	Default value
cnfg_dig_outputs_sonsdh	38	R/W	0001 1111*
Description	Configures *Digital1* and *Digital2* output frequencies to be SONET or SDH compatible frequencies.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*Not used*	Not used.	-	-	0
6	*dig2_sonsdh*	Selects whether the frequencies generated by the *Digital2* frequency generator are SONET or SDH derived. *The default value of this bit is set by the SONSDHB pin at power-up.	0 1	*Digital2* can be selected from 2048/4096/8192/16384 kHz (SDH). *Digital2* can be selected from 1544/3088/6176/12352 kHz (SONET).	0
5	*dig1_sonsdh*	Selects whether the frequencies generated by the *Digital1* frequency generator are SONET or SDH derived. *The default value of this bit is set by the SONSDHB pin at power-up.	0 1	*Digital1* can be selected from 2048/4096/8192/16384 kHz (SDH). *Digital1* can be selected from 1544/3088/6176/12352 kHz (SONET).	0
[4:0]	*Not used*	Not used.	-	-	11111

Configure digital frequencies register

Software name	Address (0x0)	Access	Default value
cnfg_digital_frequencies	39	R/W	0000 1000
Description	Configures the actual frequencies of *Digital1* & *Digital2.*		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:6]	*digital2_ frequency*	Configures the frequency of *Digital2*, in conjunction with the *dig2_sonsdh* bit in the cnfg_dig_outputs_sonsdh register. If *dig2_sonsdh* =1, then the first frequency in each set is selected. If *dig2_sonsdh* =0, then the second frequency in each set is selected. For example, if *dig2_sonsdh* =0 and this field is =10, a frequency of 8192 kHz is selected.	00 01 10 11	*Digital2* set to 1544 kHz or 2048 kHz. *Digital2* set to 3088 kHz or 4096 kHz. *Digital2* set to 6176 kHz or 8192 kHz. *Digital2* set to 12353 kHz or 16384 kHz.	00
[5:4]	*digital1_ frequency*	Configures the frequency of *Digital1*, in conjunction with the *dig1_sonsdh* bit in the cnfg_dig_outputs_sonsdh register. If *dig1_sonsdh* =1, then the first frequency in each set is selected. If *dig1_sonsdh* =0, then the second frequency in each set is selected. For example, if *dig1_sonsdh* =0 and this field is =10, a frequency of 8192 kHz is selected.	00 01 10 11	*Digital1* set to 1544 kHz or 2048 kHz. *Digital1* set to 3088 kHz or 4096 kHz. *Digital1* set to 6176 kHz or 8192 kHz. *Digital1* set to 12353 kHz or 16384 kHz.	00
[3:0]	*Not used*	Not used.	-	-	1111

Configure differential outputs register

Software name	Address (0x0)	Access	Default value
cnfg_differential_outputs	3A	R/W	1100 0110
Description	Configures the electrical compatibility of the differential output drivers to be 3 V LVPECL or 3 V LVDS.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:4]	*Not used*	Not used.	-	-	1100
[3:2]	*TO7_LVPECL_ LVDS*	Selection of the electrical compatibility of TO7 between 3 V LVPECL and 3 V LVDS.	00 01 10 11	Output TO7 is disabled. Output TO7 3 V LVPECL compatible. Output TO7 3 V LVDS compatible. Not used.	01
[1:0]	*TO6_LVDS_ LVPECL*	Selection of the electrical compatibility of TO6 between 3 V LVPECL and 3 V LVDS.	00 01 10 11	Output TO6 is disabled. Output TO6 3 V LVPECL compatible. Output TO6 3 V LVDS compatible. Not used.	10

Configure automatic bandwidth selection register

Software name	Address (0x0)	Access	Default value
cnfg_auto_bw_sel	3B	R/W	1111 1011
Description	Register to select automatic bandwidth selection for the T0 DPLL path.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*auto_BW_sel*	Bit to select locked bandwidth (register cnfg_T0_DPLL_locked_bw) or acquisition bandwidth (cnfg_T0_DPLL_acq_bw) for the T0 DPLL.	0 1	Always selects locked bandwidth. Automatically selects either locked or acquisition bandwidth, as appropriate.	1
[6:4]	*Not used*	Not used.	-	-	111
3	*T0_lim_int*	This bit allows the integral path value of the T0 DPLL to be limited, or frozen, when the DPLL reaches either its minimum or maximum frequency. Freezing the integral path value can be used to minimize subsequent overshoot when the DPLL is pulling in. Note that when the integral path value is frozen, the reported frequency value in the sts_current_DPLL_frequency [7:0], sts_current_DPLL_frequency [15:8] and sts_current_DPLL_frequency [18:16] registers is also frozen.	0 1	DPLL integral path is not frozen. DPLL integral path value is frozen if the T0 DPLL hits its minimum or maximum frequency limit.	1
[2:0]	*Not used*	Not used.	-	-	011

Configure nominal frequency register [7:0]

Software name	Address (0x0)	Access	Default value
cnfg_nominal_frequency [7:0]	3C	R/W	1001 1001
Description	Bits [7:0] of the register used to calibrate the crystal oscillator that is used to clock the device.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*cnfg_nominal_ frequency_ value[7:0]*	See register description of the cnfg_nominal_frequency [15:8] register.			1001 1001

Configure nominal frequency register [15:8]

Software name	Address (0x0)	Access	Default value
cnfg_nominal_frequency [15:8]	3D	R/W	1001 1001
Description	Bits [15:8] of the register used to calibrate the crystal oscillator that is used to clock the device.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*cnfg_nominal_ frequency_ value[15:8]*	This register is used in conjunction with the cnfg_nominal_frequency [7:0] register to offset the frequency of the crystal oscillator over the range +514 ppm and –771 ppm. The default value represents 0 ppm offset from the reference clock. This value is an unsigned integer. The value in cnfg_nominal_frequency [7:0] & cnfg_nominal_frequency [15:8] is used within the DPLL to offset the frequency value used in the DPLL only. This means that the value programmed affects the value reported in the sts_current_DPLL_frequency [7:0], sts_current_DPLL_frequency [15:8] & sts_current_DPLL_frequency [18:16] registers. It also affects the value programmed into *holdover_frequency_value* in the cnfg_holdover_frequency [7:0] & cnfg_holdover_frequency [15:8] registers, and the DPLL frequency offset limit programmed into the cnfg_DPLL_freq_limit [7:0] & cnfg_DPLL_freq_limit [9:8] registers. However, this “calibrated” frequency is NOT used in the frequency monitors affecting the cnfg_freq_mon_threshold, cnfg_current_freq_mon_threshold, sts_freq_measurement & cnfg_DPLL_soft_limit registers, which all use the un-calibrated crystal frequency. The frequency monitors can also be configured to use the clock from the output of the DPLL by programming the *freq_mon_clk* bit in the cnfg_monitors register.	-	In order to program the ppm offset of the crystal oscillator frequency, concatenate the values in the cnfg_nominal_frequency [7:0] & cnfg_nominal_frequency [15:8] registers. This value is an unsigned integer. The combined value in these registers, should be multiplied by 0.0196229 dec, and then the default value (39321 dec) subtracted, to give the absolute offset value in ppm. For example, assume the combined value in the two registers is 2,500,000. The absolute offset value is- 49057.25 - 39321 = +9736.25 ppm.	1001 1001

Configure holdover frequency register [7:0]

Software name	Address (0x0)	Access	Default value
cnfg_holdover_frequency [7:0]	3E	R/W	0000 0000
Description	Bits [7:0] of the manual holdover frequency register.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*holdover_ frequency_ value[7:0]*	See the cnfg_holdover_frequency [15:8] register for details.			0000 0000

Configure holdover frequency register [15:8]

Software name	Address (0x0)	Access	Default value
cnfg_holdover_frequency [15:8]	3F	R/W	0000 0000
Description	Bits [15:8] of the manual holdover frequency register.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*holdover_ frequency_ value[15:8]*	This value in this register is combined with the value in the cnfg_holdover_frequency [7:0] register and the *holdover_frequency_value[15:8]* bits of the cnfg_holdover_modes register to represent the programmed holdover frequency of the T0 DPLL. This register is designed such that software can read the *sts_current_DPLL_frequency* register (registers sts_current_DPLL_frequency [7:0], sts_current_DPLL_frequency [15:8] & sts_current_DPLL_frequency [18:16],) and filter the value. The result is then in a suitable format to write back to the *cnfg_holdover_frequency* register. *This register can be programmed to read back the internally averaged holdover frequency rather than the programmed value. See the *read_average* bit in the cnfg_holdover_modes register.		In order to calculate the holdover ppm offset of the DPLL with respect to the crystal oscillator frequency, concatenate the value in the cnfg_holdover_frequency [7:0] register and the *holdover_frequency_value[15:8]* bits in the cnfg_holdover_modes register. This value is a 2's complement signed integer. This combined value, multiplied by 0.0003068 dec, gives the value in ppm.	0000 0000

Configure holdover modes register

Software name	Address (0x0)	Access	Default value
cnfg_holdover_modes	40	R/W	1000 1000
Description	Register to control the holdover modes of the T0 DPLL.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*auto_averaging*	Bit to enable the use of the averaged frequency value during holdover. This bit is overridden by the *man_holdover* bit in the cnfg_input_mode register.	0 1	Averaged frequency is not used. The holdover frequency is either set manually, or is frozen at its instantaneous value. Averaged frequency is used, providing that manual holdover mode is not enabled.	1
6	*fast_averaging*	Bit to control the rate of averaging of the holdover frequency. Slow averaging gives a -3db response point of approximately 110 minutes. Fast averaging gives a -3db response point of approximately 8 minutes.	0 1	Slow holdover frequency averaging is enabled. Fast holdover frequency averaging is enabled.	0
5	*read_average*	Bit to control whether the value read from the cnfg_holdover_frequency [7:0] and cnfg_holdover_frequency [15:8] registers is the value written to that register, or the averaged holdover frequency. This allows the software to use the internal averager as part of the holdover algorithm. For optimum performance, use manual holdover mode and calculate the holdover frequency in software.	0 1	The value read from the cnfg_holdover_frequency [7:0] and cnfg_holdover_frequency [15:8] registers is the value written to them. The value read from cnfg_holdover_frequency [7:0] and cnfg_holdover_frequency [15:8] registers is either the fast or slow averaged frequency, as determined by the *fast_averaging* bit.	0
[4:3]	*mini_holdover_ mode*	Mini-holdover is a term used to describe the state of the DPLL when it is in locked mode, but it has temporarily lost its input. This may be a temporary state, or last for many seconds while an input is checked for inactivity. The DPLL behaves exactly as if it were in holdover mode. This field defines how the mini-holdover frequency is determined. The descriptions of these frequency determining methods is the same as for holdover mode.	00 01 10 11	The mini-holdover frequency is determined in the same way as for full holdover mode. The mini-holdover frequency is frozen instantaneously. The mini-holdover frequency is taken from the fast averager. The mini-holdover frequency is taken from the slow averager.	01
[2:0]	*holdover_ frequency_ value [18:16]*	See register cnfg_holdover_frequency [15:8] for details.			000

Configure DPLL frequency limit register [7:0]

Software name	Address (0x0)	Access	Default value
cnfg_DPLL_freq_limit [7:0]	41	R/W	0111 0110
Description	Bits [7:0] of the DPLL frequency limit register.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*DPLL_freq_limit _value[7:0]*	This register defines the frequency offset limit for both the T0 and the T4 DPLL, compared to the calibrated frequency of the local oscillator. If either DPLL tracks a source whose frequency drifts beyond this value, the DPLL frequency limits. This value also represents the pull-in range of the DPLLs. This offset limit is the frequency offset of the DPLL when compared to the offset of the external crystal oscillator clocking the device. If the oscillator is calibrated using the cnfg_nominal_frequency [7:0] & cnfg_nominal_frequency [15:8] registers, then this calibration is automatically taken into account.	-	In order to calculate the frequency limit in ppm, concatenate the *DPLL_freq_limit_value[9:8]* bits of the cnfg_DPLL_freq_limit [9:8] register and the *DPLL_freq_limit_value[7:0]* bits of the cnfg_DPLL_freq_limit [7:0] register. This combined value is a unsigned integer and should be multiplied by 0.078 to give both the positive and negative limit values in ppm. For example, if the combined register values are 118 dec, the limit range is ±9.204 ppm.	0111 0110

Configure DPLL frequency limit register [9:8]

Software name	Address (0x0)	Access	Default value
cnfg_DPLL_freq_limit [9:8]	42	R/W	0000 0000
Description	Bits [9:8] of the DPLL frequency limit register.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:2]	*Not used*	Not used.	-	-	0000 00
[1:0]	*DPLL_freq_limit _value[9:8]*	See the cnfg_DPLL_freq_limit [7:0] register for details.			00

Configure interrupt mask register [7:0]

Software name			Address (0x0)	Access	Default value
cnfg_interrupt_mask [7:0]			43	R/W	0000 0000
Description	Bits [7:0] of the interrupt mask register.				

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*I8*	Mask bit for input channel I8 interrupt.	0 1	Input channel I8 cannot generate interrupts. Input channel I8 can generate interrupts.	0
6	*I7*	Mask bit for input channel I7 interrupt.	0 1	Input channel I7 cannot generate interrupts. Input channel I7 can generate interrupts.	0
5	*I6*	Mask bit for input channel I6 interrupt.	0 1	Input channel I6 cannot generate interrupts. Input channel I6 can generate interrupts.	0
4	*I5*	Mask bit for input channel I5 interrupt.	0 1	Input channel I5 cannot generate interrupts. Input channel I5 can generate interrupts.	0
3	*I4*	Mask bit for input channel I4 interrupt.	0 1	Input channel I4 cannot generate interrupts. Input channel I4 can generate interrupts.	0
2	*I3*	Mask bit for input channel I3 interrupt.	0 1	Input channel I3 cannot generate interrupts. Input channel I3 can generate interrupts.	0
1	*I2*	Mask bit for input channel I2 interrupt.	0 1	Input channel I2 cannot generate interrupts. Input channel I2 can generate interrupts.	0
0	*I1*	Mask bit for input channel I1 interrupt.	0 1	Input channel I1 cannot generate interrupts. Input channel I1 can generate interrupts.	0

Configure interrupt mask register [15:8]

Software name	Address (0x0)	Access	Default value
cnfg_interrupt_mask [15:8]	44	R/W	0100 0000
Description	Bits [15:8] of the interrupt mask register.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*operating_ mode*	Mask bit for the *operating_mode* interrupt.	0 1	Operating mode cannot generate interrupts. Operating mode can generate interrupts.	0
6	*main_ref_failed*	Mask bit for the *main_ref_failed* interrupt.	0 1	Main reference failure cannot generate interrupts. Main reference failure can generate interrupts.	1
5	*I14*	Mask bit for input channel I14 interrupt.	0 1	Input channel I14 cannot generate interrupts. Input channel I14 can generate interrupts.	0
4	*I13*	Mask bit for input channel I13 interrupt.	0 1	Input channel I13 cannot generate interrupts. Input channel I13 can generate interrupts.	0
3	*I12*	Mask bit for input channel I12 interrupt.	0 1	Input channel I12 cannot generate interrupts. Input channel I12 can generate interrupts.	0
2	*I11*	Mask bit for input channel channel I11 interrupt.	0 1	Input channel I11 cannot generate interrupts. Input channel I11 can generate interrupts.	0
1	*I10*	Mask bit for input channel I10 interrupt.	0 1	Input channel I10 cannot generate interrupts. Input channel I10 can generate interrupts.	0
0	*I9*	Mask bit for input channel I9 interrupt.	0 1	Input channel I9 cannot generate interrupts. Input channel I9 can generate interrupts.	0

Configure interrupt mask register [23:16]

Software name	Address (0x0)	Access	Default value
cnfg_interrupt_mask [23:16]	45	R/W	0000 0000
Description	Bits [23:16] of the interrupt mask register.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*Sync_ip_alarm*	Mask bit for the *Sync_ip_alarm* interrupt.	0 1	The external sync input cannot generate interrupts. The external sync input can generate interrupts.	0
6	*T4_status*	Mask bit for the *T4_status* interrupt.	0 1	A change in T4 status cannot generate interrupts. A change in T4 status can generate interrupts.	0
5	*Not used*	Not used.	-	-	0
4	*T4_inputs_ failed*	Mask bit for the *T4_inputs_failed* interrupt.	0 1	Failure of T4 inputs cannot generate interrupts. Failure of T4 inputs can generate interrupts.	0
3	*AMI2_Viol*	Mask bit for the *AMI2_Viol* interrupt.	0 1	Input channel I2 cannot generate AMI violation interrupts. Input channel I2 can generate AMI violation interrupts.	0
2	*AMI2_LOS*	Mask bit for the *AMI2_LOS* interrupt.	0 1	Input channel I2 cannot generate AMI LOS interrupts. Input channel I2 can generate AMI LOS interrupts.	0
1	*AMI1_Viol*	Mask bit for the *AMI1_Viol* interrupt.	0 1	Input channel I1 cannot generate AMI violation interrupts. Input channel I1 can generate AMI violation interrupts.	0
0	*AMI1_LOS*	Mask bit for the *AMI1_LOS* interrupt.	0 1	Input channel I1 cannot generate AMI LOS interrupts. Input channel I1 can generate AMI LOS interrupts.	0

Configure frequency division register [7:0]

Software name	Address (0x0)	Access	Default value
cnfg_freq_divn [7:0]	46	R/W	1111 1111
Description	Bits [7:0] of the division factor for input channels using the DivN feature.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*divn_value[7:0]*	See the cnfg_freq_divn [13:8] register for details.			1111 1111

Configure frequency division register [13:8]

Software name	Address (0x0)	Access	Default value
cnfg_freq_divn [13:8]	47	R/W	0011 1111
Description	Bits [13:8] of the division factor for input channels using the DivN feature.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:6]	*Not used*	Not used.	-	-	00
[5:0]	*divn_value [13:8]*	This register should be concatenated with the cnfg_freq_divn [7:0] register to obtain the integer factor to be used by the DivN pre-divider. The DivN feature supports input frequencies up to a maximum of 100 MHz. Therefore, the maximum value that should be written to this register is 30D3 hex (12499 dec). Use of higher DivN values than this may result in unreliable behavior.	-	The input frequency is divided by the value in this register plus 1. i.e. to divide the frequency by 8, program a value of 7.	1111 11

Configure monitors register

Software name		Address (0x0)	Access	Default value
cnfg_monitors		48	R/W	0000 0101
Description	Configuration register controlling several input monitoring and switching options.			

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*freq_mon_clk*	Bit to select the source of the clock for the frequency monitors. This allows the frequency monitors to be clocked by either the output clock or by the local crystal oscillator.	0 1	Frequency monitors are clocked by the output of T0 DPLL. Frequency monitors are clocked by the local crystal oscillator.	0
6	*los_flag_on_ TDO*	Bit to select whether the *main_ref_fail* interrupt from the T0 DPLL is flagged on the TDO pin. If this bit is enabled, the device no longer strictly conforms to the IEEE 1149.1 JTAG[6] standard for the function of the TDO pin. When enabled, the TDO pin simply mimics the state of the *main_ref_fail* interrupt status bit.	0 1	Normal mode, TDO complies with IEEE 1149.1. TDO pin used to indicate the state of the *main_ref_fail* interrupt status. This allows the device to generate a rapid hardware indication of a source failure.	0
5	*ultra_fast_ switch*	Bit to enable ultra-fast switching mode. When this mode is enabled, the device disqualifies the current reference source as soon as it detects a few missing input cycles.	0 1	The currently selected source is only disqualified by the activity monitors (leaky buckets) or by the frequency monitors. The currently selected source is disqualified after less than 3 missing input cycles.	0
4	*ext_switch*	This bit enables external switching mode. When in external switching mode, the device is only allowed to lock to one of a pair of sources. If the programmed priority of input I3 is non-zero and the SRCSW pin is high, the device is forced to lock to input I3, regardless of the signal present on that input. If the programmed priority of input I3 is zero, and the SRCSW pin is high, it is forced to lock to input I5 instead. If the programmed priority of input I4 is non-zero and the SRCSW pin is low, the device is forced to lock to input I4 regardless of the signal present on that input. If the programmed priority of input I4 is zero, and the SRCSW pin is low, it is forced to lock to input I6 instead. * The default value of this bit depends on the value of the SRCSWIT pin at power-up.	0 1	Normal operation mode. External source switching mode is enabled. The operating mode of the device is always forced to be locked when in this mode.	0
3	*PBO_freeze*	This bit controls the freezing of phase build-out operation. If phase build-out has been enabled and there have been some source switches, then the input-output phase relationship of the T0 DPLL is unknown. If phase build-out is no longer required, then it can be frozen. This maintains the current input-output phase relationship, but prevents further phase build-out events. The alternative is to disable phase build-out without freezing the phase. This might cause a phase shift in the output, as the T0 DPLL re-locks the phase to zero degrees.	0 1	Phase build-out is not frozen. Phase build-out is frozen. No further phase build-out events will occur.	0

continued...

Configure monitors register (continued)

Bit	Bit name	Bit description	Value	Bit settings	Reset
2	*PBO_en*	This bit enables phase build-out events on source switching. When enabled, a phase build-out event is triggered every time the T0 DPLL selects a new source. This includes exiting the holdover or free-run states.	0 1	Phase build-out is not enabled. T0 DPLL locks to zero degrees phase. Phase build-out is enabled on source switching.	1
1	*freq_monitor_ soft_enable*	This bit enables frequency monitoring of input reference sources, using soft frequency alarms.	0 1	Soft frequency monitor alarms are disabled. Soft frequency monitor alarms are enabled.	0
0	*freq_monitor_ hard_enable*	This bit enables frequency monitoring of input reference sources, using hard frequency alarms.	0 1	Hard frequency monitor alarms are disabled. Hard frequency monitor alarms are enabled.	1

Configure frequency monitor threshold register

Software name	Address (0x0)	Access	Default value
cnfg_freq_mon_threshold	49	R/W	0010 0011
Description	Register to set both the hard and soft frequency alarm limits for the monitors on the input reference sources.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:4]	*soft_frequency_ alarm_ threshold*	Threshold to trigger the soft frequency alarms in the *sts_reference_sources* registers (sts_reference_sources Input pairs (1 & 2) to sts_reference_sources Input pairs (13 & 14)). A soft alarm is only used for monitoring, and does not disqualify a source.		To calculate the alarm limit in ppm, add one to the 4-bit value in this register. Then multiply the result by 3.81 ppm. The limit is symmetrical about zero. For example, a register value of 0010 bin corresponds to an alarm limit of ±11.43 ppm.	0010
[3:0]	*hard_frequency _alarm _threshold*	Threshold to trigger the hard frequency alarms in the *sts_reference_sources* registers (sts_reference_sources Input pairs (1 & 2) to sts_reference_sources Input pairs (13 & 14)). A hard alarm disqualifies a reference source.		To calculate the limit in ppm, add one to the 4-bit value in this register. Then multiply the result by 3.81 ppm. The limit is symmetrical about zero. For example, a register value of 0011 bin corresponds to an alarm limit of ±15.24 ppm.	0011

Configure current frequency monitor threshold register

Software name	Address (0x0)	Access	Default value
cnfg_current_freq_mon_threshold	4A	R/W	0010 0011
Description	Register to set both the hard and soft frequency alarm limits for the monitors on the currently selected reference source.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:4]	*current_soft_ frequency_ alarm_ threshold*	Threshold to trigger the soft frequency alarm in the *sts_reference_sources* register that applies to the currently selected source.The currently selected source can use different soft frequency alarm limits to all other sources. A soft alarm is only used for monitoring, and does not disqualify the source.		To calculate the limit in ppm, add one to the 4-bit value in this register. Then multiply the result by 3.81 ppm. The limit is symmetrical about zero. For example, a register value of 0010 bin corresponds to an alarm limit of ±11.43 ppm.	0010
[3:0]	*current_hard_ frequency_ alarm_ threshold*	Threshold to trigger the hard frequency alarm in the *sts_reference_sources* register that applies to the currently selected source. The currently selected source can use different hard frequency alarm limits to all other sources. A hard alarm can disqualify the source.		To calculate the limit in ppm, add one to the 4-bit value in this register. Then multiply the result by 3.81 ppm. The limit is symmetrical about zero. For example, a register value of 0011 bin corresponds to an alarm limit of ±15.24 ppm.	0011

Configure registers source select register

Software name	Address (0x0)	Access	Default value
cnfg_registers_source_select	4B	R/W	0000 0000
Description	Register to select the source of many of the registers.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:5]	*Not used*	Not used.	-	-	000
4	*T4_T0_select*	Bit to select between the T0 and T4 path for the following registers: (STS priority table register [7:0] & STS priority table register [15:8]); (sts_current_DPLL_frequency [7:0], sts_current_DPLL_frequency [15:8] & sts_current_DPLL_frequency [18:16]); (cnfg_ref_selection_priority (1 & 2) to cnfg_ref_selection_priority (13 & 14)); (sts_current_phase [7:0] & sts_current_phase [15:8]).	0 1	T0 path registers selected. T4 path registers selected.	0
[3:0]	*frequency_ measurement_ channel_select*	Register to select the input channel from which the frequency measurement result in the sts_freq_measurement register is taken.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	Not used - refers to no input channel. Frequency measurement taken from input channel I1. Frequency measurement taken from input channel I2. Frequency measurement taken from input channel I3. Frequency measurement taken from input channel I4. Frequency measurement taken from input channel I5. Frequency measurement taken from input channel I6. Frequency measurement taken from input channel I7. Frequency measurement taken from input channel I8. Frequency measurement taken from input channel I9. Frequency measurement taken from input channel I10. Frequency measurement taken from input channel I11. Frequency measurement taken from input channel I12. Frequency measurement taken from input channel I13. Frequency measurement taken from input channel I14. Not used - refers to no input channel.	0000

STS frequency measurement register

Software name			Address (0x0)	Access	Default value
sts_freq_measurement			4C	R/W	0000 0000
Description	Register containing the frequency measurement result.				

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*freq_ measurement_ value*	This register represents the value of the frequency measurement performed on the channel number that is selected in the cnfg_registers_source_select register. This value represents the frequency offset between the clock and the frequency monitors. The clock can be either the crystal oscillator to the device, or the output of the T0 DPLL, and is selected by the *freq_mon_clk* bit in the cnfg_monitors register.	-	This is an 8-bit 2's complement signed integer. To calculate the measured offset in ppm of the selected input channel, multiply this value by 3.81 ppm.	0000 0000

Configure DPLL soft limit register

Software name			Address (0x0)	Access	Default value
cnfg_DPLL_soft_limit			4D	R/W	1000 1110
Description	Register to program the soft frequency limit of the two DPLLs. Exceeding this limit triggers a flag, but has no other effect.				

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*freq_lim_ph_ loss*	This bit enables the phase lost indicator when the DPLL hits its hard frequency limit. This limit is programmed in the cnfg_DPLL_freq_limit [7:0] & cnfg_DPLL_freq_limit [9:8] registers. Enabling this bit causes the DPLL to enter the phase lost state any time the DPLL frequency reaches its hard limit.	0 1	Phase lost/locked determined normally. Phase lost forced when DPLL tracks to hard limit.	1
[6:0]	*DPLL_soft_limit _value*	Threshold to trigger the soft frequency alarm (bits *T0_DPLL_freq_soft_alarm* and *T4_DPLL_freq_soft_alarm* in the sts_operating register) for either of the DPLLs. A soft alarm is only used for monitoring, and does not disqualify the source. The value programmed in this register is an offset compared to the local crystal oscillator frequency, taking into account any programmed calibration.	-	To calculate the ppm offset multiply this 7-bit value by 0.628 ppm. The limit is symmetrical about zero. For example, a value of 0001110 bin is equivalent to ±8.79 ppm.	0001 110

Configure upper threshold 0 register

Software name	Address (0x0)	Access	Default value
cnfg_upper_threshold_0	50	R/W	0000 0110
Description	Register to program the activity alarm setting limit for leaky bucket configuration 0.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*upper_ threshold_0_ value*	Each leaky bucket operates on a 128 ms cycle. If the activity monitor detects that an input has either failed or has been erratic, during a cycle, then the accumulator is incremented by 1. For each period of 1, 2, 4, or 8 cycles that the input is stable, the accumulator is decremented by 1. This decrement period is programmed in the cnfg_decay_rate_0 register. If the accumulator count reaches the programmed *upper_threshold_0_value,* the leaky bucket raises an input inactivity alarm.	-	Value at which the leaky bucket accumulator raises an inactivity alarm.	0000 0110

Configure lower threshold 0 register

Software name	Address (0x0)	Access	Default value
cnfg_lower_threshold_0	51	R/W	0000 0100
Description	Register to program the activity alarm resetting limit for leaky bucket configuration 0.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*lower_threshold _0_value*	Each leaky bucket operates on a 128 ms cycle. If the activity monitor detects that an input has either failed or has been erratic, during a cycle, then the accumulator is incremented by 1. For each period of 1, 2, 4, or 8 cycles that the input is stable, the accumulator is decremented by 1. This decrement period is programmed in the cnfg_decay_rate_0 register. If the inactivity alarm has been triggered, the alarm remains active until the value in the leaky bucket accumulator falls below this programmed *lower_threshold_0_value.* When it does so, the alarm is reset.	-	Value at which the leaky bucket accumulator resets an inactivity alarm.	0000 0100

Configure bucket size 0 register

Software name	Address (0x0)	Access	Default value
cnfg_bucket_size_0	52	R/W	0000 1000
Description	Register to program the maximum size limit for leaky bucket configuration 0.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*bucket_size_0_value*	Each leaky bucket operates on a 128 ms cycle. If the activity monitor detects that an input has either failed or has been erratic, during a cycle, then the accumulator is incremented by 1. For each period of 1, 2, 4, or 8 cycles that the input is stable, the accumulator is decremented by 1. This decrement period is programmed in the cnfg_decay_rate_0 register. The accumulator value limits when it reaches the value programmed into this register.	-	Value at which the leaky bucket accumulator stops incrementing, even with further inactive periods.	0000 1000

Configure decay rate 0 register

Software name	Address (0x0)	Access	Default value
cnfg_decay_rate_0	53	R/W	0000 0001
Description	Register to program the “decay” or “leak” rate for leaky bucket configuration 0.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:2]	*Not used*	Not used.	-	-	0000 00
[1:0]	*decay_rate_0_value*	Each leaky bucket operates on a 128 ms cycle. If the activity monitor detects that an input has either failed or has been erratic, during a cycle, then the accumulator is incremented by 1. For each period of 1, 2, 4, or 8 cycles that the input is stable, the accumulator is decremented by 1. This value programs the decrement period. Setting this value programs the accumulator to “leak” or “decay” at the same rate as the “fill” cycle, or at one half, one quarter, or one eighth of the fill rate.	00 01 10 11	Bucket decay rate of 1 every 128 ms. Bucket decay rate of 1 every 256 ms. Bucket decay rate of 1 every 512 ms. Bucket decay rate of 1 every 1024 ms.	01

Configure upper threshold 1 register

Software name	Address (0x0)	Access	Default value
cnfg_upper_threshold_1	54	R/W	0000 0110
Description	Register to program the activity alarm setting limit for leaky bucket configuration 1.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*upper_ threshold_1_ value*	Each leaky bucket operates on a 128 ms cycle. If the activity monitor detects that an input has either failed or has been erratic, during a cycle, then the accumulator is incremented by 1. For each period of 1, 2, 4, or 8 cycles that the input is stable, the accumulator is decremented by 1. This decrement period is programmed in the cnfg_decay_rate_1 register. If the accumulator count reaches the programmed *upper_threshold_1_value,* the leaky bucket raises an input inactivity alarm.	-	Value at which the leaky bucket accumulator raises an inactivity alarm.	0000 0110

Configure lower threshold 1 register

Software name	Address (0x0)	Access	Default value
cnfg_lower_threshold_1	55	R/W	0000 0100
Description	Register to program the activity alarm resetting limit for leaky bucket configuration 1.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*lower_threshold _1_value*	Each leaky bucket operates on a 128 ms cycle. If the activity monitor detects that an input has either failed or has been erratic, during a cycle, then the accumulator is incremented by 1. For each period of 1, 2, 4, or 8 cycles that the input is stable, the accumulator is decremented by 1. This decrement period is programmed in the cnfg_decay_rate_1 register. If the inactivity alarm has been triggered, the alarm remains active until the value in the leaky bucket accumulator falls below this programmed *lower_threshold_1_value.* When it does so, the alarm is reset.	-	Value at which the leaky bucket accumulator resets an inactivity alarm.	0000 0100

Configure bucket size 1 register

Software name		Address (0x0)	Access	Default value
cnfg_bucket_size_1		56	R/W	0000 1000
Description	Register to program the maximum size limit for leaky bucket configuration 1.			

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*bucket_size_1_value*	Each leaky bucket operates on a 128 ms cycle. If the activity monitor detects that an input has either failed or has been erratic, during a cycle, then the accumulator is incremented by 1. For each period of 1, 2, 4, or 8 cycles that the input is stable, the accumulator is decremented by 1. This decrement period is programmed in the cnfg_decay_rate_1 register. The accumulator value limits when it reaches the value programmed into this register.	-	Value at which the leaky bucket accumulator stops incrementing, even with further inactive periods.	0000 1000

Configure decay rate 1 register

Software name		Address (0x0)	Access	Default value
cnfg_decay_rate_1		57	R/W	0000 0001
Description	Register to program the “decay” or “leak” rate for leaky bucket configuration 1.			

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:2]	*Not used*	Not used.	-	-	0000 00
[1:0]	*decay_rate_1_value*	Each leaky bucket operates on a 128 ms cycle. If the activity monitor detects that an input has either failed or has been erratic, during a cycle, then the accumulator is incremented by 1. For each period of 1, 2, 4, or 8 cycles that the input is stable, the accumulator is decremented by 1. This value programs the decrement period. Setting this value programs the accumulator to “leak” or “decay” at the same rate as the “fill” cycle, or at one half, one quarter, or one eighth of the fill rate.	00 01 10 11	Bucket decay rate of 1 every 128 ms. Bucket decay rate of 1 every 256 ms. Bucket decay rate of 1 every 512 ms. Bucket decay rate of 1 every 1024 ms.	01

Configure upper threshold 2 register

Software name	Address (0x0)	Access	Default value
cnfg_upper_threshold_2	58	R/W	0000 0110
Description	Register to program the activity alarm setting limit for leaky bucket configuration 2.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*upper_threshold_2_value*	Each leaky bucket operates on a 128 ms cycle. If the activity monitor detects that an input has either failed or has been erratic, during a cycle, then the accumulator is incremented by 1. For each period of 1, 2, 4, or 8 cycles that the input is stable, the accumulator is decremented by 1. This decrement period is programmed in the cnfg_decay_rate_2 register. If the accumulator count reaches the programmed *upper_threshold_2_value,* the leaky bucket raises an input inactivity alarm.	-	Value at which the leaky bucket accumulator raises an inactivity alarm.	0000 0110

Configure lower threshold 2 register

Software name	Address (0x0)	Access	Default value
cnfg_lower_threshold_2	59	R/W	0000 0100
Description	Register to program the activity alarm resetting limit for leaky bucket configuration 2.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*lower_threshold_2_value*	Each leaky bucket operates on a 128 ms cycle. If the activity monitor detects that an input has either failed or has been erratic, during a cycle, then the accumulator is incremented by 1. For each period of 1, 2, 4, or 8 cycles that the input is stable, the accumulator is decremented by 1. This decrement period is programmed in the cnfg_decay_rate_2 register. If the inactivity alarm has been triggered, the alarm remains active until the value in the leaky bucket accumulator falls below this programmed *lower_threshold_2_value.* When it does so, the alarm is reset.	-	Value at which the leaky bucket accumulator resets an inactivity alarm.	0000 0100

Configure bucket size 2 register

Software name	Address (0x0)	Access	Default value
cnfg_bucket_size_2	5A	R/W	0000 1000
Description	Register to program the maximum size limit for leaky bucket configuration 2.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*bucket_size_2_value*	Each leaky bucket operates on a 128 ms cycle. If the activity monitor detects that an input has either failed or has been erratic, during a cycle, then the accumulator is incremented by 1. For each period of 1, 2, 4, or 8 cycles that the input is stable, the accumulator is decremented by 1. This decrement period is programmed in the cnfg_decay_rate_2 register. The accumulator value limits when it reaches the value programmed into this register.	-	Value at which the leaky bucket accumulator stops incrementing, even with further inactive periods.	0000 1000

Configure decay rate 2 register

Software name	Address (0x0)	Access	Default value
cnfg_decay_rate_2	5B	R/W	0000 0001
Description	Register to program the “decay” or “leak” rate for leaky bucket configuration 2.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:2]	*Not used*	Not used.	-	-	0000 00
[1:0]	*decay_rate_2_value*	Each leaky bucket operates on a 128 ms cycle. If the activity monitor detects that an input has either failed or has been erratic, during a cycle, then the accumulator is incremented by 1. For each period of 1, 2, 4, or 8 cycles that the input is stable, the accumulator is decremented by 1. This value programs the decrement period. Setting this value programs the accumulator to “leak” or “decay” at the same rate as the “fill” cycle, or at one half, one quarter, or one eighth of the fill rate.	00 01 10 11	Bucket decay rate of 1 every 128 ms. Bucket decay rate of 1 every 256 ms. Bucket decay rate of 1 every 512 ms. Bucket decay rate of 1 every 1024 ms.	01

Configure upper threshold 3 register

Software name	Address (0x0)	Access	Default value
cnfg_upper_threshold_3	5C	R/W	0000 0110
Description	Register to program the activity alarm setting limit for leaky bucket configuration 3.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*upper_threshold_3_value*	Each leaky bucket operates on a 128 ms cycle. If the activity monitor detects that an input has either failed or has been erratic, during a cycle, then the accumulator is incremented by 1. For each period of 1, 2, 4, or 8 cycles that the input is stable, the accumulator is decremented by 1. This decrement period is programmed in the cnfg_decay_rate_3 register. If the accumulator count reaches the programmed *upper_threshold_3_value,* the leaky bucket raises an input inactivity alarm.	-	Value at which the leaky bucket accumulator raises an inactivity alarm.	0000 0110

Configure lower threshold 3 register

Software name	Address (0x0)	Access	Default value
cnfg_lower_threshold_3	5D	R/W	0000 0100
Description	Register to program the activity alarm resetting limit for leaky bucket configuration 3.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*lower_threshold_3_value*	Each leaky bucket operates on a 128 ms cycle. If the activity monitor detects that an input has either failed or has been erratic, during a cycle, then the accumulator is incremented by 1. For each period of 1, 2, 4, or 8 cycles that the input is stable, the accumulator is decremented by 1. This decrement period is programmed in the cnfg_decay_rate_3 register. If the inactivity alarm has been triggered, the alarm remains active until the value in the leaky bucket accumulator falls below this programmed *lower_threshold_3_value.* When it does so, the alarm is reset.	-	Value at which the leaky bucket accumulator resets an inactivity alarm.	0000 0100

Configure bucket size 3 register

Software name	Address (0x0)	Access	Default value
cnfg_bucket_size_3	5E	R/W	0000 1000
Description	Register to program the maximum size limit for leaky bucket configuration 3.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*bucket_size_3_ value*	Each leaky bucket operates on a 128 ms cycle. If the activity monitor detects that an input has either failed or has been erratic, during a cycle, then the accumulator is incremented by 1. For each period of 1, 2, 4, or 8 cycles that the input is stable, the accumulator is decremented by 1. This decrement period is programmed in the cnfg_decay_rate_3 register. The accumulator value limits when it reaches the value programmed into this register.	-	Value at which the leaky bucket accumulator stops incrementing, even with further inactive periods.	0000 1000

Configure decay rate 3 register

Software name	Address (0x0)	Access	Default value
cnfg_decay_rate_3	5F	R/W	0000 0001
Description	Register to program the “decay” or “leak” rate for Leaky Bucket Configuration 3.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:2]	*Not used*	Not used.	-	-	0000 00
[1:0]	*decay_rate_3_ value*	Each leaky bucket operates on a 128 ms cycle. If the activity monitor detects that an input has either failed or has been erratic, during a cycle, then the accumulator is incremented by 1. For each period of 1, 2, 4, or 8 cycles that the input is stable, the accumulator is decremented by 1. This value programs the decrement period. Setting this value programs the accumulator to “leak” or “decay” at the same rate as the “fill” cycle, or at one half, one quarter, or one eighth of the fill rate.	00 01 10 11	Bucket decay rate of 1 every 128 ms. Bucket decay rate of 1 every 256 ms. Bucket decay rate of 1 every 512 ms. Bucket decay rate of 1 every 1024 ms.	01

Configure output frequency T01 & T02 register

Software name	Address (0x0)	Access	Default value
cnfg_output_frequency (TO1 & TO2)	60	R/W	1000 0101
Description	Register to configure and enable the frequencies available on outputs TO1 and TO2.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:4]	*output_freq_2*	Configuration of the output frequencies that are available at output TO2. Many of the frequencies available depend on the frequencies of the T0 APLL and the T4 APLL. These are configured in the cnfg_T4_DPLL_frequency and cnfg_T0_DPLL_frequency registers. For more detail see the section on configuring the output frequencies. Additionally, for the Ethernet frequencies 25 MHz, 50 MHz 62.5 MHz and 125 MHz, Ethernet configuration register cnfg_enet_freq (Reg. 20) must be appropriately programmed.	0000	Reg. 20[1] at 0 = output disabled Reg. 20[1] at 1 = 25 MHz Ethernet	1000
			0001	Reg. 20[1] at 0 = 2 kHz Reg. 20[1] at 1 = 50 MHz Ethernet	
			0010	Reg. 20[1] at 0 = 8 kHz Reg. 20[1] at 1 = 62.5 MHz Ethernet	
			0011	Reg. 20[1] at 0 = Digital2 (Reg. 39) Reg. 20[1] at 1 = 125 MHz Ethernet	
			0100	Reg. 20[1] at 0 = Digital1 (Reg. 39) Reg. 20[1] at 1 = 25 MHz Ethernet	
			0101	Reg. 20[1] at 0 = T0 APLL frequency/48 Reg. 20[1] at 1 = 50 MHz Ethernet	
			0110	Reg. 20[1] at 0 = T0 APLL frequency/16 Reg. 20[1] at 1 = 62.5 MHz Ethernet	
			0111	Reg. 20[1] at 0 = T0 APLL frequency/12 Reg. 20[1] at 1 = 125 MHz Ethernet	
			1000	Reg. 20[1] at 0 = T0 APLL frequency/8 Reg. 20[1] at 1 = 25 MHz Ethernet	
			1001	Reg. 20[1] at 0 = T0 APLL frequency/6 Reg. 20[1] at 1 = 50 MHz Ethernet	
			1010	Reg. 20[1] at 0 = T0 APLL frequency/4 Reg. 20[1] at 1 = 62.5 MHz Ethernet	
			1011	Reg. 20[1] at 0 = T4 APLL frequency/64 Reg. 20[1] at 1 = 125 MHz Ethernet	
			1100	Reg. 20[1] at 0 = T4 APLL frequency/48 Reg. 20[1] at 1 = 25 MHz Ethernet	
			1101	Reg. 20[1] at 0 = T4 APLL frequency/16 Reg. 20[1] at 1 = 50 MHz Ethernet	
			1110	Reg. 20[1] at 0 = T4 APLL frequency/8 Reg. 20[1] at 1 = 62.5 MHz Ethernet	
			1111	Reg. 20[1] at 0 = T4 APLL frequency/4 Reg. 20[1] at 1 = 125 MHz Ethernet	

continued...

Configure output frequency T01 & T02 register (continued)

Bit	Bit name	Bit description	Value	Bit settings	Reset
[3:0]	*output_freq_1*	Configuration of the output frequencies that are available at output T01. Many of the frequencies available depend on the frequencies of the T0 APLL and the T4 APLL. These are configured in the cnfg_T4_DPLL_frequency and cnfg_T0_DPLL_frequency registers. For more detail see the section on configuring the output frequencies. Additionally, for the Ethernet frequencies 25 MHz, 50 MHz 62.5 MHz and 125 MHz, Ethernet configuration register cnfg_enet_freq (Reg. 20) must be appropriately programmed.	0000	Reg. 20[0] at 0 = output disabled Reg. 20[0] at 1 = 25 MHz Ethernet	0101
			0001	Reg. 20[0] at 0 = 2 kHz Reg. 20[0] at 1 = 50 MHz Ethernet	
			0010	Reg. 20[0] at 0 = 8 kHz Reg. 20[0] at 1 = 62.5 MHz Ethernet	
			0011	Reg. 20[0] at 0 = Digital2 (Reg. 39) Reg. 20[0] at 1 = 125 MHz Ethernet	
			0100	Reg. 20[0] at 0 = Digital1 (Reg. 39) Reg. 20[0] at 1 = 25 MHz Ethernet	
			0101	Reg. 20[0] at 0 = T0 APLL frequency/48 Reg. 20[0] at 1 = 50 MHz Ethernet	
			0110	Reg. 20[0] at 0 = T0 APLL frequency/16 Reg. 20[0] at 1 = 62.5 MHz Ethernet	
			0111	Reg. 20[0] at 0 = T0 APLL frequency/12 Reg. 20[0] at 1 = 125 MHz Ethernet	
			1000	Reg. 20[0] at 0 = T0 APLL frequency/8 Reg. 20[0] at 1 = 25 MHz Ethernet	
			1001	Reg. 20[0] at 0 = T0 APLL frequency/6 Reg. 20[0] at 1 = 50 MHz Ethernet	
			1010	Reg. 20[0] at 0 = T0 APLL frequency/4 Reg. 20[0] at 1 = 62.5 MHz Ethernet	
			1011	Reg. 20[0] at 0 = T4 APLL frequency/64 Reg. 20[0] at 1 = 125 MHz Ethernet	
			1100	Reg. 20[0] at 0 = T4 APLL frequency/48 Reg. 20[0] at 1 = 25 MHz Ethernet	
			1101	Reg. 20[0] at 0 = T4 APLL frequency/16 Reg. 20[0] at 1 = 50 MHz Ethernet	
			1110	Reg. 20[0] at 0 = T4 APLL frequency/8 Reg. 20[0] at 1 = 62.5 MHz Ethernet	
			1111	Reg. 20[0] at 0 = T4 APLL frequency/8 Reg. 20[0] at 1 = 62.5 MHz Ethernet	

Configure output frequency T03 & T04 register

Software name	Address (0x0)	Access	Default value
cnfg_output_frequency (TO3 & TO4)	61	R/W	1000 0110
Description	Register to configure and enable the frequencies available on outputs TO3 and TO4.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:4]	*output_freq_4*	Configuration of the output frequencies that are available at output TO4. Many of the frequencies available depend on the frequencies of the T0 APLL and the T4 APLL. These are configured in the cnfg_T4_DPLL_frequency and cnfg_T0_DPLL_frequency registers. For more detail see the section on configuring the output frequencies. Additionally, for the Ethernet frequencies 25 MHz, 50 MHz 62.5 MHz and 125 MHz, Ethernet configuration register cnfg_enet_freq (Reg. 20) must be appropriately programmed.	0000	Reg. 20[3] at 0 = output disabled Reg. 20[3] at 1 = 25 MHz Ethernet	1000
			0001	Reg. 20[3] at 0 = 2 kHz Reg. 20[3] at 1 = 50 MHz Ethernet	
			0010	Reg. 20[3] at 0 = 8 kHz Reg. 20[3] at 1 = 62.5 MHz Ethernet	
			0011	Reg. 20[3] at 0 = Digital2 (Reg. 39) Reg. 20[3] at 1 = 125 MHz Ethernet	
			0100	Reg. 20[3] at 0 = Digital1 (Reg. 39) Reg. 20[3] at 1 = 25 MHz Ethernet	
			0101	Reg. 20[3] at 0 = T0 APLL frequency/48 Reg. 20[3] at 1 = 50 MHz Ethernet	
			0110	Reg. 20[3] at 0 = T0 APLL frequency/16 Reg. 20[3] at 1 = 62.5 MHz Ethernet	
			0111	Reg. 20[3] at 0 = T0 APLL frequency/12 Reg. 20[3] at 1 = 125 MHz Ethernet	
			1000	Reg. 20[3] at 0 = T0 APLL frequency/8 Reg. 20[3] at 1 = 25 MHz Ethernet	
			1001	Reg. 20[3] at 0 = T0 APLL frequency/6 Reg. 20[3] at 1 = 50 MHz Ethernet	
			1010	Reg. 20[3] at 0 = T0 APLL frequency/4 Reg. 20[3] at 1 = 62.5 MHz Ethernet	
			1011	Reg. 20[3] at 0 = T4 APLL frequency/2 Reg. 20[3] at 1 = 125 MHz Ethernet	
			1100	Reg. 20[3] at 0 = T4 APLL frequency/48 Reg. 20[3] at 1 = 25 MHz Ethernet	
			1101	Reg. 20[3] at 0 = T4 APLL frequency/16 Reg. 20[3] at 1 = 50 MHz Ethernet	
			1110	Reg. 20[3] at 0 = T4 APLL frequency/8 Reg. 20[3] at 1 = 62.5 MHz Ethernet	
			1111	Reg. 20[3] at 0 = T4 APLL frequency/4 Reg. 20[3] at 1 = 125 MHz Ethernet	

continued...

Configure output frequency T03 & T04 register (continued)

Bit	Bit name	Bit description	Value	Bit settings	Reset
[3:0]	*output_freq_3*	Configuration of the output frequencies that are available at output T03. Many of the frequencies available depend on the frequencies of the T0 APLL and the T4 APLL. These are configured in the cnfg_T4_DPLL_frequency and cnfg_T0_DPLL_frequency registers. For more detail see the section on configuring the output frequencies. Additionally, for the Ethernet frequencies 25 MHz, 50 MHz 62.5 MHz and 125 MHz, Ethernet configuration register cnfg_enet_freq (Reg. 20) must be appropriately programmed.	0000	Reg. 20[2] at 0 = output disabled Reg. 20[2] at 1 = 25 MHz Ethernet	0110
			0001	Reg. 20[2] at 0 = 2 kHz Reg. 20[2] at 1 = 50 MHz Ethernet	
			0010	Reg. 20[2] at 0 = 8 kHz Reg. 20[2] at 1 = 62.5 MHz Ethernet	
			0011	Reg. 20[2] at 0 = Digital2 (Reg. 39) Reg. 20[2] at 1 = 125 MHz Ethernet	
			0100	Reg. 20[2] at 0 = Digital1 (Reg. 39) Reg. 20[2] at 1 = 25 MHz Ethernet	
			0101	Reg. 20[2] at 0 = T0 APLL frequency/48 Reg. 20[2] at 1 = 50 MHz Ethernet	
			0110	Reg. 20[2] at 0 = T0 APLL frequency/16 Reg. 20[2] at 1 = 62.5 MHz Ethernet	
			0111	Reg. 20[2] at 0 = T0 APLL frequency/12 Reg. 20[2] at 1 = 125 MHz Ethernet	
			1000	Reg. 20[2] at 0 = T0 APLL frequency/8 Reg. 20[2] at 1 = 25 MHz Ethernet	
			1001	Reg. 20[2] at 0 = T0 APLL frequency/6 Reg. 20[2] at 1 = 50 MHz Ethernet	
			1010	Reg. 20[2] at 0 = T0 APLL frequency/4 Reg. 20[2] at 1 = 62.5 MHz Ethernet	
			1011	Reg. 20[2] at 0 = T4 APLL frequency/64 Reg. 20[2] at 1 = 125 MHz Ethernet	
			1100	Reg. 20[2] at 0 = T4 APLL frequency/48 Reg. 20[2] at 1 = 25 MHz Ethernet	
			1101	Reg. 20[2] at 0 = T4 APLL frequency/16 Reg. 20[2] at 1 = 50 MHz Ethernet	
			1110	Reg. 20[2] at 0 = T4 APLL frequency/8 Reg. 20[2] at 1 = 62.5 MHz Ethernet	
			1111	Reg. 20[2] at 0 = T4 APLL frequency/4 Reg. 20[2] at 1 = 125 MHz Ethernet	

Configure output frequency T05 & T06 register

Software name	Address (0x0)	Access	Default value
cnfg_output_frequency (TO5 & TO6)	62	R/W	1000 0101
Description	Register to configure and enable the frequencies available on outputs TO5 and TO6.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:4]	*output_freq_6*	Configuration of the output frequencies that are available at output TO6. Many of the frequencies available depend on the frequencies of the T0 APLL and the T4 APLL. These are configured in the cnfg_T4_DPLL_frequency and cnfg_T0_DPLL_frequency registers. For more detail see the section on configuring the output frequencies. Additionally, for the Ethernet frequencies 25 MHz, 50 MHz 62.5 MHz and 125 MHz, Ethernet configuration register cnfg_enet_freq (Reg. 20) must be appropriately programmed.	0000	Reg. 20[5] at 0 = output disabled Reg. 20[5] at 1 = 25 MHz Ethernet	1000
			0001	Reg. 20[5] at 0 = 2 kHz Reg. 20[5] at 1 = 50 MHz Ethernet	
			0010	Reg. 20[5] at 0 = 8 kHz Reg. 20[5] at 1 = 62.5 MHz Ethernet	
			0011	Reg. 20[5] at 0 = T0 APLL/2 Reg. 20[5] at 1 = 125 MHz Ethernet	
			0100	Reg. 20[5] at 0 = Digital1 (Reg. 39) Reg. 20[5] at 1 = 25 MHz Ethernet	
			0101	Reg. 20[5] at 0 = T0 APLL frequency/1 Reg. 20[5] at 1 = 50 MHz Ethernet	
			0110	Reg. 20[5] at 0 = T0 APLL frequency/16 Reg. 20[5] at 1 = 62.5 MHz Ethernet	
			0111	Reg. 20[5] at 0 = T0 APLL frequency/12 Reg. 20[5] at 1 = 125 MHz Ethernet	
			1000	Reg. 20[5] at 0 = T0 APLL frequency/8 Reg. 20[5] at 1 = 25 MHz Ethernet	
			1001	Reg. 20[5] at 0 = T0 APLL frequency/6 Reg. 20[5] at 1 = 50 MHz Ethernet	
			1010	Reg. 20[5] at 0 = T0 APLL frequency/4 Reg. 20[5] at 1 = 62.5 MHz Ethernet	
			1011	Reg. 20[5] at 0 = T4 APLL frequency/64 Reg. 20[5] at 1 = 125 MHz Ethernet	
			1100	Reg. 20[5] at 0 = T4 APLL frequency/48 Reg. 20[5] at 1 = 25 MHz Ethernet	
			1101	Reg. 20[5] at 0 = T4 APLL frequency/16 Reg. 20[5] at 1 = 50 MHz Ethernet	
			1110	Reg. 20[5] at 0 = T4 APLL frequency/8 Reg. 20[5] at 1 = 62.5 MHz Ethernet	
			1111	Reg. 20[5] at 0 = T4 APLL frequency/4 Reg. 20[5] at 1 = 125 MHz Ethernet	

continued...

Configure output frequency T05 & T06 register (continued)

Bit	Bit name	Bit description	Value	Bit settings	Reset
[3:0]	*output_freq_5*	Configuration of the output frequencies that are available at output T05. Many of the frequencies available depend on the frequencies of the T0 APLL and the T4 APLL. These are configured in the cnfg_T4_DPLL_frequency and cnfg_T0_DPLL_frequency registers. For more detail see the section on configuring the output frequencies. Additionally, for the Ethernet frequencies 25 MHz, 50 MHz 62.5 MHz and 125 MHz, Ethernet configuration register cnfg_enet_freq (Reg. 20) must be appropriately programmed.	0000	Reg. 20[4] at 0 = output disabled Reg. 20[4] at 1 = 25 MHz Ethernet	0101
			0001	Reg. 20[4] at 0 = 2 kHz Reg. 20[4] at 1 = 50 MHz Ethernet	
			0010	Reg. 20[4] at 0 = 8 kHz Reg. 20[4] at 1 = 62.5 MHz Ethernet	
			0011	Reg. 20[4] at 0 = Digital2 (Reg. 39) Reg. 20[4] at 1 = 125 MHz Ethernet	
			0100	Reg. 20[4] at 0 = Digital1 (Reg. 39) Reg. 20[4] at 1 = 25 MHz Ethernet	
			0101	Reg. 20[4] at 0 = T0 APLL frequency/48 Reg. 20[4] at 1 = 50 MHz Ethernet	
			0110	Reg. 20[4] at 0 = T0 APLL frequency/16 Reg. 20[4] at 1 = 62.5 MHz Ethernet	
			0111	Reg. 20[4] at 0 = T0 APLL frequency/12 Reg. 20[4] at 1 = 125 MHz Ethernet	
			1000	Reg. 20[4] at 0 = T0 APLL frequency/8 Reg. 20[4] at 1 = 25 MHz Ethernet	
			1001	Reg. 20[4] at 0 = T0 APLL frequency/6 Reg. 20[4] at 1 = 50 MHz Ethernet	
			1010	Reg. 20[4] at 0 = T0 APLL frequency/4 Reg. 20[4] at 1 = 62.5 MHz Ethernet	
			1011	Reg. 20[4] at 0 = T4 APLL frequency/64 Reg. 20[4] at 1 = 125 MHz Ethernet	
			1100	Reg. 20[4] at 0 = T4 APLL frequency/48 Reg. 20[4] at 1 = 25 MHz Ethernet	
			1101	Reg. 20[4] at 0 = T4 APLL frequency/16 Reg. 20[4] at 1 = 50 MHz Ethernet	
			1110	Reg. 20[4] at 0 = T4 APLL frequency/8 Reg. 20[4] at 1 = 62.5 MHz Ethernet	
			1111	Reg. 20[4] at 0 = T4 APLL frequency/4 Reg. 20[4] at 1 = 125 MHz Ethernet	

Configure output frequency TO7 to TO11 register

Software name	Address (0x0)	Access	Default value
cnfg_output_frequency (TO7 to TO11)	63	R/W	1111 0110
Description	Register to configure and enable the frequencies available on outputs TO7 through to TO11.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*MFrSyncen*	Register bit to enable the 2 kHz sync output (TO11).	0 1	Output TO11 disabled. Output TO11 enabled.	1
6	*FrSyncen*	Register bit to enable the 8 kHz sync output (TO10).	0 1	Output TO10 disabled. Output TO10 enabled.	1
5	*TO9_en*	Register bit to enable the BITS output from the TO9 output.	0 1	Output TO9 disabled. Output TO9 enabled.	1
4	*TO8_en*	Register bit to enable the AMI composite clock output from the TO8 output.	0 1	Output TO8 disabled. Output TO8 enabled.	1
[3:0]	*output_freq_7*	Configuration of the output frequency available at output TO7. Many of the frequencies available depend on the frequencies of the T0 APLL and the T4 APLL. These are configured in registers cnfg_T4_DPLL_frequency and cnfg_T0_DPLL_frequency. For more detail see the detailed section on configuring the output frequencies.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	Output disabled. 2 kHz. 8 kHz. Digital2 (cnfg_digital_frequencies). T0 APLL frequency/2. T0 APLL frequency/48. T0 APLL frequency/16. T0 APLL frequency/12. T0 APLL frequency/8. T0 APLL frequency/6. T0 APLL frequency/4. T4 APLL frequency/64. T4 APLL frequency/48. T4 APLL frequency/16. T4 APLL frequency/8. T4 APLL frequency/4.	0110

Configure T4 DPLL frequency register

Software name	Address (0x0)	Access	Default value
cnfg_T4_DPLL_frequency	64	R/W	0000 0001
Description	Register to configure the T4 DPLL and several other parameters for the T4 path.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*Not used*	Not used.	-	-	0
6	*Auto_squelch_ T4*	Register bit to automatically squelch the T4 outputs on TO8 and TO9 when the T4 inputs have failed.	0 1	Outputs TO8 and TO9 enabled as in the cnfg_output_frequency (TO7 to TO11) register. Outputs TO8 and TO9 disabled when T4 inputs fail.	0
5	*AMI_duty_ cycle*	Register bit to configure whether the composite clock output of TO8 is 50:50 or 5:8 duty cycle.	0 1	TO8 output 50:50 duty cycle. TO8 output 5:8 duty cycle.	0
4	*T4_op_ SONSDH*	Register bit to configure the BITS output on TO9 to be either SONET or SDH frequency. This bit only has an effect when the *T4_op_from_T0* bit in the cnfg_T4_path register= 0. If *T4_op_from_T0* =1 then SONET/SDH selection for TO9 is controlled by the *ip_sonsdhb* bit in the cnfg_input_mode register. The default value of this bit is set by the SONSDHB pin at reset, as is the default value of the *ip_sonsdhb* bit in the cnfg_input_mode register.	0 1	TO9 output is 2.048 MHz (SDH). TO9 output is 1.544 MHz (SONET).	0
3	*Not used*	Not used.	-	-	0

continued...

Configure T4 DPLL frequency register (continued)

Bit	Bit name	Bit description	Value	Bit settings	Reset
[2:0]	*T4_DPLL_ frequency*	Register to configure the frequency of operation of the DPLL in the T4 path. The frequency of the DPLL also affects the frequency of the T4 APLL which, in turn, affects the frequencies available at outputs TO1 - TO7. See registers cnfg_output_frequency (TO1 & TO2) to cnfg_output_frequency (TO7 to TO11) for more details. It is also possible to run the T4 APLL directly from the T0 DPLL output, see the *T4_APLL_for_T0* bit in the cnfg_T0_DPLL_frequency register. In this scenario T4 DPLL is not used but it should not be squelched if any frequencies are required from the T4 APLL. Squelching the T4 DPLL also squelches the T4 APLL input, causing the T4 APLL to free run.	000	T4 DPLL mode = squelched (clock off).	001
			001	T4 DPLL mode = 77.76 MHz (OC-N rates), giving T4 APLL output frequency (before dividers) = 311.04 MHz.	
			010	T4 DPLL mode = 12E1, giving T4 APLL output frequency (before dividers) = 98.304 MHz.	
			011	T4 DPLL mode = 16E1, giving T4 APLL output frequency (before dividers) = 131.072 MHz.	
			100	T4 DPLL mode = 24DS1, giving T4 APLL output frequency (before dividers) = 148.224 MHz.	
			101	T4 DPLL mode = 16DS1, giving T4 APLL output frequency (before dividers) = 98.816 MHz.	
			110	T4 DPLL mode = E3, giving T4 APLL output frequency (before dividers) = 274.944 MHz.	
			111	T4 DPLL mode = DS3, giving T4 APLL output frequency (before dividers) = 178.944 MHz.	

Configure T0 DPLL frequency register

Software name	Address (0x0)	Access	Default value
cnfg_T0_DPLL_frequency	65	R/W	0000 0001
Description	Register to configure the T0 DPLL and several other parameters for the T0 path.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*T4_meas_T0_ph*	Register bit to allow the T4 path to measure phase offset from the T0 path. When this bit is enabled, the T4 path is disabled and the phase detector is used to measure the phase between the input to the T0 DPLL and the selected T4 input.	0 1	Normal- T4 Path normal operation. T4 DPLL is disabled and the T4 phase detector is used to measure the phase between the selected T0 input and the selected T4 input.	0
6	*T4_APLL_for_T0*	Register bit to select whether the T4 APLL takes its input from the T4 DPLL or the T0 DPLL. If the T0 DPLL is selected then the frequency is controlled by the *T0_freq_to_T4_APLL* bits in this register.	0 1	T4 APLL takes its input from the T4 DPLL. T4 APLL takes its input from the T0 DPLL.	0
[5:4]	*T0_freq_to_T4_APLL*	If the *T4_APLL_for_T0* bit in this register is set, T4 APLL takes its input from the T0 DPLL. This register sets the multiplied output frequency from the T0 LF output DFS in this scenario. *Note that this is not the operating frequency of the T0 DPLL itself - which is fixed at 77.76 MHz (see Figure 29).	00 01 10 11	T0 DPLL mode = 12E1, giving T4 APLL output frequency (before dividers) = 98.304 MHz. T0 DPLL mode = 16E1, giving T4 APLL output frequency (before dividers) = 131.072 MHz. T0 DPLL mode = 24DS1, giving T4 APLL output frequency (before dividers) = 148.224 MHz. T0 DPLL mode = 16DS1, giving T4 APLL output frequency (before dividers) = 98.816 MHz.	00
3	*Not used*	Not used.	-	-	0

continued...

Configure T0 DPLL frequency register (continued)

Bit	Bit name	Bit description	Value	Bit settings	Reset
[2:0]	*T0_DPLL_ frequency*	This register configures the frequency output to the T0 APLL when T0 DPLL is configured to be its input source. Consequently this register also configures the APLL output frequency in the T0 path. This register affects the frequencies available at TO1 - TO7 see registers cnfg_output_frequency (TO1 & TO2) to cnfg_output_frequency (TO7 to TO11). *Note that this register does not set the operating frequency of the T0 DPLL itself - which is fixed at 77.76 MHz. It sets the frequency of the multiplied output from the LF Output DFS block (see Figure 29).	000 001 010 011 100 101 110 111	T0 DPLL mode = 77.76 MHz, digital feedback, T0 APLL output frequency (before dividers) = 311.04 MHz. T0 DPLL mode = 77.76 MHz, analog feedback, T0 APLL output frequency (before dividers) = 311.04 MHz. T0 DPLL mode = 12E1, giving T0 APLL output frequency (before dividers) = 98.304 MHz. T0 DPLL mode = 16E1, giving T0 APLL output frequency (before dividers) = 131.072 MHz. T0 DPLL mode = 24DS1, giving T0 APLL output frequency (before dividers) = 148.224 MHz. T0 DPLL mode = 16DS1, giving T0 APLL output frequency (before dividers) = 98.816 MHz. Not used. Not used.	001

Configure T4 DPLL bandwidth register

Software name	Address (0x0)	Access	Default value
cnfg_T4_DPLL_bw	66	R/W	0000 0000
Description	Register to configure the bandwidth of the T4 DPLL.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:2]	*Not used*	Not used.	-	-	000 000
[1:0]	*T4_DPLL_ bandwidth*	Register to configure the bandwidth of the T4 DPLL.	00 01 10 11	T4 DPLL 18 Hz bandwidth. T4 DPLL 35 Hz bandwidth. T4 DPLL 70 Hz bandwidth. Not used.	00

Configure T0 DPLL locked bandwidth register

Software name	Address (0x0)	Access	Default value
cnfg_T0_DPLL_locked_bw	67	R/W	0000 1011
Description	Register to configure the bandwidth of the T0 DPLL, when it is phase locked to an input.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:5]	*Not used*	Not used.	-	-	000
[4:0]	*T0_DPLL_ locked_ bandwidth*	This register configures the bandwidth of the T0 DPLL when it is locked to an input reference. If the *auto_BW_sel* bit in the cnfg_auto_bw_sel register is set =0, this bandwidth value is used all the time. If the *auto_BW_sel* bit in the cnfg_auto_bw_sel register is set =1, this bandwidth value is automatically selected when the DPLL is locked to an input.	00000 00001 00010 00011 00100 00101 00110 00111 01000 01001 01010 01011 01100 01101 01110 01111 10000 10001 All other values	T0 DPLL 0.5 mHz locked bandwidth. T0 DPLL 1mHz locked bandwidth. T0 DPLL 2 mHz locked bandwidth. T0 DPLL 4 mHz locked bandwidth. T0 DPLL 8 mHz locked bandwidth. T0 DPLL 15 mHz locked bandwidth. T0 DPLL 30 mHz locked bandwidth. T0 DPLL 60 mHz locked bandwidth. T0 DPLL 0.1 Hz locked bandwidth. T0 DPLL 0.3 Hz locked bandwidth. T0 DPLL 0.6 Hz locked bandwidth. T0 DPLL 1.2 Hz locked bandwidth. T0 DPLL 2.5 Hz locked bandwidth. T0 DPLL 4 Hz locked bandwidth. T0 DPLL 8 Hz locked bandwidth. T0 DPLL 18 Hz locked bandwidth. T0 DPLL 35 Hz locked bandwidth. T0 DPLL 70 Hz locked bandwidth. Not used.	01011

Configure T0 DPLL acquisition bandwidth register

Software name	Address (0x0)	Access	Default value
cnfg_T0_DPLL_acq_bw	69	R/W	0000 1111
Description	Register to configure the bandwidth of the T0 DPLL, when it is not phase locked to an input.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:4]	*Not used*	Not used.	-	-	000
[4:0]	*T0_DPLL_ acquisition_ bandwidth*	Register to configure the bandwidth of the T0 DPLL when acquiring phase lock on an input reference. This value is only used if the *auto_BW_sel* bit in the cnfg_auto_bw_sel register is set =1.	00000	T0 DPLL 0.5 mHz acquisition bandwidth.	01111
			00001	T0 DPLL 1 mHz acquisition bandwidth.	
			00010	T0 DPLL 2 mHz acquisition bandwidth.	
			00011	T0 DPLL 4 mHz acquisition bandwidth.	
			00100	T0 DPLL 8 mHz acquisition bandwidth.	
			00101	T0 DPLL 15 mHz acquisition bandwidth.	
			00110	T0 DPLL 30 mHz acquisition bandwidth.	
			00111	T0 DPLL 60 mHz acquisition bandwidth.	
			01000	T0 DPLL 0.1 Hz acquisition bandwidth.	
			01001	T0 DPLL 0.3 Hz acquisition bandwidth.	
			01011	T0 DPLL 1.2 Hz acquisition bandwidth.	
			01100	T0 DPLL 2.5 Hz acquisition bandwidth.	
			01101	T0 DPLL 4 Hz acquisition bandwidth.	
			01110	T0 DPLL 8 Hz acquisition bandwidth.	
			01111	T0 DPLL 18 Hz acquisition bandwidth.	
			10000	T0 DPLL 35 Hz acquisition bandwidth.	
			10001	T0 DPLL 70 Hz acquisition bandwidth.	
			All other values	Not used.	

Configure T4 DPLL damping register

Software name	Address (0x0)	Access	Default value
cnfg_T4_DPLL_damping	6A	R/W	0001 0011
Description	Register to configure the damping factor of the T4 DPLL, along with the gain of phase detector 2 in some modes.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*Not used*	Not used.	-	-	0
[6:4]	*T4_PD2_gain_alog_8k*	Register to control the gain of T4 phase detector 2 when locking to a reference of 8 kHz or less in analog feedback mode. This setting is only used if automatic gain selection is enabled by the *T4_PD2_gain_enable* bit of the cnfg_T4_DPLL_PD2_gain register.	-	This value sets the gain of the phase detector 2, when locking to an 8 kHz reference in analog feedback mode.	001
3	*Not used*	Not used.	-	-	0
[2:0]	*T4_damping*	Register to configure the damping factor of the T4 DPLL. The bit values correspond to different damping factors, depending on the bandwidth selected. A damping factor of 5 is the default (011). The gain peak and damping factors in the table below correspond to the frequency and bit values in the table to the right.		T4 DPLL damping factor at the following bandwidth frequency selections:	011

Damping Factor	Gain Peak
1.2	0.4 dB
2.5	0.2 dB
5	0.1 dB
10	0.06 dB
20	0.03 dB

Value	18 Hz	5 Hz	70 Hz
001	1.2	1.2	1.2
010	2.5	2.5	2.5
011	5	5	5
100	5	10	10
101	5	10	20
000	Not used		
110	Not used		
111	Not used		

Configure T0 DPLL damping register

Software name	Address (0x0)	Access	Default value
cnfg_T0_DPLL_damping	6B	R/W	0001 0011

Description	Register to configure the damping factor of the T0 DPLL, along with the gain of phase detector 2 in some modes.

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*Not used*	Not used.	-	-	0
[6:4]	*T0_PD2_gain_alog_8k*	This register controls the gain of T0 phase detector 2 when locking to a reference of 8 kHz or less in analog feedback mode. This setting is only used if automatic gain selection is enabled by the *T0_PD2_gain_enable* bit in the cnfg_T0_DPLL_PD2_gain register.	-	Gain value of phase detector 2 when locking to an 8 kHz reference in analog feedback mode.	001
3	*Not used*	Not used.	-	-	0
[2:0]	*T0_damping*	Register to configure the damping factor of the T0 DPLL. The bit values correspond to different damping factors, depending on the bandwidth selected. A damping factor of 5 is the default (011).			
		The gain peak and damping factors in the table below correspond to the frequency and bit values in the table to the right.	T0 DPLL damping factor at the following bandwidths frequency selections:		

Damping Factor	Gain Peak
1.2	0.4 dB
2.5	0.2 dB
5	0.1 dB
10	0.06 dB
20	0.03 dB

Value	<4 Hz	8 Hz	18 Hz	35 Hz	70 Hz
001	5	2.5	1.2	1.2	1.2
010	5	5	2.5	2.5	2.5
011	5	5	5	5	5
100	5	5	5	10	10
101	5	5	5	10	20
000	Not used.				
110	Not used.				
111	Not used.				

Configure T4 DPLL PD2 gain register

Software name	Address (0x0)	Access	Default value
cnfg_T4_DPLL_PD2_gain	6C	R/W	1100 0010
Description	Register to configure the gain of phase detector 2 in some modes for the T4 DPLL.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*T4_PD2_gain_ enable*	Bit to enable or disable phase detector 2 on the T4 DPLL.	0 1	T4 DPLL phase detector 2 is not used. T4 DPLL phase detector 2 gain is enabled, and the choice of gain is determined according to the locking mode: - digital feedback mode. - analog feedback mode. - analog feedback at 8 kHz.	1
[6:4]	*T4_PD2_gain_ alog*	This register controls the gain of phase detector 2 when locking to a reference with a frequency that is higher than 8 kHz, in analog feedback mode. This setting is only used if automatic gain selection is enabled by the *T4_PD2_gain_enable* bit in this register.	-	Gain value of phase detector 2 when locking to a high frequency reference in analog feedback mode.	100
3	*Not used*	Not used.	-	-	0
[2:0]	*T4_PD2_gain_ digital*	This register controls the gain of phase detector 2 when locking to a reference in digital feedback mode. This setting is always used if automatic gain selection is disabled by the *T4_PD2_gain_enable* bit in this register.	-	Gain value of phase detector 2 when locking to any reference in digital feedback mode.	010

Configure T0 DPLL PD2 gain register

Software name	Address (0x0)	Access	Default value
cnfg_T0_DPLL_PD2_gain	6D	R/W	1100 0010
Description	Register to configure the gain of phase detector 2 in some modes for the T0 DPLL.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*T0_PD2_gain_enable*	Bit to enable or disable phase detector 2 on the T0 DPLL.	0 1	T0 DPLL phase detector 2 is not used. T0 DPLL phase detector 2 gain is enabled, and the choice of gain is determined according to the locking mode: - digital feedback mode. - analog feedback mode. - analog feedback at 8 kHz.	1
[6:4]	*T0_PD2_gain_alog*	This register controls the gain of phase detector 2 when locking to a reference, higher than 8 kHz, in analog feedback mode. This setting is only used if automatic gain selection is enabled by the *T0_PD2_gain_enable* bit in this register.	-	Gain value of phase detector 2 when locking to a high frequency reference in analog feedback mode.	100
3	*Not used*	Not used.	-	-	0
[2:0]	*T0_PD2_gain_digital*	This register controls the gain of phase detector 2 when locking to a reference in digital feedback mode. This setting is always used if automatic gain selection is disabled by the *T0_PD2_gain_enable* bit in this register.	-	Gain value of phase detector 2 when locking to any reference in digital feedback mode.	010

Configure phase offset register [7:0]

Software name	Address (0x0)	Access	Default value
cnfg_phase_offset [7:0]	70	R/W	0000 0000
Description	Bits [7:0] of the phase offset control register.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*phase_offset_value[7:0]*	This register forms part of the phase offset control.	-	See register cnfg_phase_offset [15:8] for more details.	0000 0000

Configure phase offset register [15:8]

Software name	Address (0x0)	Access	Default value
cnfg_phase_offset [15:8]	71	R/W	0000 0000
Description	Bits [15:8] of the phase offset control register.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*phase_offset_ value[15:8]*	This register forms part of the phase offset control. If the phase offset register is written to when the DPLL is locked to an input, it is possible that some internal signals could lose synchronization. In order to avoid this, the phase offset is automatically “ramped” to the new value. If the phase offset is only ever adjusted when the device is in holdover mode, then this is not necessary. In this circumstance automatic “ramping” can be disabled, using the cnfg_sync_monitor register. This register is ignored, and has no effect, when phase build-out is enabled in either register cnfg_monitors or register cnfg_phasemon.	-	The value in this register is concatenated with the contents of the cnfg_phase_offset [7:0] register. The combined value is a 16-bit 2’s complement signed number. This value, multiplied by 6.279, represents the applied phase offset in picoseconds. The phase offset register does not control a “traditional” delay line. This number 6.279 actually represents a fractional portion of the period of an internal 77.76 MHz cycle and can, therefore, be represented more accurately as follows. Each bit value of the register represents the period of the internal 77.76 MHz clock divided by 2^{11} (1024). If, for example, the DPLL is locked to a reference that is +1 ppm in frequency with respect to a perfect oscillator, then the period, and hence the phase offset, are decreased by 1 ppm. Programming a value of 1024 into the phase offset register produces a complete inversion of the 77.76 MHz output clock. The exact period of the internal 77.76 MHz clock is determined by the current state of the DPLL: In locked mode its accuracy depends on that of the locked to input. In holdover or free-run modes it depends on the accuracy of the external oscillator.	0000 0000

Configure PBO phase offset register

Software name	Address (0x0)	Access	Default value
cnfg_PBO_phase_offset	72	R/W	0000 0000
Description	Register to offset the mean time error of phase build-out events.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:6]	*Not used*	Not used.	-	-	00
[5:0]	*PBO_phase_offset*	Each time a phase build-out event is triggered, an uncertainty of up to 5 ns is introduced. This translates to a phase hit on the output. The mean error over a large number of events is designed to be zero. This register can be used to introduce a fixed offset into each PBO event. This has the effect of moving the mean error in a positive or negative direction in time.	-	The value in this register is a 6-bit 2's complement number. The value multiplied by 0.101 gives the programmed offset in nanoseconds. Values greater than +1.4 ns or less than -1.4 ns should NOT be used as they may cause internal mathematical errors.	0000 00

Configure phase loss fine limit register

Software name	Address (0x0)	Access	Default value
cnfg_phase_loss_fine_limit	73	R/W	1010 0010
Description	Register to configure some of the parameters of the T0 DPLL phase detector.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*fine_limit_en*	Register bit to enable the phase loss fine limit alarm, as defined in the *phase_loss_fine_limit* bits in this register. When this bit is disabled, phase lock/loss is determined by other means within the device. This bit must be disabled when multi-UI jitter tolerance is required, see register cnfg_phase_loss_coarse_limit.	0 1	Phase loss indication is only triggered by other means. Phase loss is triggered when the phase error exceeds the limit programmed in the *phase_loss_fine_limit* bits in this register.	1
6	*noact_ph_loss*	The DPLL detects that an input has failed very rapidly. Normally the DPLL uses a leaky bucket accumulator to detect a phase loss condition, which means that a certain number of missing cycles are tolerated. When the source becomes available again the DPLL phase locks to the nearest edge (±180°). If the leaky bucket accumulator detects a phase loss condition, then frequency and phase locking is used (±360° locking) when a source becomes available again. This bit forces the DPLL to immediately indicate a phase loss condition when no activity is detected.	0 1	Lack of activity on a reference does not trigger a phase lost indication. Lack of activity triggers a phase lost indication.	0
5	*narrow_en*	(test control bit) Set to 1 (default value).	1	Set to 1.	1
[4:3]	*Not used*	Not used.	-	-	00
[2:0]	*phase_loss_ fine_limit*	When the *fine_limit_en* bit of this register is enabled, these bits set the phase limit value, in steps, before the device indicates phase lost or locked. The phase position of the inputs to the DPLL has to be within the window limit for 1 to 2 seconds before the device indicates phase lock. If the phase position drifts outside the window for any time then phase loss is immediately indicated. For most cases the default value of 2 (010) is satisfactory. The default value of 2 (010) gives a window size of around ±(90° to 180°). The window size changes in proportion to the value, so a value of 1 (001) gives a narrow phase acceptance or lock window of approximately ±(45° to 90°).	000 001 010 011 100 101 110 111	Do not use. Indicates phase loss continuously. Small phase window for phase lock indication. Recommended value.)) Larger phase windows for phase lock indication.))	010

Configure phase loss coarse limit register

Software name	Address (0x0)	Access	Default value
cnfg_phase_loss_coarse_limit	74	R/W	1000 0101
Description	Register to configure some of the parameters of the T0 DPLL coarse phase loss detector.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*coarse_lim_phaseloss_en*	This bit enables the coarse phase detector, whose range is determined by the *phase_loss_coarse_limit* bits in this register. The coarse phase loss detector limits the number of input clock cycles (UI) that the input phase can move before the DPLL indicates phase loss.	0 1	Phase loss is not triggered by the coarse phase lock detector. Phase loss is triggered when the phase error exceeds the limit programmed in the *phase_loss_coarse_limit*, bits in this register.	1
6	*wide_range_en*	This bit enables the wide range phase detector. Using this detector allows the device to directly phase lock (at the input frequency of 77.76 MHz), even if there is a large amount of jitter on the input. This detector tracks drifts in input phase of many cycles (UI) without triggering an alarm. The range of this phase detector is set by the same *phase_loss_coarse_limit* bits used for the phase loss coarse limit.	0 1	Wide range phase detector is disabled. Wide range phase detector is enabled.	0
5	*multi_ph_resp*	Enables the phase result from the coarse phase detector to be used in the DPLL algorithm. The *wide_range_en* bit in this register should also be set if this feature is activated. The coarse phase detector can measure and keep track of phase errors over many thousands of input cycles. This provides excellent jitter and wander tolerance. If this bit is set, the measured phase result is used in the DPLL algorithm, giving a faster pull-in of the DPLL when the phase result is large. If this bit is not set then the phase measurement is limited to ±360°. This can give slower pull-in rates at higher input frequencies, but might also produce less overshoot. Setting this bit in direct locking mode, for example with a 19.44 MHz input, would give the same dynamic response as a 19.44 MHz input used with Lock8k mode (which divides the input frequency down to 8 kHz before applying it to the DPLL).	0 1	The DPLL phase detector is limited to ±360° (±1 UI). However it still remembers its original phase position over many thousands of UI if the *wide_range_en* bit is set. The DPLL phase detector also uses the full coarse phase detector result. It can now measure up to: ±360° X 8191 UI = ±2,948,760°.	0
4	*Not used*	Not used.	-	-	0

continued...

Configure phase loss coarse limit register (continued)

Bit	Bit name	Bit description	Value	Bit settings	Reset
[3:0]	*phase_loss_ coarse_limit*	Sets the range of the coarse phase loss detector and the coarse phase detector. If a jitter tolerance of greater than 0.5 UI is required, when locking to a high frequency signal, the DPLL can be configured to track phase errors over many input clock periods. This is particularly useful with very low bandwidths. This register configures the UI range over which the input phase can be tracked. It also sets the range of the coarse phase loss detector, which can be used with or without the multi-UI phase capture range capability. This register value is used by the *wide_range_en* and *coarse_lim_phaseloss_en* bits in this register.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100-1111	Input phase error tracked over ±1 UI. Input phase error tracked over ±3 UI. Input phase error tracked over ±7 UI. Input phase error tracked over ±15 UI. Input phase error tracked over ±31 UI. Input phase error tracked over ±63 UI. Input phase error tracked over ±127 UI. Input phase error tracked over ±255 UI. Input phase error tracked over ±511 UI. Input phase error tracked over ±1023 UI. Input phase error tracked over ±2047 UI. Input phase error tracked over ±4095 UI. Input phase error tracked over ±8191 UI.	0101

Configure phase monitor register

Software name	Address (0x0)	Access	Default value
cnfg_phasemon	76	R/W	0000 0110
Description	Register to configure the noise rejection function for low frequency inputs.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*ip_noise_ window*	This bit enables a timing window of 5% tolerance around the expected edge, when using low-frequency inputs (2, 4 and 8 kHz). This feature ensures that the DPLL ignores any edge caused by noise outside the 5% window. Using this feature reduces any possible phase hit when a low-frequency connection is removed and contact bounce is possible.	0 1	The DPLL considers all edges for phase locking. The DPLL ignores input edges outside a 95% to 105% timing window.	0
[6:0]	*Not used*	Not used.	-	-	000 0110

STS current phase register [7:0]

Software name	Address (0x0)	Access	Default value
sts_current_phase [7:0]	77	RO	0000 0000
Description	Bits [7:0] of the current phase register.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*current_phase*	Bits [7:0] of the current phase register. See register sts_current_phase [15:8] for details.	-	See sts_current_phase [15:8] for details.	0000 0000

STS current phase register [15:8]

Software name	Address (0x0)	Access	Default value
sts_current_phase [15:8]	78	RO	0000 0000
Description	Value [15:8] of the current phase register.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*current_phase*	Bits [15:8] of the current phase register. This register reports the value read from the phase detector of either the T0 DPLL or the T4 DPLL. The selection of DPLL is set by *T4_T0_select* bit in the cnfg_registers_source_select register. The phase detector value is averaged in the phase averager before being made available.	-	The value in this register should be concatenated with the value in the sts_current_phase [7:0] register. This 16-bit value is a 2's complement signed integer. The value should be multiplied by 0.707 to obtain the averaged value of the current phase error, in degrees, as measured at the DPLL's phase detector.	0000 0000

Configure phase alarm timeout register

Software name	Address (0x0)	Access	Default value
cnfg_phase_alarm_timeout	79	R/W	0011 0010
Description	Register to configure how long the T0 DPLL attempts to lock to an input before it raises a phase alarm.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:6]	*Not used*	Not used.	-	-	00
[5:0]	*timeout_value*	Phase alarms can only be raised on an input when the T0 DPLL is attempting to lock to it. Once an input has been rejected due to a phase alarm, there is no way to measure whether it is good again, because it is no longer selected by the DPLL. This register specifies how long the T0 DPLL attempts to lock to an input before it raises a phase alarm. The *phalarm_timeout* bit in the cnfg_input_mode register defines whether an alarm remains active until the software resets it, or whether it resets automatically after a 128 second timeout period.	-	This 6-bit unsigned integer represents the length of time that must elapse before a phase alarm is raised on an input. Multiply the value in this register by 2 to obtain the time in seconds. This value is the time that the controlling state machine spends in pre-locked, pre-locked2 or phase-lost modes before setting the phase alarm on the selected input.	1100 10

Configure sync pulses register

Software name	Address (0x0)	Access	Default value
cnfg_sync_pulses	7A	R/W	0000 0000
Description	Register to configure the sync outputs available from TO10 and TO11 and to select the source for the 2 kHz and 8 kHz outputs from TO1 - TO7.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*2k_8k_from_T4*	Register to select the source (T0 or T4) for the 2 kHz and 8 kHz outputs available from TO1 to TO7.	0 1	2/8 kHz on TO1-TO7 is generated from the T0 DPLL. 2/8 kHz on TO1-TO7 is generated from the T4 DPLL.	0
[6:4]	*Not used*	Not used.	-	-	0
3	*8k_invert*	Register bit to invert the 8 kHz output from TO10.	0 1	8 kHz TO10 output not inverted. 8 kHz TO10 output inverted.	0
2	*8k_pulse*	Register bit to enable the 8 kHz output from TO10 to be either pulsed or 50:50 duty cycle. Output TO3 must be enabled to use “pulsed output” mode on output TO10. Then the pulse width on TO10 is defined by the period of the output programmed on TO3.	0 1	8 kHz TO10 output not pulsed. 8 kHz TO10 output pulsed.	0
1	*2k_invert*	Register bit to invert the 2 kHz output from TO11.	0 1	2 kHz TO11 output not inverted. 2 kHz TO11 output inverted.	0
0	*2k_pulse*	Register bit to enable the 2 kHz output from TO11 to be either pulsed or 50:50 duty cycle. Output TO3 must be enabled to use “pulsed output” mode on output TO10. Then the pulse width on TO11 is defined by the period of the output programmed on TO3.	0 1	2 kHz TO11 output not pulsed. 2 kHz TO11 output pulsed.	0

Configure sync phase register

Software name	Address (0x0)	Access	Default value
cnfg_sync_phase	7B	R/W	0000 0000
Description	Register to configure the synchronization behavior for the external frame reference.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*indep_FrSync/ MFrSync*	Allows the option to maintain the alignment of FrSync and other clock outputs during synchronization from the SYNC2K input, or not to maintain alignment to all clocks and thus leave any of the output clocks undisturbed.	0 1	The OC-N rate clocks are not affected by the SYNC2K input. The SYNC2K input is sampled with a 6.48 MHz precision. 6.48MHz should be provided as the input reference clock. Allows the SYNC2K input to operate with a 19.44 MHz or 38.88 MHz input clock reference. Input sampling and output alignment to 19.44 MHz are used when the current clock input is 19.44 MHz: otherwise 38.88 MHz sampling precision is used.	0
6	*sync_OC-N_rates*	Allows the SYNC2K input to synchronize the OC-3 derived clocks in order to maintain alignment between the FrSync output and the output clocks. This provides finer sampling precision of the SYNC2K input of 19.44 MHz or 38.88 MHz.	0 1	The OC-N rate clocks are not affected by the SYNC2K input. The SYNC2K input is sampled with a 6.48 MHz precision. 6.48MHz should be provided as the input reference clock. Allows the SYNC2K to operate with a 19.44 MHz or 38.88 MHz input clock reference. Input sampling and output alignment to 19.44 MHz are used when the current clock input is 19.44 MHz: otherwise 38.88 MHz sampling precision is used.	0
[5:2]	*Not used*	Not used.	-	-	0000
[1:0]	*sync_phase*	Register to control the sampling of the external sync input. Nominally the falling edge of the input is aligned with the falling edge of the reference clock. The sampling margin is ±0.5 U.I. (Unit Interval).	00 01 10 11	The external sync input is sampled around the target time. The external sync input is sampled 0.5 U.I. early. The external sync input is sampled 1 U.I. late. The external sync output is sampled 0.5 U.I. late.	00

Configure sync monitor register

Software name	Address (0x0)	Access	Default value
cnfg_sync_monitor	7C	R/W	0010 1011
Description	Register to configure the external sync input monitor. It also has a bit to control the phase offset automatic ramping feature.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
7	*ph_offset_ramp*	This bit forces an internal phase offset calibration, see register cnfg_phase_offset [15:8]. The calibration routine is transparent to the outside and puts the device in holdover mode while it internally ramps the phase offset to zero, resets all internal output and feedback dividers and then ramps the phase offset to the value that is current programmed value in registers cnfg_phase_offset [7:0] or cnfg_phase_offset [15:8]. Holdover mode is then turned off. This entire process is transparent to the outside, and produces no visible change in output phase offset.	0 1	Phase offset is automatically ramped from the old value to the new value when there is a change in registers cnfg_phase_offset [7:0] or cnfg_phase_offset [15:8]. Start the phase offset internal calibration routine. This bit automatically resets to 0 when the routine is complete.	0
[6:4]	*sync_monitor_ limit*	The input can be used to synchronize the outputs. An alternative is to use the sync monitor block to raise an alarm if the input does not align with the output within a certain number of input clock cycles. This register defines this number of cycles in UI of the selected reference source. If alignment does not occur within this limit, then a sync alarm is raised in the sts_operating register.	000 001 010 011 100 101 110 111	Sync alarm raised beyond ±1 UI. Sync alarm raised beyond ±2 UI. Sync alarm raised beyond ±3 UI. Sync alarm raised beyond ±4 UI. Sync alarm raised beyond ±5 UI. Sync alarm raised beyond ±6 UI. Sync alarm raised beyond ±7 UI. Sync alarm raised beyond ±8 UI.	010
[3:0]	*sync_reference _source*	The reference can only be associated with a particular input channel. When automatic external sync enabling is selected by the *auto_extsync_en* bit in the cnfg_input_mode register, the input is only enabled when locked to the selected source. This feature can be used to associate the Frame Sync reference with a reference clock for master/slave operation.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	Not used. External sync is associated with input channel I1. External sync is associated with input channel I2. External sync is associated with input channel I3. External sync is associated with input channel I4. External sync is associated with input channel I5. External sync is associated with input channel I6. External sync is associated with input channel I7. External sync is associated with input channel I8. External sync is associated with input channel I9. External sync is associated with input channel I10. External Sync is associated with input channel I11. External sync is associated with input channel I12. External sync is associated with input channel I13. External sync is associated with input channel I14. Not used.	1011

Configure interrupt register

Software name	Address (0x0)	Access	Default value
cnfg_interrupt	7D	R/W	0000 0010
Description	Register to configure the interrupt output pin.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:3]	*Not used*	Not used.	-	-	00000
2	*GPO_en*	(Interrupt general purpose output). If the interrupt output pin is not required, then setting this bit allows the pin to be used as a general purpose output. The pin is then driven to the state of the polarity control bit, *int_polarity*.	0 1	Interrupt output pin used for interrupts. Interrupt output pin used for GPO purpose.	0
1	*tristate_en*	The interrupt pin can be configured so it can be connected directly to a processor, or it can be wired together with other sources.	0 1	Interrupt pin is always driven when inactive. Interrupt pin is only driven when it is active. When inactive, the pin becomes high-impedance.	1
0	*int_polarity*	The interrupt pin can be configured to be active high or low.	0 1	Active low - the pin is driven low to indicate an active interrupt. Active high - the pin is driven high to indicate an active interrupt.	0

Configure protection register

Software name	Address (0x0)	Access	Default value
cnfg_protection	7E	R/W	1000 0101
Description	Protection register to protect against erroneous software writes.		

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:0]	*protection_ value*	This register can be used to ensure that the software writes a specific value to this register, before being able to modify any other register in the device. Three modes of protection are offered: (i) protected. (ii) fully unprotected. (iii) single unprotected. When protected, no other register in the device can be written to. When fully unprotected, any writable register in the device can be written to. When single unprotected, only one register can be written to before the device automatically re-protects itself.	0000 0000 to 1000 0100 1000 0101 1000 0110 1000 0111 to 1111 1111	Protected mode. Fully unprotected. Single unprotected. Protected mode.	1000 0101

Configure microprocessor selection register

Software name	Address (0x0)	Access	Default value
cnfg_upsel	7F	R/W*	0000 0101*

Description	This register reflects the state of the UPSEL device pins following a reset. It can also be written to in EPROM mode. *The default value depends on the value on the UPSEL[2:0] pins.

Bit	Bit name	Bit description	Value	Bit settings	Reset
[7:3]	*Not used*	Not used.	-	-	0000 0
[2:0]	*upsel_value*	Do not use.		Set to 101	000

APPLICATIONS

Figure 34 shows three different ways in which timing (that is, frequency stability) can be delivered to the end-points of a transmission link.

The TDM method uses physical layer signals to carry timing from a Primary Reference Clock (PRC), using a chain of interconnected SDH Equipment Clocks (SEC) and Synchronisation Supply Units (SSU); this is the traditional method.

The SyncE method uses Synchronous Ethernet, an adaptation of the TDM method, whereby timing is carried on the physical-layer signals of the Ethernet network. The method uses Ethernet Equipment Clocks (EEC) and SSUs to carry timing from the PRC. SyncE can only operate on equipment that allows the timing to be applied to the physical layer signals and thus requires new Ethernet equipment. The performance specifications of the EEC and the network limits of SyncE are such as to allow SyncE and TDM timing paths to interwork.

The PTP method uses the Precision Timing Protocol to carry timing information in the form of timestamps contained in special PTP frames. This method has the advantage of being able to operate on legacy Ethernet equipment. However, the performance can be affected by traffic loading. The ITU have defined a new PTP profile to suit frequency delivery over legacy packet networks; this is defined in ITU Recommendation G.8265.1[33].

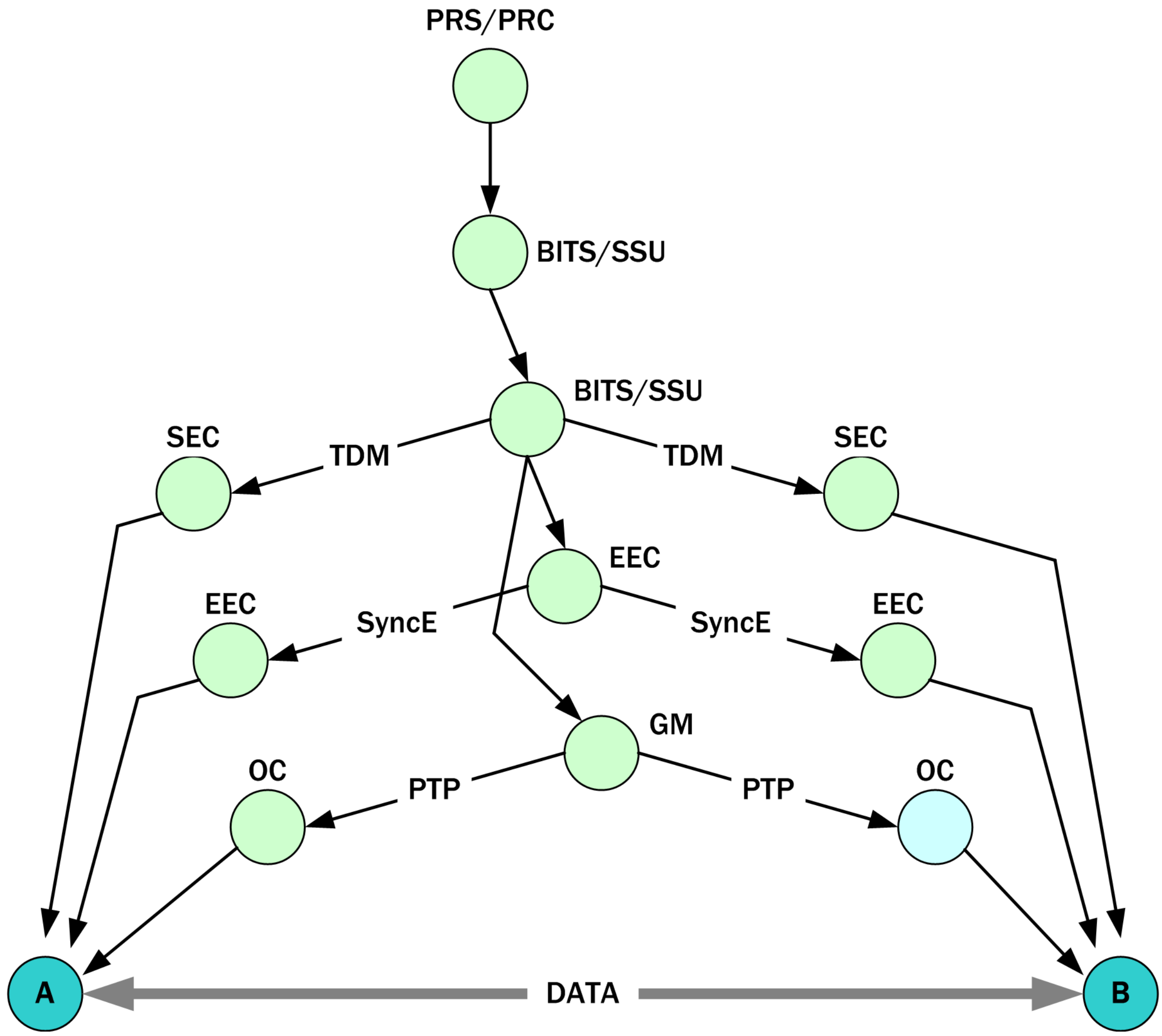

Figure 34 - Timing techniques for different networks

The ACS9522 contains timing functions that can be used in many ways to support a variety of situations. The device can generate output clock signals and/or timing packets from a range of input clocks, and can thus serve as a general-purpose, next-generation timing device.

Refer to Figure 2 for a block diagram of the ACS9522.

When the device is operating in the PTP mode, the TDM and PTP blocks are tied together through the TDM Block Multiplexer and the PTP Block Multiplexer. This allows them to support each other in the ways outlined in previous sections. That is, the TDM Block and PTP Block multiplexers can be used to position the TDM Block to precede or succeed the PTP Block. This option can be used to provide enhanced stability - for example when locking a PTP Master to a reference clock signal, or for adding a PTP-recovered clock from a slave to a reference-selection scheme. In PTP mode, the control of the device, including the multiplexers and the TDM Block, is achieved by using API calls.

An overview of PTP mode behavior is given in Next-generation timing and an overview of TDM mode behavior is given in TDM timing.

Next-generation timing

Next-generation equipment uses a packet network to transport information. If a tie-up to the existing synchronization network can be made by using traditional PDH/SDH/SONET signals or Synchronous Ethernet signals, then this method of timing can still be delivered. The ACS9522 can operate as an integral part of the Synchronous Ethernet distribution scheme or, if traditional line-timing methods are not available, the device can operate within a packet-based timing transfer mechanism.

The ACS9522 supports Synchronous Ethernet by meeting ITU-T recommendation G.8262[29] in terms of noise-filtering, noise-generation and noise-transfer, including reference-switching transient control and holdover. The output wander is well within the requirements, but output jitter must be further reduced, which is typically done near to the output PHY to limit noise pick-up.

The ACS9522 also supports packet-based timing methods. Packet-based timing methods can provide the usual frequency transfer, or they can also provide ToD transfer, or the transfer of a common phase. The second version of the Precision Time Protocol, PTPv2 (otherwise known as IEEE 1588v2[13]), has been developed with many telecommunication applications in mind, and DPSync, when acting in a packet-timing mode, uses PTP as the transport method to carry timing data between the GM clock and the ordinary clocks.

The basic principle by which PTP performs time transfer is described in the PTP standard. However, the standard does not stipulate how to operate in the presence of packet delay variation. DPSync adds its own proprietary filtering algorithms to provide accurate timing transfer in the presence of PDV, network re-routes and other conditions.

The ACS9522 DPSync can act as either a PTP GM clock or as a PTP OC. The role can be decided automatically as part of a clock-selection mechanism, or by configuration by the host code.

PTP messages

Figure 35 shows the three main messages used to transfer timing data between a GM and its OCs.

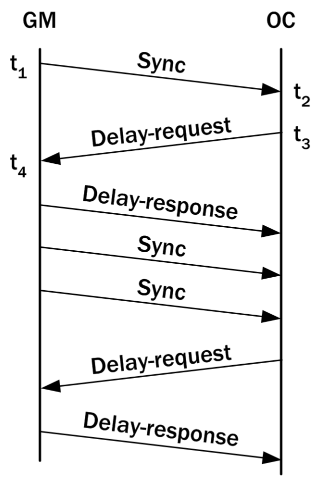

Figure 35 - Message triplet of PTP

The Sync message is sent most frequently and carries the time t1 at which the timestamp point of the message crossed the MII of the GM. The time at which the Sync message crosses the MII of the OC is t2 and is measured using the timebase of the OC. The rate of Sync messages should be high enough to overcome drift in the local reference of the OC and allow sufficient filtering of packet delay variation encountered in the network. Typical rates for most telecom applications connected via a typical network range from 8 to 32 Sync packets per second, when using a local oscillator of acceptable quality at the OC.

The Delay-Request message is sent to the GM by the OC and allows the network path delay to be estimated. The message carries the time t3 at the OC at the moment of transmission. The rate of transmission of Delay-Request messages should be chosen to suit the PDV, and rates similar to that of the Sync message can be expected, although other rates are allowed.

The GM sends one Delay-Response message for each Delay-Request message that it receives. The Delay-Response message carries the time t4 at which the GM received the Delay-Request message.

These message transfers provide the four timestamps, carrying times t1-t4, to the OC, from which it can calculate the time at the GM.

There are other messages in PTP, but they are not involved in the time-transfer. Announce messages, for example, carry information about the reference source used by a clock.

The Sync and Delay-Request messages are classed as event messages in PTP and, when using the UDP-IP-Ethernet mapping, are from UDP Port 319. Other messages are general messages from UDP Port 320.

To transfer ToD or common phase across a network, the PTP packet flow must be two-way; that is, both Sync and Delay-Request PTP messages must be used. It is recommended that unicast transmission be used, supported, where possible, by Quality of Service (QoS) assistance in the nodes in the network through which the PTP messages flow. These measures not only help to provide the best accuracy and stability of the ToD deliverable by an OC, but they also reduce the traffic load on clocks. The alternative use of multicast PTP event messages means that each clock receives Delay-Request messages from every OC in the network, and it also receives Delay-Response messages intended for every OC in the network. As the number of PTP clocks in a network grows, this can overload the ports of the clocks and interfere with the legitimate flow of other services.

Grandmaster selection (default IEEE 1588 BMCA)

The GM is the clock which distributes the timescale amongst the clocks in the network. Most of the other clocks would take their timing from it, although it is possible to have some clocks which cannot defer to others; these could also distribute their timing or they could go into a passive state. The action they take depends on the clock selection mechanism employed. A basic clock-selection mechanism has been defined in PTP (the BMCA), which is suitable for many applications of PTP. It may not, however, be universally adopted in telecoms applications because it does not mirror the traditional clock hierarchy. Alternative clock-selection mechanisms can be defined in PTP profiles.

According to the PTP BMCA, the GM clock is the one to which all other clocks have deferred. On start-up, each PTP clock listens for Announce messages from a GM; these contain information about the reference source quality and any pre-configured preferences for the order in which clocks should be selected. If no Announce messages are heard after a short period of time, the clock begins to send its own Announce messages. Each clock compares the information from other clocks with its local values and decides whether it is the best clock in the network; if not, it becomes an OC (if it can) and prepares to accept timing from another clock. The parameters compared, and the order in which they are compared, is as follows:

Priority 1
Clock Quality
Priority 2
Clock ID

Using the Priority 1 value in the first comparison allows the network operator to pre-determine the order in which GMs would be selected. However, this assumes that the quality of the reference source driving the selected GM is constant; the BMCA cannot respond to changes in the quality of the clock if the Priority 1 value alone is enough to make the selection. To bring the clock quality parameters into the selection mechanism, the Priority 1 value has to be set to be the same value in all clocks being considered for the GM role. This then allows the BMCA to identify the clock which advertises the best reference source and can allow that to become the GM. Using the BMCA, therefore, the selection depends heavily on the configured quality of the reference sources used by the clocks.

The reference source is of vital importance in PTP. Not only does it control the quality of the timing being distributed around the network (in the case of the GM), it is also used by the BMCA to identify the GM; in addition to this, it also limits the range of applications that the timing network can support. For example, if an application requires ToD, then the reference supplied to the GM must provide this.

The reference is the source of timing to which a clock is tied. Potential GMs and OCs both have references, where the reference of a potential GM would typically be supplied from an external source (e.g., a GPS receiver if ToD is to be transferred), while that of an OC would typically be the local oscillator that provides a local system clock frequency.

The quality of the reference is represented by three parameters, known as clock accuracy, clock variance and clock class. The clock accuracy parameter indicates how closely the reference represents the ideal source. This is usually an estimate derived from experience with the type of reference employed - for example, a GPS receiver can be expected to be within 100 ns of true GPS time, even though the actual error is unknown for a particular receiver.

The clock accuracy parameter is only of use when ToD applications are to be supported; it is redundant for frequency-delivery applications, for example.

The clock variance represents the stability of the reference, which is related to the noise content and drift of the reference over time; again, this is usually an estimate based on experience with the type of reference. In principle, clock variance could be useful in frequency-delivery applications, but this would need additional standardisation beyond the current PTP standard.

The clock class parameter indicates the type of reference and how it can be used in a PTP network -- for example, whether the clock is currently locked to its reference and the reference is valid, or that the clock's reference is currently invalid but is still within the tolerated accuracy error; the clock class can also indicate whether a clock can be used as a GM or whether it can only become an OC. The clock class parameter is the most useful of the clock quality parameters in telecom applications. It is analogous to an SSM value, although any equivalence would need to be standardised (e.g. G.8265.1[33]).

Using these clock quality parameters, the "best master clock" would be the clock which was allowed to be a GM and was tied to a valid reference which had the tightest accuracy, the smallest variance and was suitable for the application.

In accordance with the PTP standard, it is sometimes appropriate to limit a PTP clock to adopting a role which is appropriate to its particular situation, and barring it from adopting other roles; for example, clocks which do not have good enough local oscillators or external references should not be allowed to become GrandMasters, even if they are the best clocks visible in the PTP network (such a clock would be a so-called "Slave-only" clock); similarly, some clocks may not be allowed to become slaves of other clocks. To support this, the ACS9522 can be individually barred from adopting either the GM role or the OC role. An API call is available to control this configuration, but the default setting is to be able to freely adopt either role according to the clock selection algorithm in use.

BMCA selection based on priority

If the PTP network has a preference for the order in which clocks can become the GM then this can be indicated in the Priority 1 and Priority 2 parameters of the Announce message. Priority 1 is tested first by the BMCA, and the clock with the higher priority is selected; this means that Priority 1 overrides the clock quality parameters. This is useful if it is known that all GM candidates have the same clock quality, and one clock is preferred over others, but it does not allow for changes in the clock quality of a GM to influence the selection. For example, if a GM lost its reference source and went into holdover, this would be indicated by the clock class parameter, but it would not cause the GM to be replaced by one which is still tied to its reference source. For this reason, Priority 1 is probably best used to segregate potential GMs from other clocks (that is, give all potential GMs a high Priority 1 value, and give lesser clocks a lower value). The BMCA would then not be able to select a GM on Priority 1 alone but must look at other parameters as well.

BMCA selection based on reference quality

If the network requires that the clock with the best reference be selected, then Priority 1 should be set to the same value in all GM candidates. The BMCA then selects the GM based on the Clock Quality parameters, in the order ClockClass, Clock Accuracy, Clock Variance. In the BMCA, Clock Class values greater than 127 are used to indicate clocks which are not required to become PTP GrandMasters. To select between clocks which have the same clock quality, the Priority 2 value is used.

BMCA in Multicast vs Unicast networks

Once the best master clock has been identified, all other potential GMs should decide whether to cease transmission of PTP event and Announce messages, leaving just the best master clock to control all the ordinary clocks, or continue transmission.

A strict interpretation of the PTP standard shows that the BMCA need only be applied when multicast transmission is used; there is no strict requirement to apply the BMCA if unicast transmission is used. This is just as well if the Acceptable Master Table (AMT) is to be used, because this allows more than one GM to send PTP messages at any time.

Acceptable Master Table

The AMT is an option in the PTP standard. It allows the behavior of the BMCA to be modified to provide better protection against malicious attacks and/or better application-dependent GM selection.

The AMT enhances protection by allowing an OC to reject potential GMs that are not listed in the Table. As such, it can protect against invalid GMs which are not part of the PTP network.

The AMT can modify the GM-selection mechanism of the BMCA to pick out valid GMs which are able to support a particular application from a greater set of valid GMs which meet all the general PTP requirements but which are not suitable for the application (TAI-traceable GMs as against non-TAI-traceable GMs, for example).

For those GMs which are listed in the AMT, a new priority order can be applied. The priority of each entry in the AMT replaces the Priority 1 value of that GM. This allows an application to treat the set of potential GMs in a very different order to that applied by the GMs themselves (as usually accessed via the Priority 1 values).

This is useful because the requirements of an application are better known by an OC than by the GMs, and it is possible to separate the selection of an OC from that envisaged by the network operator when setting up the Priority 1 values of the GM.

For example, an OC feeding an application which requires ToD traceability may populate the AMT with GMs that have valid ToD references and reject all other GMs. The AMT itself is limited, however, to selecting between potential GMs based on only the replacement priority value.

Without having the host code look at the clock class value, the current GM would remain selected, based on just the AMT priority value, even though an alternative GM, which was still locked to its reference, was available. There is an API call which allows the host code to access clock class data.

The ACS9522 supports both the basic BMCA and the AMT. An API call is available to populate the AMT.

Reference sources for telecom applications

The most important reference source of a PTP system is the one which feeds the GM. The qualities of the reference source can determine which master, out of a set of possible masters, becomes the GM.

To become a PTP GM, the ACS9522 must be supplied with a reference source which meets the needs of the application. Figure 36, Figure 37 and Figure 38 summarise what are expected to be the three main types of applications: ToD, common-phase-transfer and frequency-transfer. The reference source must support the application. For example, a ToD reference must be used if the application requires ToD (see Time of day port).

A ToD reference source would be supplied to the GM as a ToD timing message and a 1PPS signal. Peripheral information, such as the current count of leap seconds, would be supplied via API calls. The ToD timing message would be supplied to the UART receive port. The timing of the message is not critical, provided the message has been received before the rising edge of the 1PPS signal occurs. Supported by the leap-second count, the timing message would be used to derive the PTP timescale inside the ACS9522, and this is carried in the timestamps. The 1PPS signal is fed to the PTP Block and the internal timescale is aligned with it.

To support frequency-transfer applications, a PTP GM using the ACS9522 can accept a signal carrying a spot frequency. If this signal comes from an existing telecom network then it can be routed to the TDM Block of the ACS9522. Some telecom clocks are noisy (e.g., line-recovered clocks) and this noise can affect the stability of the GM timebase if it is supplied directly to the PTP Block. However, the TDM Block can be used to reduce wander and jitter noise, in the traditional SETS role, before the signal is supplied to the PTP Block of the ACS9522. The TDM Block can also be used to select between several such signals if there is a choice to be made; the phase transient caused by such reference-switching is very small even if the signals operate at different frequencies. An example of how to get the ACS9522 to do this filtering and reference-switching is given later.

Alternatively, for telecom clocks which are known to be stable, such as the outputs of BITS/SSUs, or for clocks which cannot be accepted by the TDM Block (such as 1PPS signals), the reference signal can be supplied directly to an input port of the PTP Block. The PTP Block can accept signals at frequencies which cannot be accepted by the TDM Block, but the frequency should meet the requirements in section “PTP input reference port (time selector)”. The control of whether a reference signal is applied to the TDM Block or directly to the PTP Block is made using the TDM Block multiplexer and the PTP Block multiplexer.

Whichever type of reference is supplied, the PTP Block must know the quality of the selected clock and it is given this using an API call.

The accuracy and variance are parameters obtained from the manufacturer of the reference source (or interpreted by the user). For ToD applications, these parameters could be important; for example, if each of the potential Masters have different accuracies or stabilities to offer, then the Master with the best performance should be selected as the GM for the application. However, the individual values for these parameters at each Master may not be known absolutely and may have to be estimated from anecdotal information (such as production test records). Alternatively, if there is no way to know the parameters with sufficient accuracy, the parameters could be removed from the selection mechanism by making them identical across all Masters (the default values provide an easy way to do this). Similarly, for many telecom applications, such as the transfer of existing network clocks across a packet network, these parameters are likely to be meaningless, and it would be best to use the default values.

The clock class parameter is a status flag and does not require an accurate measurement of a physical parameter. It is simply assigned by a network manager in accordance with the rules of PTP. The clock class values are used to indicate what state the reference is in (that is, whether it is traceable to a reference point or not) and this information has to be passed to the ACS9522.

NOTE: The ACS9522 cannot learn any of the quality parameters by itself, but must rely on the honesty of the reference source manufacturer and the host code driving the ACS9522.

ToD applications

If an application requires a ToD signal, the timebase of the GM must be traceable to TAI and OCs (slaves) must be controlled to select only GMs which have TAI-traceable references. The GM reference source determines the traceability to TAI. The selection of GMs with TAI-traceable timebases can be achieved by the OCs using their AMT, which is programmed using host code. Host code must monitor traceability and status information that is passed out in the Announce messages. An API call makes this information available to the host code.

In PTP GM mode, the input reference port consists of IPCLK input clocks and the UART port. With a ToD reference source, an IPCLK port is supplied with a 1 PPS signal and the timing message carrying the current time is applied to the UART port of the ACS9522.

The ToD port can support either TAI-traceable or non-TAI-traceable applications. TAI-traceable applications are those which require the timebase of the ACS9522 to be aligned with a primary time source which is derived from TAI (such as UTC or GPS). Non-TAI-traceable applications are those which require alignment to some other, application-specific, time source.

The UART port accepts timing-related ToD 0183 timing messages (ignoring other messages, such as those which carry position information). The format and timing of this message is described in Time of day message format.

The UART port is used in the same way in both TAI-traceable and non-TAI-traceable applications, but the ACS9522 has to be informed by configuration which type of application it is supporting. In both types of application, the day/hours/minutes/seconds information given by the ToD messages determines the coarse phase of the timebase relative to the source time reference. Failure of the UART port is detected and the messages ignored.

So long as the ACS9522 had previously been receiving good messages, the timebase is correctly aligned to the external timebase and, so long as the 1 PPS signal remains good, the timebase remains aligned during the failure.

When the ACS9522 is informed by configuration that it is tied to a time standard which is traceable to TAI, then, in accordance with IEEE 1588 version 2[13], the internal timebase is aligned to the PTP epoch (which is derived from TAI). Timestamps in PTP event messages are PTP timebase values. PTP announce messages have the following flags and fields set accordingly:

PTP flag is TRUE (indicating that the timebase is traceable to TAI).

L1 and L2 flags are valid.

timeTraceable flag is TRUE.

frequencyTraceable flag is TRUE.

currentUtcOffset field is valid (as set by configuration via an API call).

timeSource field is valid (as set by configuration).

clockClass field is as set by configuration (6, if no special profile is in use).

Figure 36 shows an example of a PTP link delivering ToD to an application, which applies to TAI-traceable and non-TAI-traceable situations.

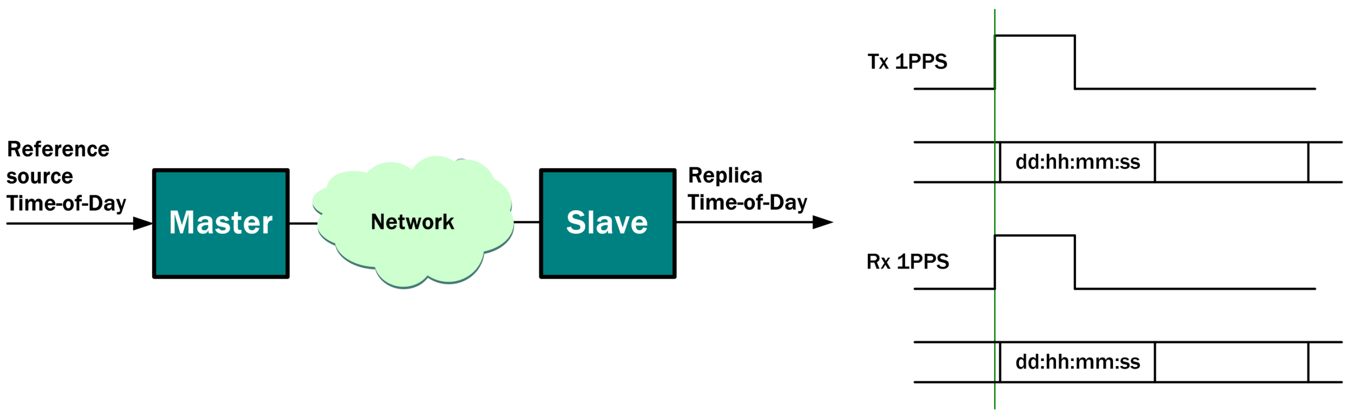

Figure 36 - Example of ToD transfer between ACS9522 pair

In TAI and non-TAI traceable applications, the low-frequency clock input is used to determine the rate and phase of the timebase. The seconds rollover of the internal timebase is steered until it coincides with the rising edge of this input. In this mode, alignment to an external timebase is required, and this input must be driven by a 1 PPS signal (a 1 Hz signal generated so that the rising edge indicates the *top-of-second* point of the external time source: the end of one second and the beginning of the next).

Failures of the 1 PPS signal are detected by an activity monitor integral to the ACS9522 and the signal no longer controls the rate of change of phase of the internal timebase. In this mode, the ACS9522 goes into holdover (if it has been locked for a time sufficient to acquire good holdover data) or free-run. However, there is no automatic reference switching available because the 1PPS signal goes directly to the PTP Block. Instead, the host code has to select an alternative input port if a back-up signal is available.

Common-phase applications

If the application requires a common phase, then the GM can be served by a ToD source, but it can also be served by a source which has an arbitrary epoch. This source would resemble a time-of-day signal but it would not necessarily be traceable to TAI; the timebase of the GM will then be traceable to the arbitrary reference epoch.

OCs must only select GMs which have the same epoch. If the AMT is used in the clock selection mechanism, then this can be configured with GMs which are known to be driven by references traceable to the same source (as mentioned in the ToD section, this requires some help from the host code). However, if the basic BMCA is being used, then another method must be found. The PTP standard does not define how this can be done, but one method could be to assign specific clock class values to specific reference sources. Many clock class values have been set aside for use in individual profiles but, at this time, no profiles have yet been defined.

Figure 37 shows an example of the transfer of a common phase using a 1PPS as the reference.

When the ACS9522 is informed by configuration that it is not tied to a time standard which is traceable to TAI, then the internal timebase is aligned to the epoch of the supplied time source (which may not be derived from TAI, and may thus be considered to have an arbitrary phase).

Timestamps in PTP event messages are ARB timebase values, and PTP announce messages have the following flags and fields set accordingly:

PTP flag is FALSE (indicating that the timebase is not traceable to TAI).

L1 and L2 flags are FALSE.

timeTraceable flag is FALSE.

frequencyTraceable flag is TRUE.

currentUtcOffset field is invalid.

timeSource field is valid (as set by configuration).

clockClass field is as set by configuration (13, if no special profile is in use).

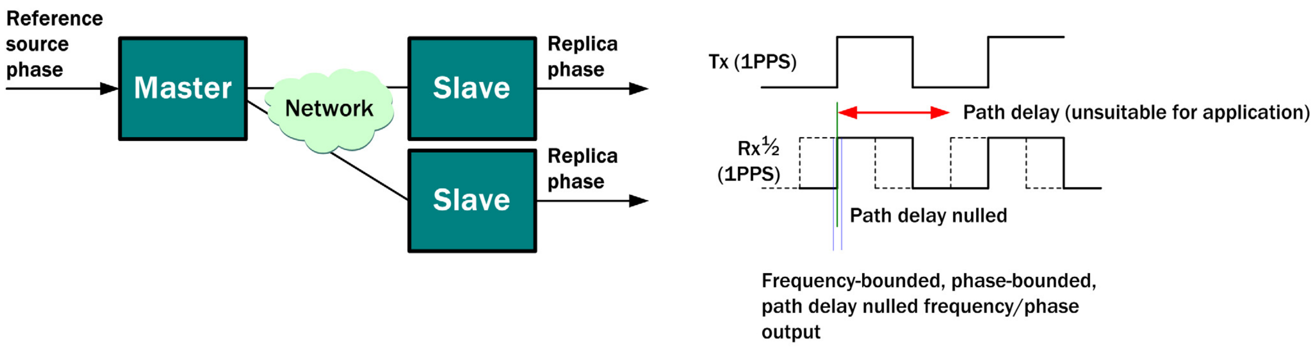

Figure 37 - Example of common phase transfer using PPS as reference

Frequency-transfer applications

If the application requires a frequency only, then the GM can be served by a TAI-traceable ToD signal, an arbitrary-epoch ToD signal or a simple frequency. In the latter case, the timebase of the GM will not be traceable to any external reference epoch but will be generated internally. It will have an arbitrary phase (its own epoch) but will increase at a rate controlled by the reference frequency signal.

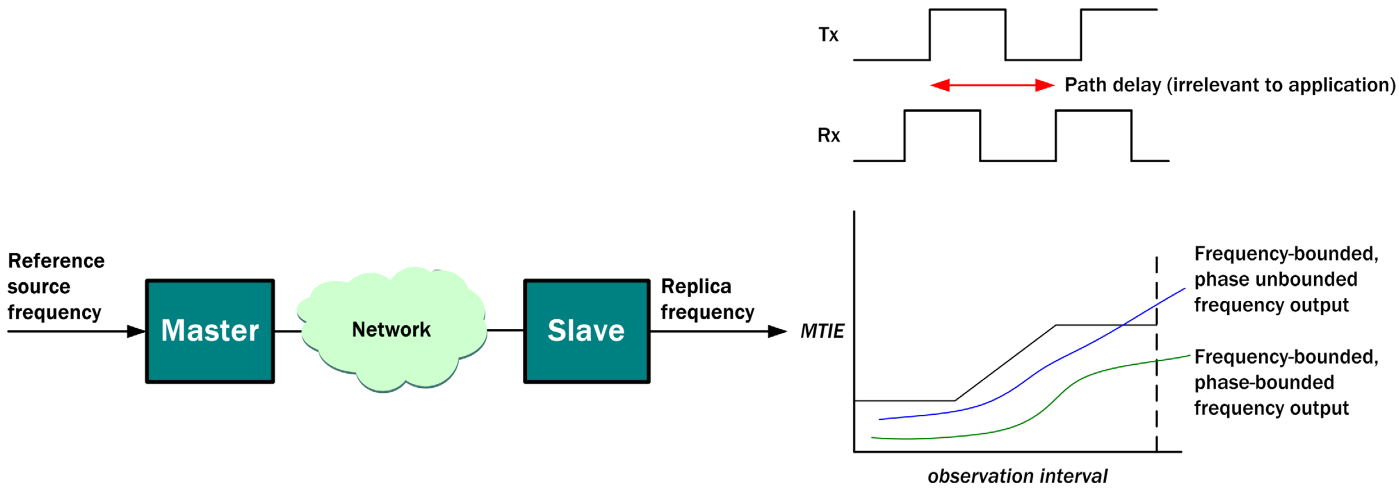

Figure 38 - Example of internally-generated timebase

There are two types of frequency delivery, in which the phase deviation is either bounded or unbounded. Both are examples of frequency-transfer, but have different applications. Bounded phase delivery is required by applications which need to protect buffers against overflow; circuit-emulation (e.g. psuedo-wire emulation end-to-end, PWE3) is an example of this sort of application. The performance requirement would be defined by MTIE and TDEV masks. Unbounded phase delivery is acceptable for applications where the frequency accuracy is the important parameter. Wireless basestations using frequency division duplex (FDD) technology are an example of where unbounded phase delivery can be used (although these have tended to obtain their timing from synchronized backhaul links, and so actually use bounded phase delivery by default).

An important difference between frequency-transfer and the previous applications is that there is no need to remove any path delay from the output of the OC. This follows traditional telecom practice; the path delay is not important to the application.

Figure 38 shows examples of bounded-phase and unbounded-phase frequency-transfer applications.

If the application requires a bounded-phase delivery of frequency, then all potential GMs that could be selected by an OC must have the same reference source (e.g., traceable to TAI or a telecom PRC). This ensures that they operate at the same rate so that, if a reference switch is necessary, the output phase can still be bounded. If the application requires an unbounded-phase delivery, potential GMs that could be selected by the OCs must all have references that are frequency-aligned within the margins required by the application.

A frequency-transfer application could use a reference source which has been derived from a non-TAI-traceable source, such as a telecom PRC or network clock. Depending upon the frequency at which the source operates, this could be supplied to an ACS9522-based GM and routed via the TDM Block; this differs from ToD and common-phase applications which have to route directly to the PTP Block.

Figure 39 shows an example of a PTP network in which two GMs, GM1 and GM2, are tied to the same reference source (a PRC) and so support a phase-bounded frequency-transfer application; at the same time, another GM, GM3, can support a ToD application.

Although a two-way flow is not obviously necessary for the delivery of a stable frequency, it has the benefit of overcoming the large phase plateaux that occur due to long-term variations in traffic load in wide-area packet networks. These phase plateaux can cause the requirements of, for example, G.8261[20] to be violated. Using a two-way flow therefore helps to meet the G.8261[20] standard.

In frequency-transfer applications, the timebase of the ACS9522 has an arbitrary phase with respect to recognized time scales. To indicate that the ACS9522 is not tied to a TAI-traceable time source, the PTP announce messages carry the following flag and field values:

PTP flag is FALSE (indicating that the timebase is not traceable to TAI).

L1 and L2 flags are FALSE.

timeTraceable flag is FALSE.

frequencyTraceable flag is TRUE.

currentUtcOffset field is invalid.

timeSource field is INTERNAL_OSCILLATOR.

clockClass field is as set by configuration (according to special profile in use).

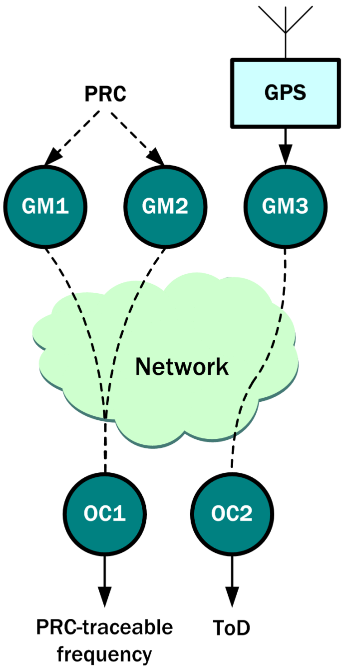

Figure 39 - Selection of GM must suit application needs

Sources of error in PTP networks

PTP is a two-way protocol. It requires timing messages to flow in each direction in order that the path delay can be calculated, and accounted for, when aligning the slave timebase to the GM. Any asymmetry between the path delays of sync and delay-request messages causes an offset in the slave timebase relative to the GM timebase. This offset is an error. Asymmetry can have many causes, including differential routing where the sync messages take a different path to the delay-request messages (static asymmetry) and load-dependent delay where the delay caused by waiting in loaded queues can be different in each direction (dynamic asymmetry). Asymmetries can also be caused by physical attributes of networking equipment such as differential delays in twisted-pair cables, unbalanced delays in optical cables due to dissimilar corrections of chromatic or polarity dispersion, and differential serialization/de-serialization delays in the transceivers.

NOTE: Static asymmetry can be compensated for within DPSync.

Measures can be taken to minimize the effects of asymmetries. For example, differential routing can be avoided by engineering the same route in each direction; similarly, load-dependent delay asymmetry can often be minimized by appropriate use of quality-of-service facilities. These are examples of how network engineering can be applied to improve the performance of a PTP link, and they are applied at a *network level*.

Other techniques can be applied to the *physical level* of a link to improve the performance in the face of physical-layer imperfections. Serialization/de-serialization phases are often readable from the transceivers and the asymmetry can thus be calculated.

Similarly, differential delays in the two directions of a link caused by un-balanced twisting in unshielded twisted pair (UTP) cabling can often be estimated with a high degree of accuracy: for example, an estimate of the average differential delay can be obtained by taking measurements on a sample of known length and scaling up the result to suit the length of the transmission cable used.

The length of the transmission cable can be estimated from the round-trip time, so that the total differential delay can be estimated automatically. This feature is not included in DPSync but can be easily implemented in the host code.

Differential delays in optical fibres due to chromatic or polarization dispersion comes into play when cables are many kilometers in length. A survey of the cable lengths can be useful in estimating differential delay. PTP v2 includes a correction field where any such information can be sent to the slave clock. DPSync will use this data to reduce the effects of asymmetry.

Influences on Grandmaster fan-out

PTP distributes the timebase of a GM clock to a population of slave clocks. The number of slaves that can be correctly controlled by an ACS9522 running as a PTP GM depends on several factors. An important consideration is the utilization figure of the port which is receiving the delay-request messages (the incoming port). If the utilization figure is too high, head-of-line blocking may occur. This can result in the accumulation of extra delay in the slave-to-master direction which, in turn, can lead to asymmetric delay and consequent time offset error.

The same characteristic also applies to the outgoing ports of all network switches that carry PTP delay-request messages to the GM. It is important therefore to limit the average utilization of the incoming port by carefully balancing the number of slaves and the message rate.

The utilization of the port transmitting the sync, delay-response and announce messages (the outgoing port), should also be considered as a limiting factor in the number of slaves that can be supported. The outgoing link carries all of the announce, sync and delay-response messages sent by the GM to its community of slaves. Announce and delay-response messages are classed as general messages in PTP. The sync and delay-request messages are classed as event messages. In a PTP system in which a slave performs PDV filtering, best performance is obtained when the rate of delay-request messages is approximately the same as the rate of sync messages.

Each delay-request message must be answered by a corresponding delay-response message, so the rate of delay-response messages is approximately the same as that of sync messages. (In comparison, the rate of announce messages is negligibly small.) If the full capacity of an outgoing fast Ethernet link (100 Mbaud) could be devoted to carrying PTP sync and delay-response messages, the maximum aggregate rate would be approximately 76,000 messages per second. On the incoming port, this would be matched by an equal rate of delay-request messages and would produce an average utilization of some 50%. This could be expected to cause significant head-of-line blocking on the incoming link, with frequent periods of additional queueing delay and a consequent time offset error.

Reducing the utilization of the incoming port to a value nearer 20%, for example, would improve the performance and produce an insignificant time offset error. A utilization value of 20% on an incoming fast Ethernet port would allow the port to handle approximately 30,000 PTP event messages per second which could, in principle, support a population of approximately 1000 slaves at 30 messages per second. A population of this size is useful for many applications using PTP Grandmasters that can support such a population. However, it should be noted that a number of 1000 slaves exceeds that which can be supported by an ACS9522 GM.

To support a larger community of slaves, companion ACS9522 devices in PTP GM mode can be used at the same time in a network. As dictated by the PTP best master clock algorithm, a GM enters the passive state if it detects another GM on the same sub-domain, and so each of the ACS9522s must operate in its individual sub-domain. The sub-domain can be configured via the API.

TDM timing

TDM-timing refers to the way timing has been transported around telecom networks for the last two decades. The requirements have been developed by various standards bodies, principally ITU-T and ANSI, with support from ETSI and OPTIX. The chief requirement has been to provide a clocking scheme which maintains phase movements of clocks at the edge of the network within tight bounds in order to minimize buffer spills and maintain data integrity. There has been no need to take path delay into account since the objective has been to prevent the instantaneous phase of a clock moving too far from an average position. A hierarchical approach has commonly been adopted, with a primary reference clock at the centre and a clock distribution scheme using clocking functions built into the networking equipment, plus additional specialized clocking equipment located in central offices where possible.

The clocking functionality that is built into networking equipment is called the Synchronous Equipment Timing System (SETS) and that of the central office is called the Synchronisation Supply Unit (SSU). An alternative name used in the ANSI market is Building Integrated Timing System (BITS).

The TDM timing mode of the ACS9522 provides most of the clocking functions that are required by a SETS; it lacks only a high-stability oscillator used to control the frequency drift in free-running or holdover situations. A TCXO is sufficient to meet the requirements in most applications, and an OCXO meets the requirements for other applications.

The TDM Block shares an oscillator with the PTP Block (the local oscillator). This oscillator may run at a frequency of 10MHz, 12.8 MHz or 20 MHz when the TDM Block is in use (the PTP Block can also use 10 MHz, 12.8 MHz and 20 MHz oscillators). The ACS9522 functionality needed in the TDM-timing mode is derived from that defined in ITU-T Recommendation G.783[11] and it meets the performance requirements defined in G.813[15] and/or G.812[14].

The primary requirement of a SETS function is to reduce wander noise on a selected reference signal, and a phase locked loop with a narrow filter bandwidth of typically a fraction of a Hertz is used for this. The output of the phase locked loop would be used to time outgoing signals which flow further downstream towards the edge of the network. In G.783[11], this signal is termed the T0 signal; another term in common usage for this signal is the equipment clock. The reference signal must be selected from a set of possible references, and it must be possible to switch to a standby reference signal if the primary reference is removed from service.

References can be classed into two types - those which are recovered from incoming synchronization-carrying traffic signals (usually called line-timing), and those coming from SSUs. As a general rule, if an SSU is available, then its output should be the primary reference used by networking equipment in the central office. Line-timing is usually held back as a standby reference in case of failure of the SSU. However, for equipment that is located either in outside plant or in a central office which does not have an SSU, then line-timing is likely to be the only option, and one direction of the line would be selected as the primary reference source.

Switching between reference sources must be done with the minimum of disruption to the output phase, and phase build-out is commonly used for this. Although switching between references should be automated, the selection of primary, secondary, tertiary, etc, references is usually done to suit an overall synchronisation plan defined by a network planner (in other words, the selection order is known in advance, but the network equipment must operate autonomously when a failure is detected).

Failures to timing trails can be internal to the equipment, such as faulty connectors, broken devices, and so on: or they can be external, such as cable breaks or failures upstream. The SETS function of the ACS9522 has the ability to detect a badly-behaving clock signal, but this is useful mostly for detecting problems which are internal to the equipment because many LIUs switch to a standby clock source if they detect a cable failure (and the standby clock source can be the transmit-side clock, thereby potentially causing a clocking loop).

Most failures that affect the timing trail would occur outside the equipment and these would be detected by other functions. For example, an LIU could detect a loss-of-signal condition, or a framer could detect loss-of-frame or AIS conditions. These conditions should be used by the equipment to disqualify that line from the set of possible references. However, failure conditions may be only temporary and a reference should not be rejected too quickly. In particular, switching away from the selected reference path too quickly, only to return to it soon afterwards, would be unfortunate as an unnecessary phase disturbance could have been introduced.

The ACS9522 supports two types of protection switching in the TDM Timing mode to protect the application against local and remote failures. Local failures are those which can be detected by the equipment in which the ACS9522 is used, see Table 51.

Table 51 Local failures in TDM Timing mode

Failure type	Anomaly/alarm	Action
Cable break	LOS	This anomaly/alarm is not detected by the ACS9522 but should be processed by the host control software. Await new priority tables and react accordingly (generally expect to select the next highest priority input source).
Internal clock-recovery or equipment distribution failure	Inactivity alarm	This anomaly/alarm is detected by the ACS9522. If the currently-selected input source is affected, switch to the next input source; else re-order the priority tables and interrupt the host control software.
Out of frequency	Off-frequency alarm	This anomaly/alarm is detected by the ACS9522. If the currently-selected input source is affected, switch to the next input source; else re-order the priority tables and interrupt the host control software.
Active SETS failure	Fast detector	This anomaly is usually detectable by a standby SETS function and/or one or more of the line cards taking the output clocks. Take the active SETS out of action, promote the standby SETS to become active, and switch-over on line cards. This is known as a *hardware switch*.
Maintenance activity	Various	If this causes the active and standby SETS functions to swap over, then this is known as a *hardware switch*.

Remote failures are those which have been detected in upstream equipment but which need action locally. These are detailed in Table 52.

Table 52 Remote failures in TDM Timing mode

Failure type	Anomaly/alarm	Action
Upstream failure	AIS	This anomaly/alarm is not detected by the ACS9522 but should be processed by the host control software. Await new priority tables and react accordingly (generally expect to select the next highest priority input source).
Upstream event	SSM change	This anomaly/alarm is not detected by the ACS9522 but should be processed by the host control software. Await new priority tables and react accordingly (generally expect to select the next highest priority input source).

G.783[11] defines how to use a hold-off time to maintain synchronisation network stability during temporary disturbances. To support this, the holdover mode of the ACS9522 can be used during the soak period. Similarly, a higher-priority reference should not be re-selected until it has been observed to be steady. Again, G.783[11] shows how to use a wait-to-restore period to ensure that a reversion to a returning reference is not made before the reference has proved itself to be truly available.

In addition to using the SETS function to generate the line clocks in networking equipment, the SETS function can also be required to route timing signals to an SSU or BITS. G.783[11] calls this signal the T4 signal (another term in common usage for this signal is the station clock). This would be required when the networking equipment is located in a central office but is not used in outside plant. The selection of the reference source for the T4 signal is separate to the selection of the reference for the T0 signal. In a typical case, the T4 signal is generated by locking a phase locked loop to an incoming line clock, while the T0 signal is generated by locking another phase locked loop to the signal coming from the SSU. The SETS function must therefore have two separate priority tables if it is to support both T0 and T4 signals. The same rules on qualifying/disqualifying references, and the use of hold-off and wait-to-restore times, apply to the T4 signal as to the T0 signal.

The SETS function of the ACS9522 provides the physical functions required to generate both T0 and T4 clock signals. It can individually filter the references and switch between them, independently for T0 and T4. The priority orders for both T0 and T4 signals can be downloaded into the device and it will switch automatically between the available references if the integrated monitors detect failures.

However, failure conditions which are external to the equipment must be detected elsewhere in the equipment (LOS, AIS, SSM, etc.). Also, to meet G.783[11] requirements, the hold-off timing and the wait-to-restore timing must be implemented elsewhere in the equipment.

Figure 40 shows how the TDM Block can interact with a BITS/SSU, highlighting the use of the various types of clock signal (i.e., T0 to T4).

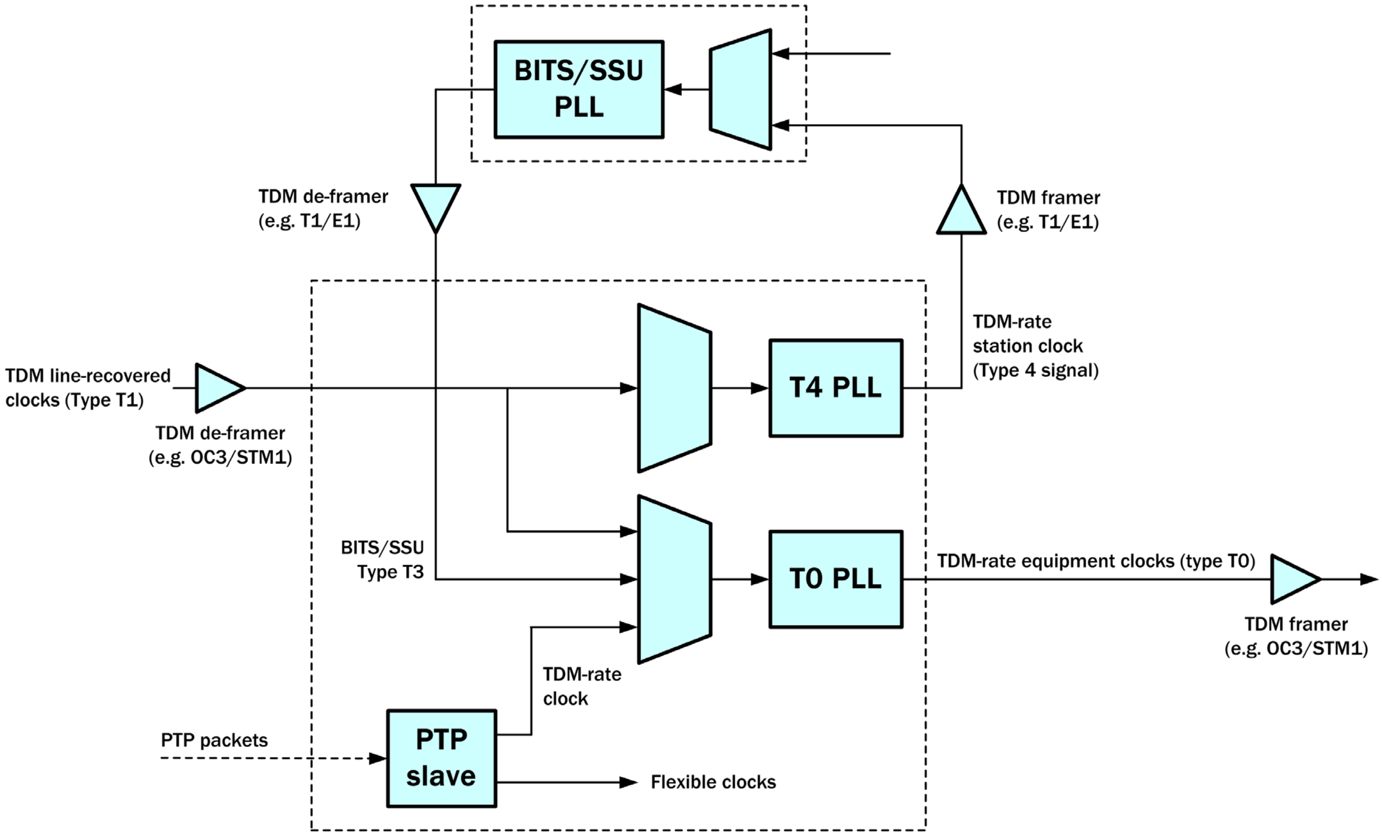

Figure 40 - Interactions between SETS function and SSU/BITS function

PACKAGE DETAILS

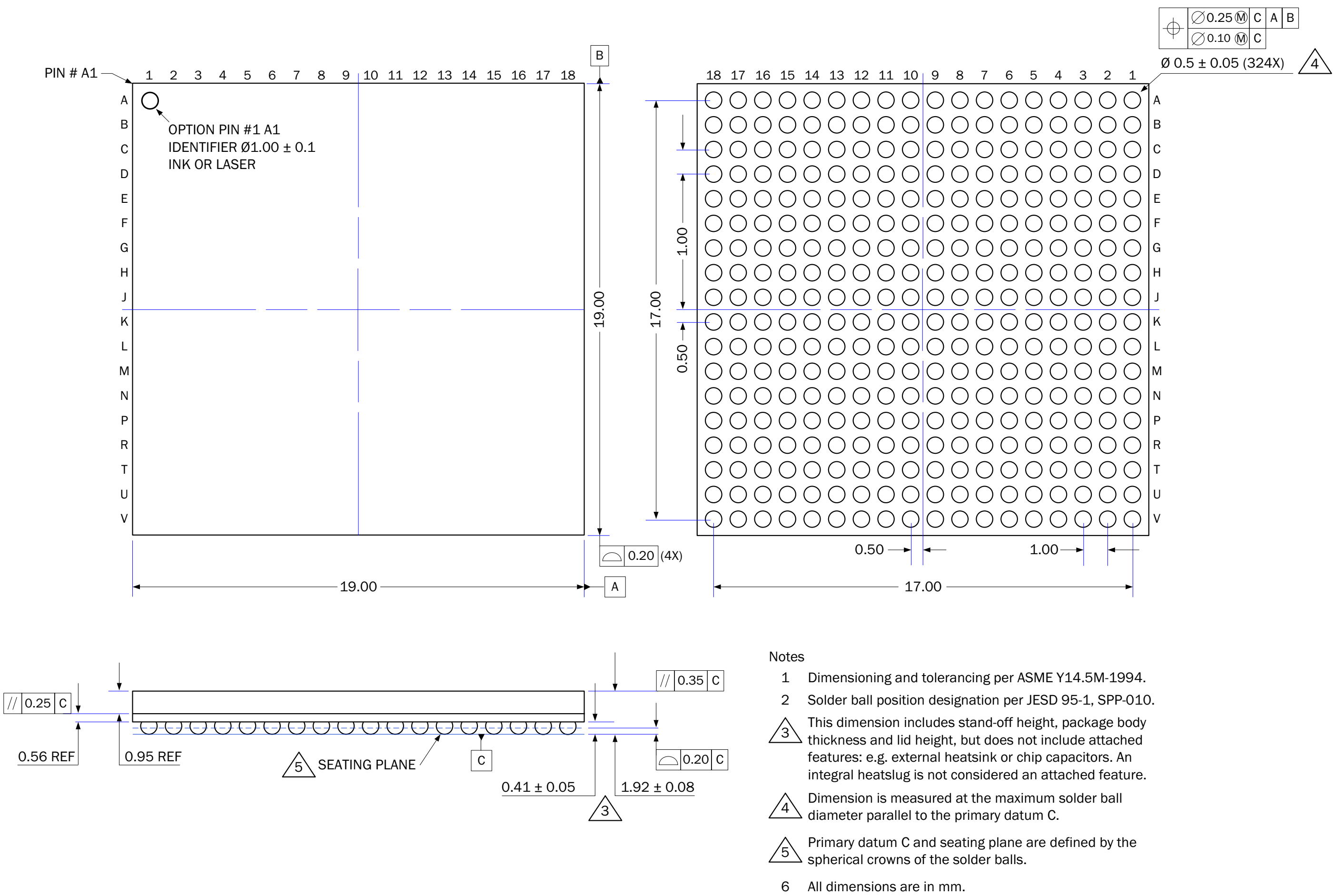

Figure 41 - LBGA package, 1.0 mm pitch, 19 mm x 19 mm x 1.92 mm, 324 balls

MSL level 3 and peak reflow temperature = 260°C
RoHS level = RoHS-6.
Terminal metallization (BGA balls) = SAC305.

Thermal conditions

The ACS9522 is rated for the full temperature range of -40°C to +85°C when this package is used with a PCB of eight layers or more.

Copper coverage must exceed 50%.

All balls must be soldered to the PCB.

Maximum operating temperature must be reduced, or an appropriate airflow must be used, when the ACS9522 is used with a PCB that does not meet these minimum requirements.

Table 53 ACS9522 thermal resistance

Parameter	Symbol	Airflow	Value (°C/W)
Theta-$_{JA}$ (thermal resistance - junction to ambient)	θ_{JA}	at 0 m/sec airflow at 1 m/sec airflow at 2 m/sec airflow	15.4 11.8 10.9
Theta-$_{JB}$ (thermal resistance - junction to board)	θ_{JB}		6.7
Theta-$_{JC}$ (thermal resistance - junction to case)	θ_{JC}		2.3

GENERAL INFORMATION

Acronyms and abbreviations

ADSL	Asymmetric Digital Subscriber Line
AMI	Alternate Mark Inversion
API	Application Programming Interface
APLL	Analogue Phase Locked Loop
ARB	Arbitrary Time Base (see IEEE 1588, v2)
ASSP	Application Specific Standard Product
BGA	Ball Grid Array
BITS	Building Integrated Timing Supply
BMC	Best Master Clock
BSDL	Boundary Scan Description Language
CAS	Column Address Strobe
CMU	Clock Multiplier Unit
DDS	Direct Digital Synthesis
DFS	Digital Frequency Synthesis
DPLL	Digital Phase Locked Loop
DS1	1544 kbit/s interface rate
DTO	Discrete Time Oscillator
E1	2048 kbit/s interface rate
EEC	Ethernet Equipment Clock
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
GM	Grandmaster
GPS	Global Positioning System
HBD	Human Body Model
IEEE	Institute of Electrical & Electronics Engineers
I/O	Input - Output
ITU	International Telecommunications Union
LIU	Line Interface Unit
LOF	Loss of Frame Alignment
LOS	Loss Of Signal
LQFP	Low profile Quad Flat Pack
LVDS	Low Voltage Differential Signal
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTL	Low Voltage Transistor - Transistor Logic
MAC	Media Access Controller
MII	Media Independent Interface
MTIE	Maximum Time Interval Error
NE	Network Element
OC	Ordinary Clock
OCXO	Oven Controlled Crystal Oscillator
PBO	Phase Build-out
PCB	Printed Circuit Board
PDH	Plesiochronous Digital Hierarchy
PDV	Packet Delay Variation
PFD	Phase and Frequency Detector
PHY	Physical Layer Device
PLL	Phase Locked Loop
POR	Power-On Reset

p-p	peak-to-peak
ppb	parts per billion
ppm	parts per million
PPS	Pulse Per Second
PRC	Primary Reference Clock
PTP	Precision Time Protocol (synonymous with 1588™)
PWE3	Psuedo Wire Emulation End-to-End
R/W	Read/Write
rms	root-mean-square
RO	Read Only
RoHS	Restrictive Use of Certain Hazardous Substances (directive)
SDH	Synchronous Digital Hierarchy
SEC	SDH/SONET Equipment Clock
SETS	Synchronous Equipment Timing Source
SGMII	Serial Gigabit Media Independent Interface
SONET	Synchronous Optical Network
SPI	Serial Peripheral Interface
SSM	Synchronous Status Messages
SSU	Synchronization Supply Unit
STM	Synchronous Transport Module
TAI	Temps Atomic International (International Atomic Time)
TBA	To be advised
TCXO	Temperature Compensated Crystal Oscillator
TDEV	Time Deviation
TDM	Time Division Multiplexing
ToD	Time of Day
TTL	Transistor - Transistor Logic
UART	Universal Asynchronous Receiver Transmitter
UDP	User Datagram Protocol
UI	Unit Interval
UTC	Universal Time, Coordinated
UTP	Unshielded Twisted Pair
W-CDMA	Wide Code Division Multiple Access, one of several 3G radio interface standards
WEEE	Waste Electrical and Electronic Equipment (directive)
3G	3rd Generation - an ITU specification for increased bandwidth cellular communications
3GPP	3rd Generation Partnership Project

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Product status/datasheet revision history

Product status

The relationship between the status of the ACS9522 within the product design cycle and this datasheet is shown in the right of the header bar at the top of the datasheet.

DRAFT DATASHEET signifies that the design is being realized but is not yet physically available. The datasheet gives advance notification of the intention of the design.

PRELIMINARY DATASHEET signifies that initial prototype devices are physically available. The content of the datasheet more accurately represents the realization of the product design.

FINAL DATASHEET signifies that the device is fully characterized. The datasheet contains measured parameter values instead of simulated values.

Datasheet revision

This datasheet is Revision 5.0, as shown in the left footer at the bottom of each page. The changes made to this document and a summary of previous revisions are listed in Table 54. For specific changes between earlier revisions of the datasheet, please refer to the earlier revisions (where available). Always use the latest revision of the datasheet.

Table 54 Revision history

Revision	Reference	Description of changes
1.0	All pages	First release of FINAL Datasheet for ACS9522.
2.0	Pages 12, 14	Details of PWM and DAC balls added to Figure 7 and Figure 2.
3.0	Page 168	TDM Module register 67 definition updated
4.0	Page 37 Page 42	Table 26 updated Fig 16 updated to add PORB.

Ordering information

Table 55 Parts list

Order code	Description
ACS9522IFALBGT	DPSync Timing-over-packet synchronization technology master/slave 1588 device. Lead (Pb)-free packaged version. RoHS and WEEE compliant.

Disclaimers

Life support - this product is not designed or intended for use in life support equipment, devices or systems, or other critical applications, and is not authorized or warranted for such use.

Right to change - changes may be made to this product without notice. Customers are advised to obtain the latest version of the relevant information before placing orders.

Compliance to relevant standards - operation of this device is subject to the user's implementation and design practices. It is the responsibility of users to ensure that equipment using this device is compliant to all relevant standards.

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