To Customer：_____

Realtime Clock Module

INS5T8900

Datasheet

Document Version 1.0

Released on Nov 26th, 2024

Ordering Information

Manufacture Part Number	Product Name	Description
INS5T8900-2DEY000Y00SA-S664	INS5T8900-S664	±5ppm @ -40℃~+85℃，SMD3225

Guangdong Dapu Telecom Technology Co., Ltd

Bldg 5, SSL Modern Enterprise Accelerator Zone, Dongguan City, Guangdong Province, PRC China

TEL:0086-0769-88010888 FAX:0086-0769-81800098

Revision History

Version	Change Contents	Prepared by	Revised Date
V1.0	First Issued		2024.11.26

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1 Overview

INS5T8900 is a high-accuracy I²C bus interface real-time clock with low power consumption. It embeds a 32.768KHz TCXO. The high precise temperature sensor and temperature compensated circuit ensure the high clock accuracy. It supports calendar (year, month, day, hour, minute, second), clock and timer functions etc. The SMD3225 package with only 1.0mm thickness makes it very suitable to be used in portable and small size electronic devices.

2 Block Diagram

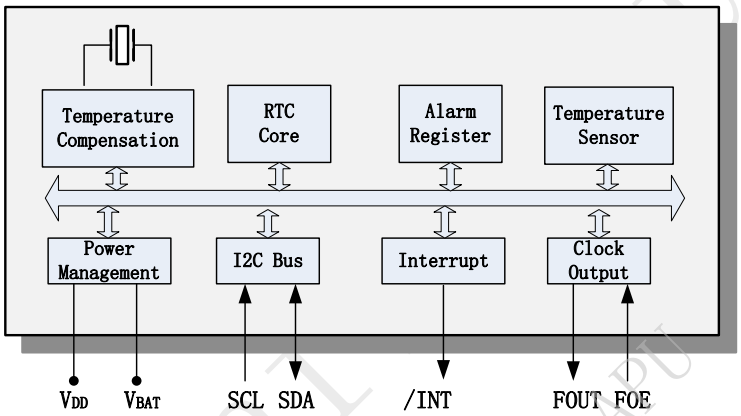


Figure 1. Block Diagram

3 Features

- Low current consumption: 1.0uA (Typ.)
- Power Supply Voltage: 1.6V ~ 5.5V
- Package: 3.2mm × 2.5mm × 1.0mm
- Operation Temperature Range: -40℃ ~ +85℃
- Communication Interface: I2C bus
- Leap years autocorrection
- Build-in TCXO: 32.768KHz
- Backup battery switchover function
- Build-in temperature sensor
- Timer output function with adjustable period
- High stability: ±5ppm @ -40℃ ~ +85℃

4 Pin definition

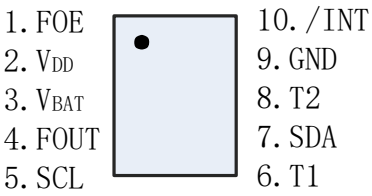


Table1. Pin Definition

Pin Number	Pin Name	I/O	Description
1	FOE	In	FOUT output control pin. “1” - enable FOUT, “0”- FOUT Hi-Z
2	V_{DD}	-	Power supply
3	V_{BAT}	-	Backup battery pin. Connect to large-capacity capacitors or a backup battery. Connect to V_{DD} when switchover function is not necessary
4	FOUT	Out	Frequency output. Controlled by FOE. Frequency can be set by FSEL bits.
5	SCL	In	I^2C clock signal
6	T1	-	Manufacturer test only. Ensure to be floating
7	SDA	In/Out	I^2C data signal
8	T2	-	Manufacturer test only. Ensure to be floating
9	GND	-	Ground
10	/INT	Out	Interrupt Output, Open-Drain; Waveforms can be output in backup mode;

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table2. Absolute Maximum Ratings

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage	V_{DD}	-0.3		6.5	V	
Backup Battery Voltage	V_{BAT}	-0.3		6.5	V	
Input Voltage	V_{IN}	GND-0.3		6.5	V	FOE, SCL, SDA input
Clock Output Voltage	V_{OUT1}	GND-0.3		V_{DD}+0.3	V	FOUT output
Output Voltage	V_{OUT2}	GND-0.3		6.5	V	SDA, /INT output
Storage temperature	T_{STG}	-55		125	℃	

5.2 Recommended Operating Conditions

Table3. Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage (normal mode)	V_{DD}	2.5	3.0	5.5	V	
Power Supply Voltage In case of single supply (V_{DD} = V_{BAT}) (Note 1)	V_{DD}	1.6	3.0	5.5	V	
Backup Battery	V_{BAT}	1.6	3.0	5.5	V	
Current consumption	I_{DD}		1.0		uA	Using Battery supply only
Operation temperature	T_{OPR}	-40	25	85	℃	

Note 1: To apply Min. value of V_{DD} and V_{BAT}, V_{CORE} need to be supplied with more than 2.5V at least for the oscillation to stabilize (oscillation start time t_{STA}).

Note2：After powered off, ensure that V_{DD} = V_{BAT} = GND for more than 10 seconds before next power on

Note3：If there is no special indication, the test conditions are GND = 0V, VDD = Vbat = 2.5V ~ 5.5V, Ta = - 40 ℃ ~ + 85 ℃

5.3 Frequency Characteristics

Table4. Frequency Characteristics

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Frequency stability	Δf/f	-5		+5	ppm	-40℃ ~ +85℃
Oscillation start time	t_{STA}			1	s	@25℃
Year Aging	f_a			±3	ppm	@25℃, First year

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Temperature Sensor Accuracy	T_{emp}			±5	℃	V_{DD}=3.0V
FOUT duty cycle	$t_{w/t}$	40	50	60	%	

Note：If there is no special indication, the test conditions are GND = 0V, VDD = Vbat = 2.5V ~ 5.5V, Ta = - 40 ℃ ~ + 85 ℃

5.4DC Characteristics

Table5. DC Characteristics

Parameter	Symbol	Value			Unit	Notes	
		Min.	Typ.	Max.			
Average Current consumption1	I_{DD1}		1.25	5.1	uA	V_{DD}=5.0V	f_{SCL}=0Hz, FOE=GND, /INT = V_{DD}; V_{DD}=V_{BAT}; FOUT off (High-Z); Compensation interval 2s; V_{DD} voltage detection time 2ms
Average Current consumption2	I_{DD2}		1.0	4.9		V_{DD}=3.0V	
Average Current consumption3	I_{DD3}		5.8	20	uA	V_{DD}=5.0V	f_{SCL}=0Hz, FOE=V_{DD}, /INT = V_{DD}; V_{DD}=V_{BAT}; FOUT:32.768kHz, CL=0pF; Compensation interval 2s; V_{DD} voltage detection time 2ms
Average Current consumption4	I_{DD4}		3.8	19		V_{DD}=3.0V	
High-level input voltage	V_{IH}	0.8*V_{DD}		5.5V	V	SCL, SDA, FOE pin	
Low-level input voltage	V_{IL}	GND-0.3		0.2*V_{DD}	V		
High-level output voltage	V_{OH1}	4.0		5.0	V	V_{DD}=5.0V, I_{OH} = -1mA	FOUT pin
	V_{OH2}	2.2		3.0		V_{DD}=3.0V, I_{OH} = -1mA	
	V_{OH3}	2.9		3.0		V_{DD}=3.0V, I_{OH} = -100uA	
Low-level output voltage	V_{OL1}	GND		GND+0.5	V	V_{DD}=5.0V, I_{OL} = 1mA	FOUT pin
	V_{OL2}	GND		GND+0.8		V_{DD}=3.0V, I_{OL} = 1mA	
	V_{OL3}	GND		GND+0.1		V_{DD}=3.0V, I_{OL} = 100uA	
	V_{OL4}	GND		GND+0.25	V	V_{DD}=5.0V, I_{OL} = 1mA	/INT pin
	V_{OL5}	GND		GND+0.4		V_{DD}=3.0V, I_{OL} = 1mA	
	V_{OL6}	GND		GND+0.4	V	V_{DD}≥3.0V, I_{OL} = 3mA	SDA pin
Input leakage current	I_{LK}	-0.5		0.5	uA	FOE, SDA, SCL pin, V_{IN} = V_{DD} or GND	
Output leakage current	I_{OZ}	-0.5		0.5	uA	FOUT, SDA, /INT pin, V_{IN} = V_{DD} or GND	

Note：If there is no special indication, the test conditions are GND = 0V, VDD = Vbat = 2.5V ~ 5.5V, Ta = - 40 ℃ ~ + 85 ℃

5.5 AC Characteristics

Table6. AC Characteristics

V_{DD}=2.5V ~ 5.5V; Ta=-40℃ ~ +85℃

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}			400	kHz
SCL low level time	t_{LOW}	1.3			us
SCL high level time	t_{HIGH}	0.6			us
Start condition setup time	$t_{HD;STA}$	0.6			us
Start condition hold time	$t_{SU;STA}$	0.6			us
Stop condition setup time	$t_{SU;STO}$	0.6			us
Bus idle time between start condition and stop condition	t_{RCV}	1.3			us
Data setup time	$t_{SU;DAT}$	100			ns
Data hold time	$t_{HD;DAT}$	0			ns
SCL, SDA rising time	t_r			0.3	us
SCL, SDA falling time	t_f			0.3	us

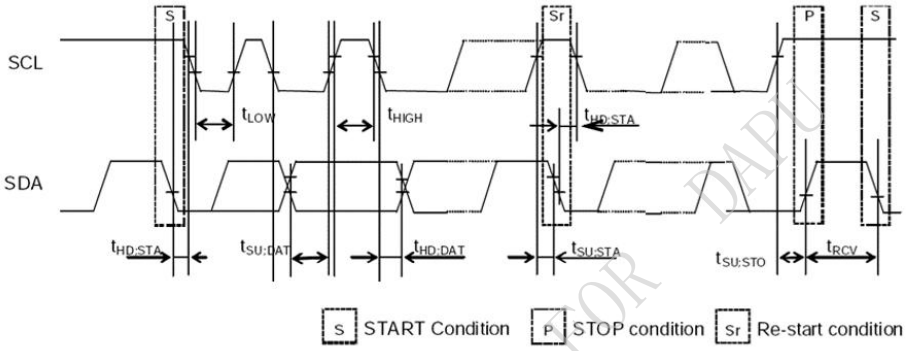


Figure 2. I^2C bus Timing Chart

Note: when the master equipment accesses the equipment through I2C bus, all communication from sending start condition to sending stop shall be completed within 1 second. If it exceeds 1 second, the I2C bus interface will be reset through the internal bus timeout function.

6 Registers

6.1 Register Lists

Address 0x00~0x0F: Basic Time and Calendar Registers

Address 0x10~0x1F: Extended Register Group 1

Address 0x20~30: Extended Register Group 2

Note: 0x10~16 and 0x00~06 with the same function, 0x1B~1F and 0x0B~0F with the same function

Table7. Basic Time and Calendar Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x00	SEC	○	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				R/W
0x01	MIN	○	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R/W
0x02	HOUR	○	○	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0x03	WEEK	○	6	5	4	3	2	1	0	R/W
0x04	DAY	○	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x05	MONTH	○	○	○	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				R/W
0x06	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				R/W
0x07	RAM	●	●	●	●	●	●	●	●	R/W
0x08	MIN Alarm	AE	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R/W
0x09	HOUR Alarm	AE	●	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0x0A	WEEK Alarm	AE	6	5	4	3	2	1	0	R/W
	DAY Alarm		●	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x0B	Timer Counter 0	128	64	32	16	8	4	2	1	R/W
0x0C	Timer Counter 1	●	●	●	●	2048	1024	512	256	R/W
0x0D	Extension Register	TEST	WADA	USEL	TE	FSEL [1]	FSEL [0]	TSEL [1]	TSEL [0]	R/W
0x0E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET	R/W
0x0F	Control Register	CSEL [1]	CSEL [0]	UIE	TIE	AIE	○	○	RESET	R/W

Table8. Extended Register Group 1

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x10	SEC	○	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				R/W
0x11	MIN	○	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R/W

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x12	HOUR	○	○	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0x13	WEEK	○	6	5	4	3	2	1	0	R/W
0x14	DAY	○	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x15	MONTH	○	○	○	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				R/W
0x16	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				R/W
0x17	TEMP	128	64	32	16	8	4	2	1	R
0x18	Backup Function	○	○	○	○	VDET OFF	SWOFF	BKSMP [1]	BKSMP [0]	R/W
0x19	Not use	○	○	○	○	○	○	○	○	R
0x1A	Not use	○	○	○	○	○	○	○	○	R
0x1B	Timer Counter 0	128	64	32	16	8	4	2	1	R/W
0x1C	Timer Counter 1	●	●	●	●	2048	1024	512	256	R/W
0x1D	Extension Register	TEST	WADA	USEL	TE	FSEL [1]	FSEL [0]	TSEL [1]	TSEL [0]	R/W
0x1E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET	R/W
0x1F	Control Register	CSEL [1]	CSEL [0]	UIE	TIE	AIE	○	○	RESET	R/W

Table9. Extended Register Group2

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x20	Device ID	Vendor ID[3:0]				Ver[3:0]				R
0x21	Control Register 1	Reserved: Ensure to be 0x8				○	○	○	VBATSW	R/W
0x22-26	RSV	Reserved: Ensure to be 0x00								R
0x27	SubSEC	Reserved				SubSEC[3:0]				R
0x28-30	RSV	Reserved: Ensure to be 0x00								R/W

Note:

1, After power-up reset or in case VLF bit returns “1”, make sure to initialize all registers to default state before using the RTC. Ensure all inputs are in the required range and the defined values are set for the reserved bits in case the clock cannot work normally.

- ✓ During the initial power-up, below bits will be in the state as below:

  Initial 0:TEST, WADA, USEL, TE, FSEL[1:0], TSEL[0], UF, TF, AF, CSEL[1], UIE, TIE, RESET, VDETOFF, SWOFF, BKSMP[1:0], VBATSW.

  Initial 1: VLF, VDET, CSEL[0].

- ✓ All other register values are undefined, so make sure to reset the module before using it.
- ✓ The bits marked with “○” can be read out “0” only after initializing.
- ✓ The bits marked with “●” are RAM bits which can be used to write or read any data.

- ✓ Only 0 can be written to UF, TF, AF, VLF, VDET bits.
- ✓ Make sure “0” to be written for TEST bits which are used for testing only.
- ✓ Reserved bits must be set to the defined values accordingly.

6.2 Details of Registers

6.2.1 Clock counter registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x00/10	SEC	○	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				0x00
0x01/11	MIN	○	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x00
0x02/12	HOUR	○	○	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				0x00

SEC: BCD format, Value: 0~59

MIN: BCD format, Value: 0~59

HOUR: BCD format, Value: 0~23

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x03/13	WEEK	○	6	5	4	3	2	1	0	0x40

WEEK: Value 01h, 02h, 04h, 08h, 10h, 20h, 40h. Only one bit can be set to 1 each time, all others must be set to 0.

Table10. WEEK Register

WEEK	Data	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sunday	01h	0	0	0	0	0	0	0	1
Monday	02h	0	0	0	0	0	0	1	0
Tuesday	04h	0	0	0	0	0	1	0	0
Wednesday	08h	0	0	0	0	1	0	0	0
Thursday	10h	0	0	0	1	0	0	0	0
Friday	20h	0	0	1	0	0	0	0	0
Saturday	40h	0	1	0	0	0	0	0	0

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x04/14	DAY	○	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				0x01

DAY: BCD format, the value range will be adjusted automatically according to the month setting and if a leap year or not .

Table11. DAY Register Value

Month	Day Value Range
1, 3, 5, 7, 8, 10, 12	1~31
4, 6, 9, 11	1~30

Month	Day Value Range
February in normal year	1~28
February in leap year	1~29

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x05/15	MONTH	○	○	○	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				0x01
0x06/16	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				0x00

MONTH: BCD format, Value1~12

YEAR: BCD format, Value0~99(2000~2099)

Example: 2020/01/01 Wednesday 21:18:36

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x00/10	SEC	○	0	1	1	0	1	1	0
0x01/11	MIN	○	0	0	1	1	0	0	0
0x02/12	HOUR	○	○	1	0	0	0	0	1
0x03/13	WEEK	○	0	0	0	1	0	0	0
0x04/14	DAY	○	○	0	0	0	0	0	1
0x05/15	MONTH	○	○	○	0	0	0	0	1
0x06/16	YEAR	0	0	1	0	0	0	0	0

6.2.2 Alarm registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x08	MIN Alarm	AE	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x00
0x09	HOUR Alarm	AE	●	BCD code, Hour tens place, 0-2		BCD code, Minute ones place, 0-9				0x00
0x0A	WEEK Alarm	AE	6	5	4	3	2	1	0	0x00
	DAY Alarm		●	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				

According to AIE, AF, WADA bits setting, the alarm interrupt will be generated once the current time match the settings in the above registers, the /INT pin goes to low level and AF bit is set to '1' to record an alarm interrupt event has occurred.

WEEK Alarm/DAY Alarm: Controlled by WADA bit in 0x0D register

AE: Alarm Enable bit, 0-enable; 1-disenable

AF: Defined in 0x0E register bit3

AIE: Defined in 0x0F register bit3

6.2.3 Timer control registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0B/1B	Timer Counter 0	128	64	32	16	8	4	2	1	0x00
0x0C/1C	Timer Counter	●	●	●	●	2048	1024	512	256	0x00

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
	1									

According to TE, TF, TIE, TSEL[1:0] bits setting, a timer interrupt will be generated once the value counts down to 0 from the one set in the above registers.
TE: Defined in 0x0D register bit4
TF: Defined in 0x0E register bit4
TIE: Defined in 0x0F register bit4
TSEL[1:0]: Defined in 0x0D register bit1 and bit0

6.2.4 Extension registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0D/1D	Extension Register	TEST	WADA	USEL	TE	FSEL[1]	FSEL[0]	TSEL[1]	TSEL[0]	0x02

TEST: Test bit, must be set to “0”
WADA: Week Alarm/Day Alarm control bit, decide 0x0A register as DAY Alarm or WEEK Alarm. 0-WEEK alarm, 1-DAY alarm
USEL: Update Interrupt Select bit, 0-output interrupt once a second, 1-output interrupt once a minute
TE: Timer Enable bit, 0-disenable, 1-enable; Timer counter can update new config when TE from “0” to “1”;

FSEL[1], FSEL[0]: FOUT frequency setting:

FSEL[1]	FSEL[0]	FOUT Frequency
0	0	32.768KHz (Default)
0	1	1024Hz
1	0	1Hz
1	1	32.768KHz

TSEL[1], TSEL[0]: Timer countdown period(source clock) setting:

TSEL[1]	TSEL[0]	Source clock
0	0	4096Hz
0	1	64Hz
1	0	1Hz
1	1	1/60Hz

6.2.5 Flag registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0E/1E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET	0x03

UF: Update flag bit. When time update interrupt event occurs, it will be set to “1” and keeps “1” until a “0” is written to it.
TF: Timer Flag bit. When a fixed-cycle timer interrupt event occurs, it will be set to “1” and keeps “1” until a “0” is written to it.
AF: Alarm Flag bit. When an alarm interrupt event occurs, it will be set to “1” and keeps “1” until a “0” is written to it.

VLF: Voltage Low Flag bit. When supply voltage is lower than 1.4V, it will be set to “1” and keeps “1” until a “0” is written to it.
VDET: Voltage Detection Flag bit. When supply voltage is lower than 2.1V, it will be set to “1” and keeps “1” until a “0” is written to it.

6.2.6 Control registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0F/1F	Control Register	CSEL [1]	CSEL [0]	UIE	TIE	AIE	○	○	RESET	0x40

CSEL[1], CSEL[0]: Compensation interval Select 1, 0 bits, used to set temperature compensation interval.

CSEL[1]	CSEL[0]	Compensation interval
0	0	0.5s
0	1	2s(default)
1	0	10s
1	1	30s

UIE: Update Interrupt Enable bit. When UF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disenable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).
TIE: Timer Interrupt Enable bit: When TF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disenable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).
AIE: Alarm Interrupt Enable bit: When AF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disenable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).
RESET: Reset IC, prepared for the synchronized starting of time or timer.

6.2.7 Temperature register

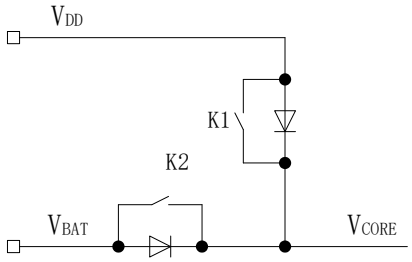
Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x17	TEMP	128	64	32	16	8	4	2	1	0x00

Read digital temperature data, Temp [℃] = (TEMP[7:0] * 2 -187.19) / 3.218.

6.2.8 Battery Backup switchover register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x18	Backup Function	○	○	○	○	VDET OFF	SWOFF	BKSMP [1]	BKSMP [0]	0x00

This register controls the power switchover function. Once abnormal VDD is detected, it will be switched to use battery as the power supply.
The power circuit diagram is shown below:



VDETOFF (Voltage Detector OFF): Main power supply VDD voltage detection control bit. 0-enable detection function (Default), VDD voltage will be detected once a second; 1-disenable detection function.
SWOFF (Switch OFF): Switch K1 control bit. 0- close (Default); 1- open
BKSMP[1], BKSMP[0](Backup mode Sampling time): Control the voltage detection sampling time. Default: 00.

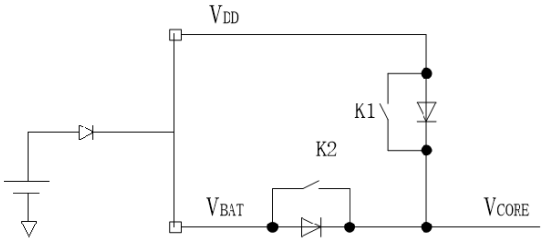


Table12. V_{DD} Voltage Sampling Time

VDD Detect Function	VDETOFF	SWOFF	BKSMP [1]	BKSMP [0]	V_{DD} Voltage Sampling Time	Switch K1 ON/OFF	Notes
ON	0	X	0	0	2ms	2ms OFF	Default
			0	1	16ms	16ms OFF	
			1	0	128ms	128ms OFF	
			1	1	256ms	256ms OFF	
OFF	1	0	x	x	OFF	ON	K1 Close
		1	x	x	OFF	OFF	K1 Open

6.2.9 Device ID register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x20	Device ID	VendorID[3:0]				Ver[3:0]				0xD2

VendorID[3:0]: The fixed value is defined as VendorID[3:0]=1101b=Dh to represent DAPU.
Ver[3:0]: version of the IC

6.2.10 Control Register 1

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x21	Control Register 1	Reserved: must be 0x8				○	○	○	VBATSW	0x80

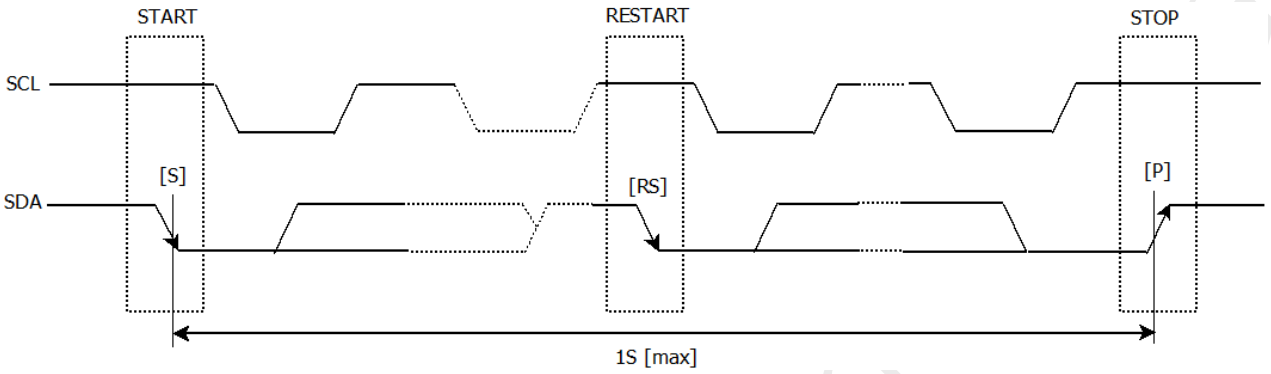
VBATSW： Battery supply switch K2 control bit. Default 0, 0- Open, 1-Close.

6.2.11 Sub-second timer register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x27	SubSEC	Reserved				SubSEC[3:0]				0x00

SubSEC[3:0]: sub second bit, and unit is 1/16s.

7 I²C Bus Interface



I²C bus supports bi-directional communications through a serial clock line SCL and a serial data line SDA. I²C bus device can be defined as “Master” and “Slave”. INS5T8900 can only be used as Slave.

7.1 Cautions

I²C bus includes START, RESTART, STOP conditions, the duration between START and STOP must be less than 1 second just in case the bus to be set to standby mode automatically. A new START condition must be transferred before restarting of any communications.

INS5T8900 I²C bus interface supports single byte read/write operations as well as multiple bytes incremental access. After 0xFF address, the next one will be 0x00.

7.2 Slave Address

Table13. I²C Bus Slave Address

Transfer data	Slave address							R/W
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
65h (Read)	0	1	1	0	0	1	0	1 (Read)
64h (Write)								0 (Write)

INS5T8900 I²C bus Slave Address is [0110 010*].

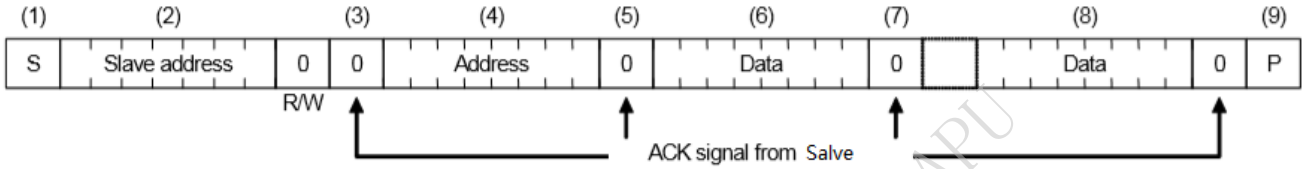
7.3 I²C bus protocol

It is assumed CPU is master and INS5T8900 is slave in this section.

7.3.1 Write process

I²C bus includes an address auto-increment function, once the initial address has been specified, the INS5T8900 increments (+1) the address automatically after each data is sent, then to write next data.

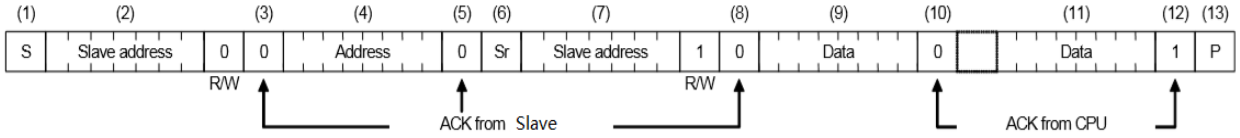
(1) CPU sends start condition[S]
(2) CPU sends INS5T8900's slave address with R/W bit to set to write mode
(3) CPU verifies ACK signal from INS5T8900
(4) CPU sends write address to INS5T8900
(5) CPU verifies ACK signal from INS5T8900
(6) CPU sends write data to the address specified at step (4)
(7) CPU verifies ACK signal from INS5T8900
(8) Repeat (6) (7) if multiple bytes need to be written, address will be incremented automatically
(9) CPU ends stop condition[P]



7.3.2 Read process

Writing the address to be read with write mode firstly, then reading the data with read mode.

(1) CPU sends start condition[S]
(2) CPU sends INS5T8900's slave address with R/W bit to set to write mode
(3) CPU verifies ACK signal from INS5T8900
(4) CPU sends address for reading from INS5T8900
(5) CPU verifies ACK signal from INS5T8900
(6) CPU sends RESTART condition [Sr]
(7) CPU sends INS5T8900's slave address with R/W bit to set to read mode
(8) CPU verifies ACK signal from INS5T8900
(9) CPU reads data from the specified address in step (4)
(10) CPU sends ACK signal for "0"
(11) Repeat (9) (10) if multiple bytes need to be read, address will be incremented automatically
(12) CPU sends ACK signal for "1"
(13) CPU sends stop condition[P]



8 Reflow Soldering Curve

Standard: IPC/JEDEC J-STD-020

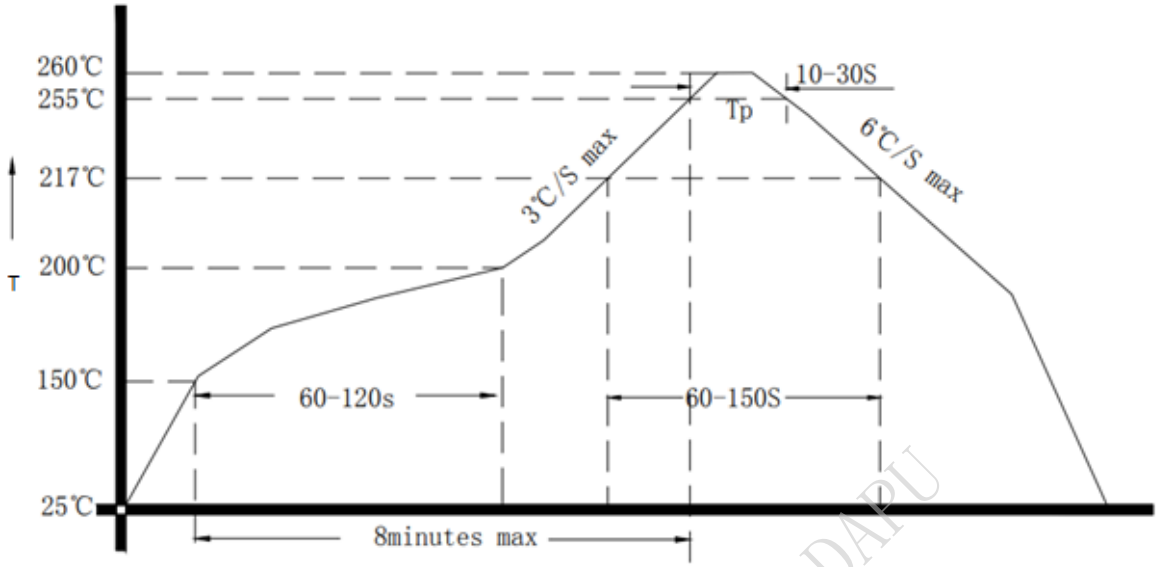
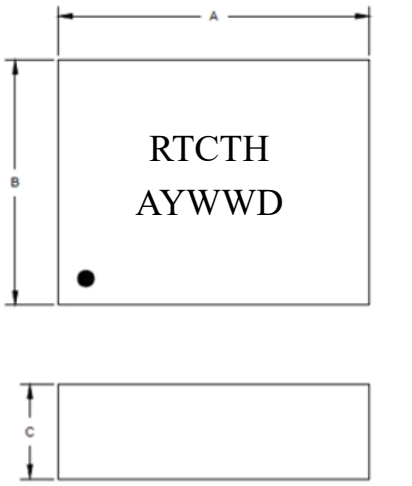


Figure 3. Reflow Soldering Curve

Note: It is suggested to solder IC under the condition shown in the curve above. Must pay attention to the temperature and time when manual soldering, if the temperature over +260℃, or you will make the xo performance bad, even damage it.

9 Dimensions



Dimension	Min.	Typ.	Max.
A	3.0	3.2	3.4
B	2.3	2.5	2.7
C	--	1.0	--
E	--	0.3	--
F	--	0.4	--
G	--	0.6	--
H	--	1.3	--
F1	--	0.45	--
F2	--	0.3	--

Unit：mm

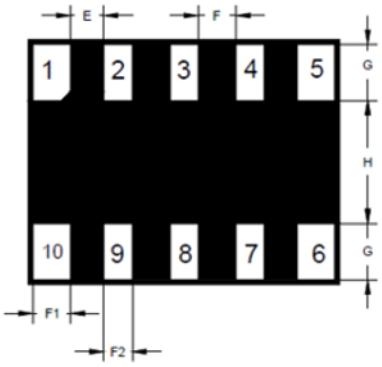
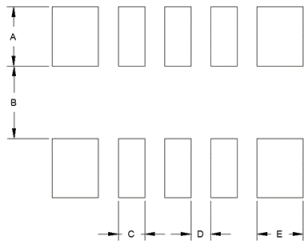


Figure 4. Dimension



Dimension	Max.
A	0.9
B	1.1
C	0.4
D	0.3
E	0.7

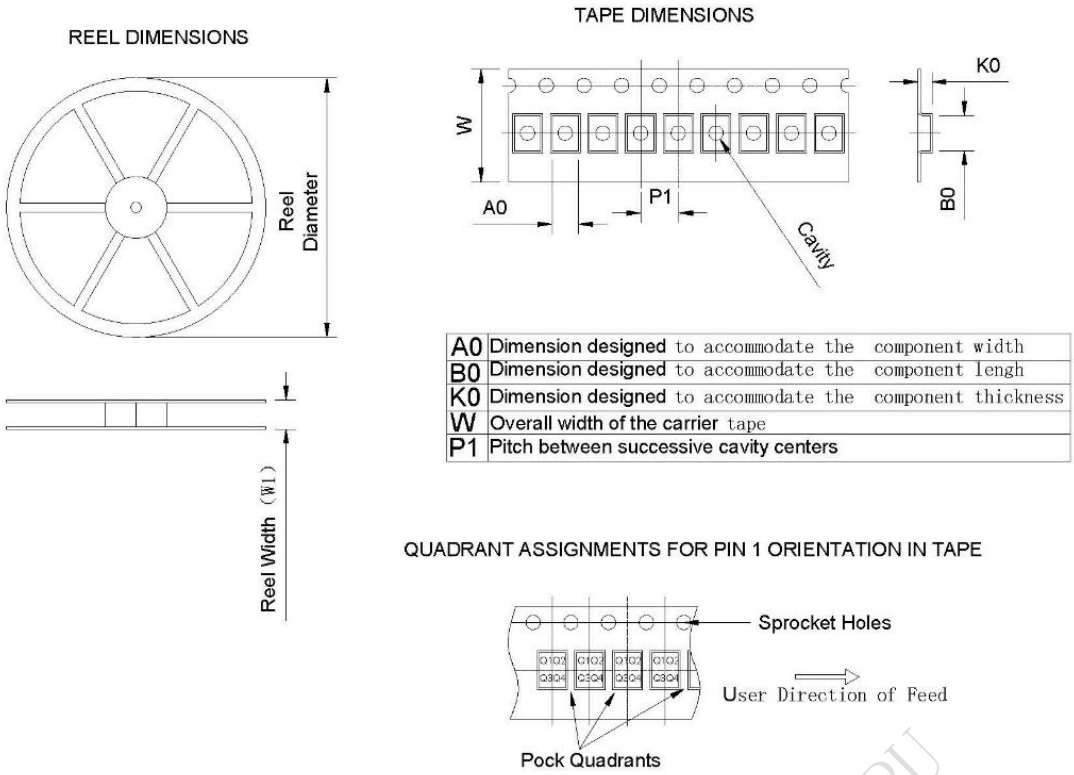
Unit：mm

Figure 5. Recommended Soldering Pattern

Marking

●	Pin #1 indicator
RTCTH	Fixed Code
A	Fixed Code
Y	Year Code, Last digit of Year “4” for 2024, “5” for 2025(for example)
WW	Work week is “01” to “52”
D	Supplier Code

10 Package



Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	PIN1 Quadrant
INS5T8900-2DEY000Y00SA-S664	SMD3225	10	3000	180	11.6±2.0	3.00	3.70	1.50	4.00	8.00	Q1

Figure 6. Package

11 Reference design circuits

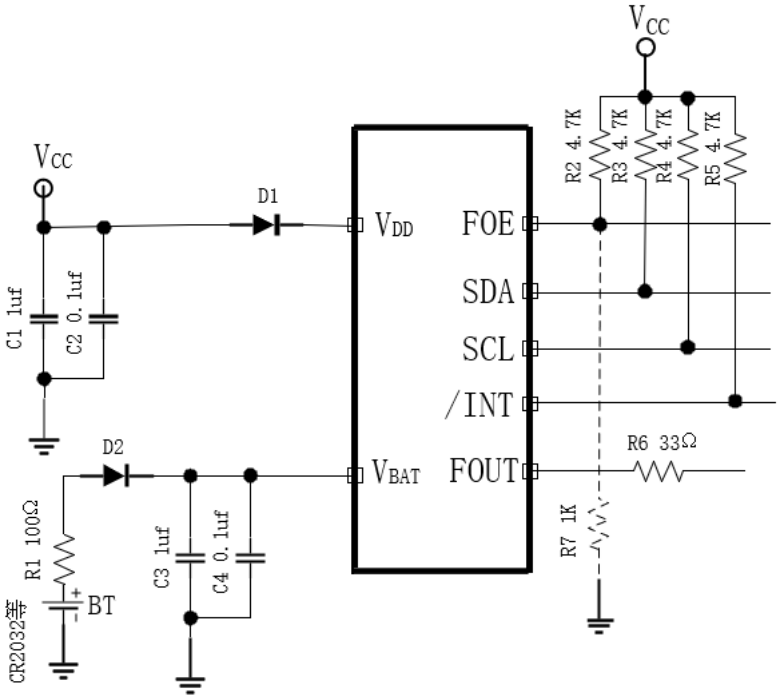


Figure 7. Non-rechargeable battery

Notes：

1. D1, D2 is Schottky diodes
2. FOE pin is forbidden to floating, pull up or pull down according to necessary
3. Recommend FOUT connect to test point or floating when not using
4. VDD power on time, tr < 50ms
5. The value is for reference only, please adjust according to specific design

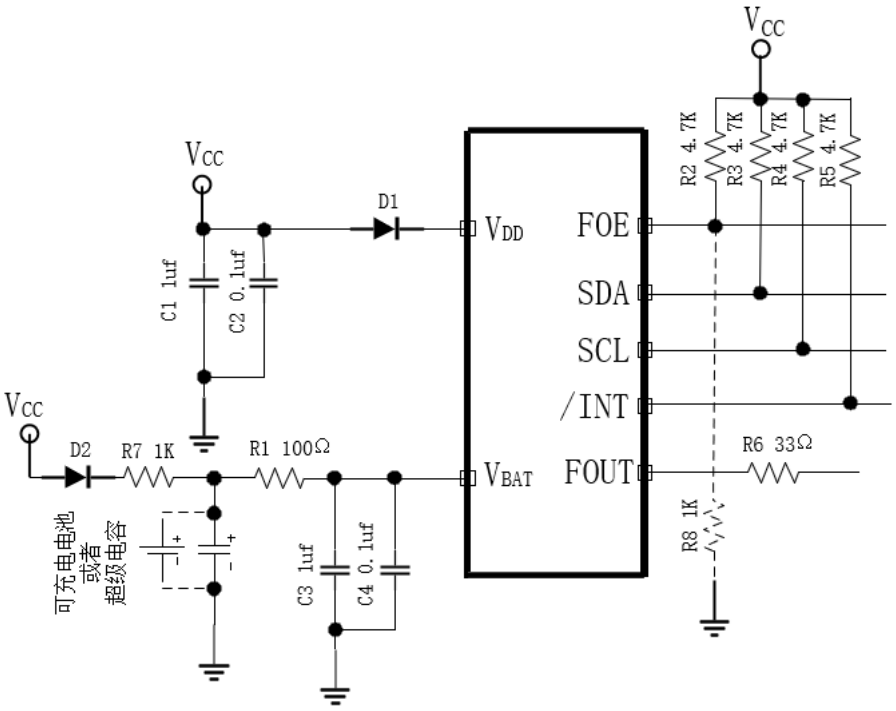


Figure 8. Rechargeable battery & Supercapacitors

Notes:

1. D1, D2 is Schottky diodes
2. The resistance R7 needs to be calculated based on the actual charging current
3. FOE pin is forbidden to floating, pull up or pull down according to necessary
4. Recommend FOUT connect to test point or floating when not using
5. VDD power on time, tr < 50ms
6. The value is for reference only, please adjust according to specific design

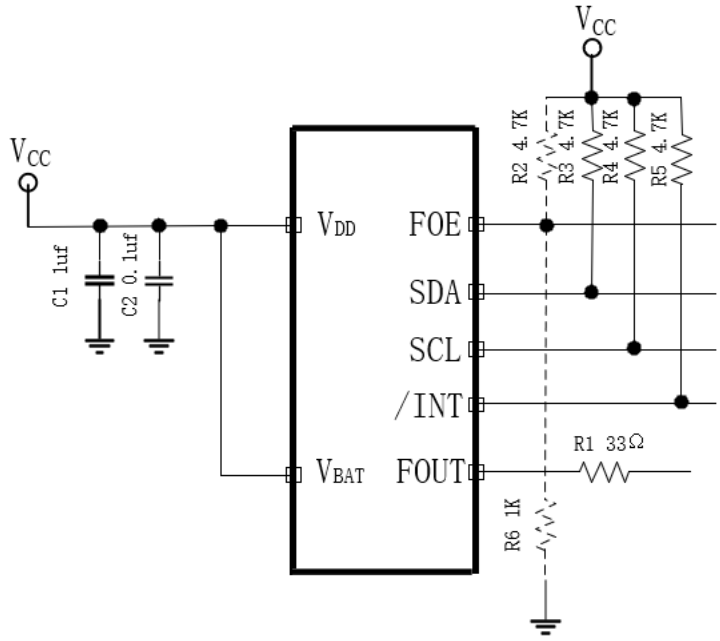


Figure 9. Single supply VDD

Notes:

1. FOE pin is forbidden to floating, pull up or pull down according to necessary
2. Recommend FOUT connect to test point or floating when not using
3. VDD power on time, tr < 50ms
4. The value is for reference only, please adjust according to specific design

12 Power-on initialization configuration

When the RTC supply voltage VDD beyond the range defined in the specification, it may cause the RTC to work abnormally. Therefore, when the system is powered on normally, the following code is added to the power-on initialization function of the MCU to ensure that the RTC works normally:

Reference Code：

```
reg:0x30=0xD1
if (reg:0x41 bit[7]=1'b1)
{
    reg:0x40=0x00
    reg:0x32=0x81
```

```
        delay_ms(50)          //delay 50ms
        reg:0x32=0x80
        delay_ms(50)          //delay 50ms
        reg:0x32=0x04
        if (reg:0x20=0xD2)
        {
            if (reg:0x5C bit[3:0]=4'b0101)
            {
                reg:0x5C bit[3]=1'b1
                delay_ms(50)          //delay 50ms
                reg:0x5C bit[3]=1'b0
            }
        }
          reg:0x30=0
    }
else
    {   reg:0x32 =0x66
        reg:0x32 =0x77
        reg:0x32 =0x83
        reg:0x32 =0x94
        reg:0x36 bit[2] =1'b1
        reg:0x36 bit[2] =1'b0
        reg:0x32=0x00
    }
```