

To Customer: \_\_\_\_\_

# Realtime Clock Module

## INS5A4000

## Datasheet

Document Version 1.0

Released on Jan 14th, 2025

### Ordering Information

| Manufacture Part Number | Product Name | Description |  |
|-------------------------|--------------|-------------|--|
| INS5A4000ASGX           | INS5A4000    | Option A    | $\pm 5\text{ppm}@-40^{\circ}\text{C}\sim+85^{\circ}\text{C}$   |
| INS5A4000BSGX           | INS5A4000    | Option B    | $\pm 8\text{ppm}@85^{\circ}\text{C}\sim+105^{\circ}\text{C}$   |
| INS5A4000CSGX           | INS5A4000    | Option C    | $\pm 50\text{ppm}@105^{\circ}\text{C}\sim+125^{\circ}\text{C}$ |
| INS5A4000DSGX           | INS5A4000    | Option D    | 0.43uA(Typ)  |
| INS5A4000ESGX           | INS5A4000    | Option E    | LGA3225  |

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# 1 Overview

The INS5A4000 is a high-accuracy SPI bus interface real-time clock with low power consumption and wide operation temperature range. It embeds a 32.768KHz TCXO. The high precise temperature sensor and temperature compensated circuit ensure the high clock accuracy. It supports calendar (year, month, day, hour, minute, second) with a leap-year correction, time alarm, wakeup timer, time update interrupt, clock output, internal status output and two times stamp function that can record two times and dates when an event occurs. This product is capable of low power consumption and automotive applications.

# 2 Key Features

|  |   |
|--|---|
| <ul style="list-style-type: none"> <li>● Low current consumption: 430nA (Typ.)</li> </ul>  | <ul style="list-style-type: none"> <li>● AEC-Q100 compliant</li> </ul>  |
| <ul style="list-style-type: none"> <li>● High stability:<br/> <math>\pm 5\text{ppm @ } -40^{\circ}\text{C} \sim 85^{\circ}\text{C}</math>; <math>\pm 8\text{ppm @ } 85^{\circ}\text{C} \sim 105^{\circ}\text{C}</math>;<br/> <math>\pm 50\text{ppm @ } 105^{\circ}\text{C} \sim 125^{\circ}\text{C}</math>;</li> </ul> | <ul style="list-style-type: none"> <li>● Support calendar, time alarm, wakeup timer, time update interrupt, clock output, internal status output and time stamp function</li> </ul> |
| <ul style="list-style-type: none"> <li>● Build-in TCXO: 32.768KHz</li> </ul>   | <ul style="list-style-type: none"> <li>● Self-monitor function</li> </ul>   |
| <ul style="list-style-type: none"> <li>● Operation Temperature Range: <math>-40^{\circ}\text{C} \sim +125^{\circ}\text{C}</math></li> </ul>  | <ul style="list-style-type: none"> <li>● Size: <math>3.2\text{mm} \times 2.5\text{mm} \times 1.0\text{mm}</math> (LGA)</li> </ul>   |
| <ul style="list-style-type: none"> <li>● Communication Interface: SPI bus</li> </ul>   | <ul style="list-style-type: none"> <li>● RoHS2.0, REACH &amp; Halogen-free compliant</li> </ul>   |
| <ul style="list-style-type: none"> <li>● Power Supply Voltage: 1.6V~5.5V</li> </ul>  |   |

### 3 Block Diagram

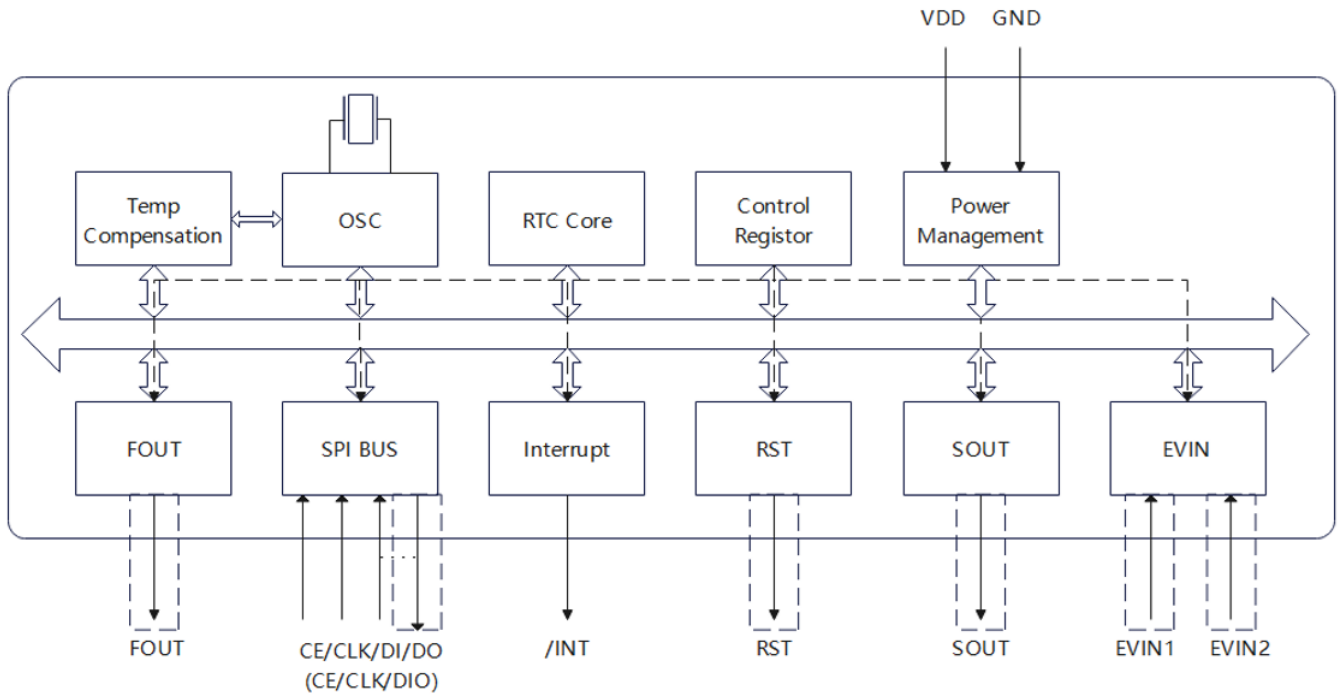


Figure1. Block Diagram

### 4 Pin definition

|          |  |          |  |
|----------|--|----------|--|
| Option A |  | Option B |  |
| Option C |  | Option D |  |

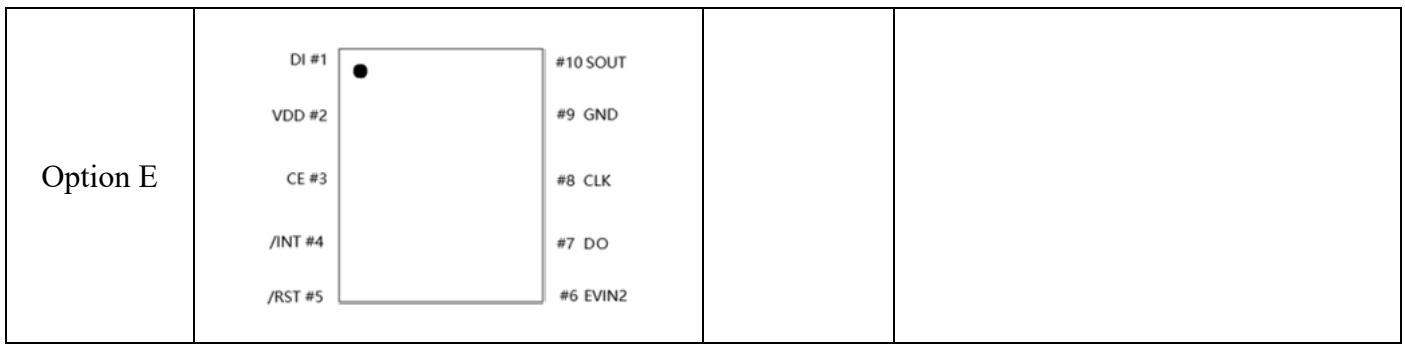


Table1. Pin Definition

| Pin Name | I/O | Initial State | Description  | INS5A4000 |   |   |   |   |
|----------|-----|---------------|--|-----------|---|---|---|---|
|          |     |               |  | A         | B | C | D | E |
| EVIN1    | I   | 1MΩ PU        | Time stamp trigger signal input pins, programmable PU and PD resistors and noise filters;  | √         | √ | - | - | - |
| EVIN2    | I   | 1MΩ PU        |  | √         | √ | - | √ | √ |
| CLK      | I   | Hi-Z          | 3-wires/4-wires SPI serial clock input pin; Not allow to keep floating;  | √         | √ | √ | √ | √ |
| DIO      | I/O | Hi-Z          | 3-wire SPI serial data input/output pin. Not allow to keep floating;   | √         | √ | √ | - | - |
| DO       | O   | Hi-Z          | 4-wire SPI serial data output pin;   | -         | - | - | √ | √ |
| DI       | I   | 1MΩ PU        | 4-wire SPI serial data input pin;  | -         | - | - | √ | √ |
| CE       | I   | 300KΩ PD      | 3-wire/4-wire SPI slave select input pin A pull-down resistor is included. Not allow to keep floating;   | √         | √ | √ | √ | √ |
| FOUT     | O   | Hi-Z          | Clock output pin (CMOS) 32.768 kHz, 1024 Hz or 1 Hz clock output is selectable. Can be switched to the wakeup timer interrupt output (CMOS).   | √         | √ | - | - | - |
| /INT     | O   | Hi-Z          | Interrupt output pin (Open drain). The wakeup timer, time update, alarm, and/or event detection interrupt signals can be selected to output from this pin.   | √         | √ | √ | √ | √ |
| /RST     | O   | Hi-Z          | Reset output pin (Open drain). A reset signal can be output to external devices when a VDD voltage drop below the predefined value is detected. When the VDD voltage is restored (a VDD voltage rise to the predefined value is detected), the reset output is cancelled (set to a Hi-Z state) after at least 60ms and less than 185ms from the detection. | -         | √ | - | - | √ |
| SOUT     | O   | Hi-Z          | Status output pin One of the internal flags (TF/AF/UF/EF/VTMPLF/VLF/'H'/'L') can be selected to output its status from this pin. The output signal polarity can also be selected.  | -         | - | - | √ | √ |
| VDD      | -   | -             | Main power supply pin;   | √         | √ | √ | √ | √ |
| GND      | -   | -             | Ground pin;  | √         | √ | √ | √ | √ |

Notes:

I: Input

O: Output

I/O: Input / output

PU: Pull Up

PD: Pull Down

✓ : This pin is available

-: This pin is unavailable

- Do not leave the unused input and input/output pins open nor apply an intermediate potential to them if the internal pull-up or -down resistor is not enabled.
- Leave the output pins (FOUT, SOUT, /INT, and DO) open when they are not used.
- When the reset output function is not use in the model with /RST pin function, the /RST pin should connect to a GND or keep floating.
- N.C. of PIN1 and PIN6 initial status is 1MΩ PU, do not connect to GND, otherwise is will add additional power consumption;
- N.C. PIN5 should keep floating or connect GND.
- N.C. PIN10 is Hi-Z output, it can connect to 'H', 'L' or keep floating.

## 5 Electrical Characteristics

### 5.1 Absolute Maximum Ratings

**Table2. Absolute Maximum Ratings**

| Parameter            | Symbol           | Value |      |      | Unit | Notes                           |
|----------------------|------------------|-------|------|------|------|---------------------------------|
|                      |                  | Min.  | Typ. | Max. |      |                                 |
| Power Supply Voltage | V <sub>DD</sub>  | -0.3  |      | 6.5  | V    |                                 |
| Input Voltage        | V <sub>IN</sub>  | 0.3   |      | 6.5  | V    | FOE, CE, DI, DIO, EVIN1, EVIN2  |
| Clock Output Voltage | V <sub>OUT</sub> | 0.3   |      | 6.5  | V    | /INT, /RST, FOUT, SOUT, DIO, DO |
| Storage temperature  | T <sub>STG</sub> | -55   |      | 125  | °C   |                                 |

### 5.2 Recommended Operating Conditions

**Table3. Recommended Operating Conditions**

| Parameter                        | Symbol            | Value |      |      | Unit | Notes  |
|----------------------------------|-------------------|-------|------|------|------|--|
|                                  |                   | Min.  | Typ. | Max. |      |  |
| Operating supply voltage         | V <sub>DD</sub>   | 1.6   | 3.0  | 5.5  | V    |  |
| Power on voltage                 | V <sub>UP</sub>   | 2     | 3.0  | 5.5  | V    | Power on voltage*  |
| Interface supply voltage         | V <sub>COM</sub>  | 1.6   | 3.0  | 5.5  | V    | SPI communication voltage                                    |
| Temperature compensation voltage | V <sub>TEMP</sub> | 1.8   | 3.0  | 5.5  | V    | VDD voltage that can keep temperature compensation operation |
| Operation temperature            | T <sub>OPR</sub>  | -40   | 25   | 125  | °C   |  |

\*Note:

1. During the power on and oscillation starting time, a voltage more than 2.0V must be provided to ensure the oscillation circuit to a stable state.
2. A bypass capacitor for noise suppression must be connected as close to the power supply pin as possible.
3. After the power supply is removed or power off, ensure that VDD=GND for more than 10 seconds before next power on cycle.

## 5.3 Power-On Characteristics

**Table4. Power-On Characteristics**

| Parameter                             | Symbol          | Value |      |      | Unit | Notes  |
|---------------------------------------|-----------------|-------|------|------|------|--|
|                                       |                 | Min.  | Typ. | Max. |      |  |
| Power supply rise time 1              | T <sub>R1</sub> | 0.5   | -    | 100  | ms/V | Voltage slope while the VDD voltage is rising from GND to V <sub>UP</sub> .  |
| Power supply rise time 2              | T <sub>R2</sub> | 0.5   | -    | 100  | ms/V | Voltage slope while the VDD voltage is rising from VDET on /RST mode.  |
| Access waiting time after power on    | T <sub>CL</sub> | 300   | -    | -    | ms   | Time after VDD reaches V <sub>UP</sub> (Min.) until accessing can be started                                       |
| Access end hold time before power off | T <sub>CD</sub> | 0     | -    | -    | ms   | The waiting time until the VDD voltage starts dropping in the T <sub>F</sub> voltage slope after the end of access |
| Power supply fall time                | T <sub>F</sub>  | 0.5   |      | 100  | ms/V | Voltage slope while the VDD voltage is dropping  |

## 5.4 Frequency Characteristics

**Table5. Frequency Characteristics**

| Parameter              | Symbol           | Value |      |          | Unit  | Notes                        |
|------------------------|------------------|-------|------|----------|-------|------------------------------|
|                        |                  | Min.  | Typ. | Max.     |       |                              |
| Frequency stability    | $\Delta f/f$     |       |      | $\pm 5$  | ppm   | @ -40°C to +85°C, VDD=3V     |
|                        |                  |       |      | $\pm 8$  |       | @ 85°C to +105°C, VDD=3V     |
|                        |                  |       |      | $\pm 50$ |       | @ 105°C to +125°C, VDD=3V    |
| Frequency vs voltage   | f/V              | -1    |      | 1        | ppm/V | @25 °C, VDD = 1.8 V to 5.5 V |
| Oscillation start time | t <sub>STA</sub> |       |      | 1        | s     | @25°C, VDD=2V~5.5V           |
|                        |                  |       |      | 3        | s     | @-40°C to 125°C, VDD=2V~5.5V |
| Year Aging             | f <sub>a</sub>   | -5    |      | +5       | ppm   | @25°C, First year            |
| FOUT duty cycle        | t <sub>w/t</sub> | 40    | 50   | 60       | %     |                              |

Note: If there is no special indication, the test conditions are GND = 0V, VDD = 3V, T<sub>OPR</sub> = -40°C~+125°C

## 5.5 DC Characteristics

Table6. DC Characteristics

| Parameter                     | Symbol             | Value               |      |      | Unit | Notes  |
|-------------------------------|--------------------|---------------------|------|------|------|--|
|                               |                    | Min.                | Typ. | Max  |      |  |
| Average Current consumption1  | I <sub>DD1</sub>   | -                   | 0.48 | 2.2  | uA   | V <sub>DD</sub> =5.0V<br>T <sub>OPR</sub> =25°C<br>/ INT = Hi-Z, FOUT: Output OFF (Hi-Z)<br>Temperature compensation interval: 2.0 s No  |
| Average Current consumption2  | I <sub>DD2</sub>   | -                   | 0.43 | 2.0  |      | V <sub>DD</sub> =3.0V<br>T <sub>OPR</sub> =25°C<br>/RST pin, SCL, SDA = H, CE = L  |
| Average Current consumption3  | I <sub>DD3</sub>   | -                   | 3.7  | 8    | uA   | V <sub>DD</sub> =5.0V<br>T <sub>OPR</sub> =25°C<br>/INT = Hi-Z FOUT: 32 kHz output, CL = 0 pF<br>Temperature compensation interval: 2.0 s No   |
| Average Current consumption4  | I <sub>DD4</sub>   | -                   | 2    | 6    |      | V <sub>DD</sub> =3.0V<br>T <sub>OPR</sub> =25°C<br>/RST pin, SCL, SDA = H, CE = L  |
| Average Current consumption5  | I <sub>DD5</sub>   | -                   | 8.0  | 17   | uA   | V <sub>DD</sub> =5.0V<br>T <sub>OPR</sub> =25°C<br>/INT= Hi-Z FOUT: 32 kHz output, CL= 30 pF<br>Temperature compensation interval: 2.0 s No  |
| Average Current consumption6  | I <sub>DD6</sub>   | -                   | 5.0  | 12   |      | V <sub>DD</sub> =3.0V<br>T <sub>OPR</sub> =25°C<br>/RST pin, SCL, SDA = H, CE = L  |
| Average Current consumption7  | I <sub>DD7</sub>   | -                   | 0.45 | 2.15 | uA   | V <sub>DD</sub> =5.0V<br>T <sub>OPR</sub> =25°C<br>/INT = Hi-Z FOUT: Output OFF (Hi-Z)<br>Temperature compensation circuit: OFF No   |
| Average Current consumption8  | I <sub>DD8</sub>   | -                   | 0.4  | 1.95 |      | V <sub>DD</sub> =3.0V<br>T <sub>OPR</sub> =25°C<br>/RST pin, SCL, SDA = H, CE = L  |
| Average Current consumption9  | I <sub>DD9</sub>   | -                   | 28   | 80   | uA   | V <sub>DD</sub> =5.0V<br>T <sub>OPR</sub> =25°C<br>/INT = Hi-Z FOUT: Output OFF (Hi-Z) The<br>temperature compensation operation: peak<br>performance No /RST pin, SCL, SDA = H, CE                          |
| Average Current consumption10 | I <sub>DD10</sub>  | -                   | 25   | 60   |      | V <sub>DD</sub> =3.0V<br>T <sub>OPR</sub> =25°C<br>= L   |
| Average Current consumption11 | I <sub>DD11</sub>  | -                   | 1.5  | 3    | uA   | V <sub>DD</sub> =5.0V<br>T <sub>OPR</sub> =25°C<br>/INT = Hi-Z, FOUT: Output OFF (Hi-Z)<br>Temperature compensation interval: 2.0 s With<br>/RST pin, during output cancelled (Hi-Z) SCL,<br>SDA = H, CE = L |
| Average Current consumption12 | I <sub>DD12</sub>  | -                   | 0.45 | 2.8  |      | V <sub>DD</sub> =2.0V<br>T <sub>OPR</sub> =25°C<br>/INT = Hi-Z, FOUT: Output OFF (Hi-Z)<br>Temperature compensation interval: 2.0 s With<br>/RST pin, during output (Low) SCL, SDA = H,<br>CE = L            |
| Voltage Low Detection         | V <sub>LF</sub>    | 1                   | 1.2  | 1.4  | V    | V <sub>LF</sub> detection voltage. When V <sub>DD</sub> drop below V <sub>LF</sub> , device will reset.  |
| VDD Voltage Detection1        | V <sub>DET1</sub>  | 1.4                 | 1.6  | 1.8  | V    | Temperature compensation stop detection voltage  |
| VDD Voltage Detection2        | -V <sub>DET2</sub> | 2.1                 | 2.4  | 2.7  | V    | V <sub>DD</sub> drop detection voltage for /RST signal generation  |
|                               | +V <sub>DET2</sub> | 2.2                 | 2.5  | 2.8  | V    | V <sub>DD</sub> rise detection voltage for /RST signal release   |
| High-level input voltage      | V <sub>IH</sub>    | 0.8*V <sub>DD</sub> | -    | 5.5  | V    | CE, CLK, DIO, DI, EVINn  |



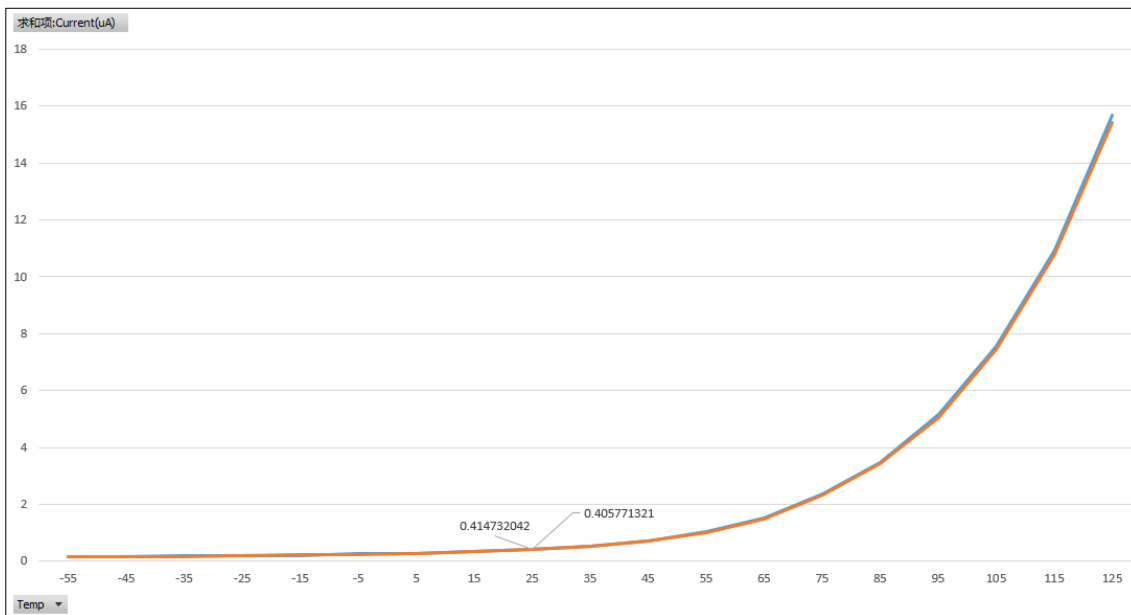
| Parameter                             | Symbol             | Value |      |                     | Unit | Notes   |                             |
|---------------------------------------|--------------------|-------|------|---------------------|------|---|-----------------------------|
|                                       |                    | Min.  | Typ. | Max                 |      |   |                             |
| Low-level input voltage               | V <sub>IL</sub>    | 0.3   | -    | 0.2*V <sub>DD</sub> | V    |   |                             |
| High-level output voltage             | V <sub>OH1</sub>   | 4.5   | -    | 5.5                 | V    | V <sub>DD</sub> =5.5V, I <sub>OH</sub> = -1mA   | FOUT, SOUT, DIO, DO         |
|                                       | V <sub>OH2</sub>   | 2.2   | -    | 3.0                 |      | V <sub>DD</sub> =3.0V, I <sub>OH</sub> = -1mA   |                             |
|                                       | V <sub>OH3</sub>   | 2.9   | -    | 3.0                 |      | V <sub>DD</sub> =3.0V, I <sub>OH</sub> = -100uA |                             |
| Low-level output voltage              | V <sub>OL1</sub>   | 0     | -    | 0.5                 | V    | V <sub>DD</sub> =5.5V, I <sub>OL</sub> = 1mA    | FOUT, SOUT                  |
|                                       | V <sub>OL2</sub>   | 0     | -    | 0.8                 |      | V <sub>DD</sub> =3.0V, I <sub>OL</sub> = 1mA    |                             |
|                                       | V <sub>OL3</sub>   | 0     | -    | 0.1                 |      | V <sub>DD</sub> =3.0V, I <sub>OL</sub> = 100uA  |                             |
|                                       | V <sub>OL4</sub>   | 0     | -    | 0.25                | V    | V <sub>DD</sub> =5.5V, I <sub>OL</sub> = 1mA    | /INT, /RST, DO, DIO         |
|                                       | V <sub>OL5</sub>   | 0     | -    | 0.4                 |      | V <sub>DD</sub> =3.5V, I <sub>OL</sub> = 1mA    |                             |
| Input leakage current                 | I <sub>LK1</sub>   | 2     | -    | 8                   | uA   | Input voltage = GND                             | EVINn                       |
|                                       | I <sub>LK2</sub>   | -0.5  | -    | 0.5                 |      | Input voltage = VDD                             |                             |
|                                       | I <sub>LK3</sub>   | -0.5  | -    | 0.5                 |      | Input voltage = GND                             | CE                          |
|                                       | I <sub>LK4</sub>   | 10    | -    | 20                  |      | Input voltage = VDD                             |                             |
|                                       | I <sub>LK5</sub>   | -0.5  | -    | 0.5                 |      | Input voltage = GND                             | DIO, CLK, DI                |
|                                       | I <sub>LK6</sub>   | -0.5  | -    | 0.5                 |      | Input voltage = VDD                             |                             |
| Output leakage current                | I <sub>OZ</sub>    | -0.5  | -    | 0.5                 | uA   | Input voltage = VDD or GND                      | /RST, /INT, FOUT, SOUT, DIO |
| Open drain output pin pull-up voltage | V <sub>PUP1</sub>  | -     | -    | 5.5                 | V    | /INT  |                             |
|                                       | V <sub>PUP2</sub>  | VDD   | -    | 5.5                 | V    | /RST  |                             |
| Pull-up resistance                    | R <sub>UP1</sub>   | 100   | 500  | 2000                | KΩ   | EVINn, VDD=3V, 500KΩ setting                    |                             |
|                                       | R <sub>UP2</sub>   | 200   | 1000 | 4000                | KΩ   | EVINn, VDD=3V, 1MΩ setting                      |                             |
|                                       | R <sub>UP3</sub>   | 200   | 1000 | 4000                | KΩ   | DI  |                             |
|                                       | R <sub>UP4</sub>   | 200   | 1000 | 4000                | MΩ   | Option C: N.C. pin1 / pin6                      |                             |
| Pull-down resistance                  | R <sub>DOWN1</sub> | 100   | 500  | 2000                | KΩ   | EVINn, VDD=3V, 500KΩ setting                    |                             |
|                                       | R <sub>DOWN2</sub> | 50    | 300  | 600                 | KΩ   | CE  |                             |

Note: If there is no special indication, the test conditions are GND=0V, VDD=3V, T<sub>OPR</sub>=-40°C~+125°C.

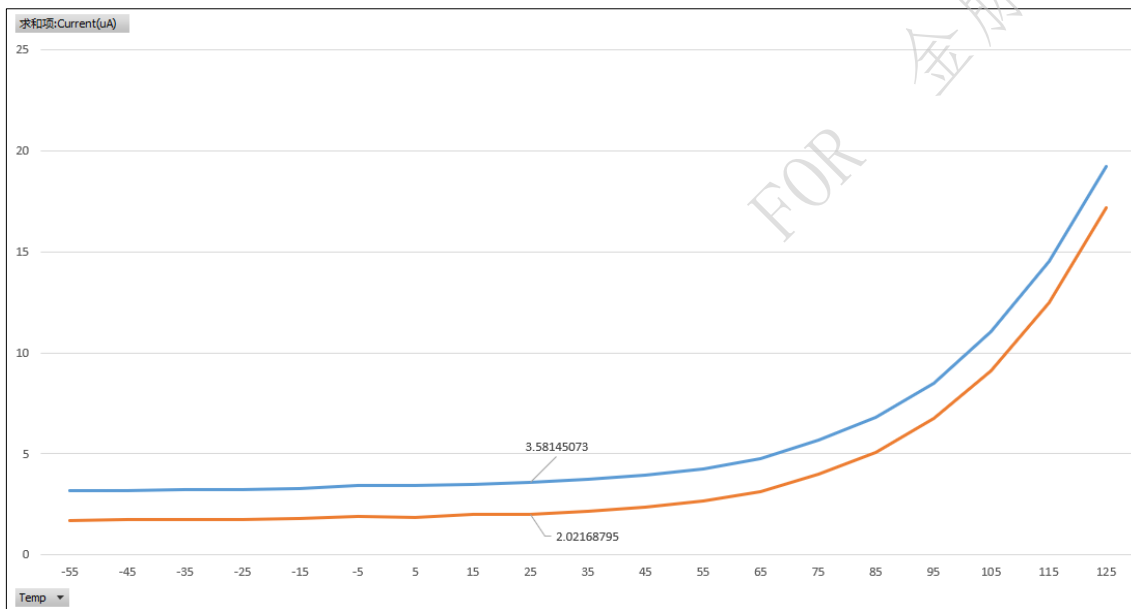


## 6 Reference Data

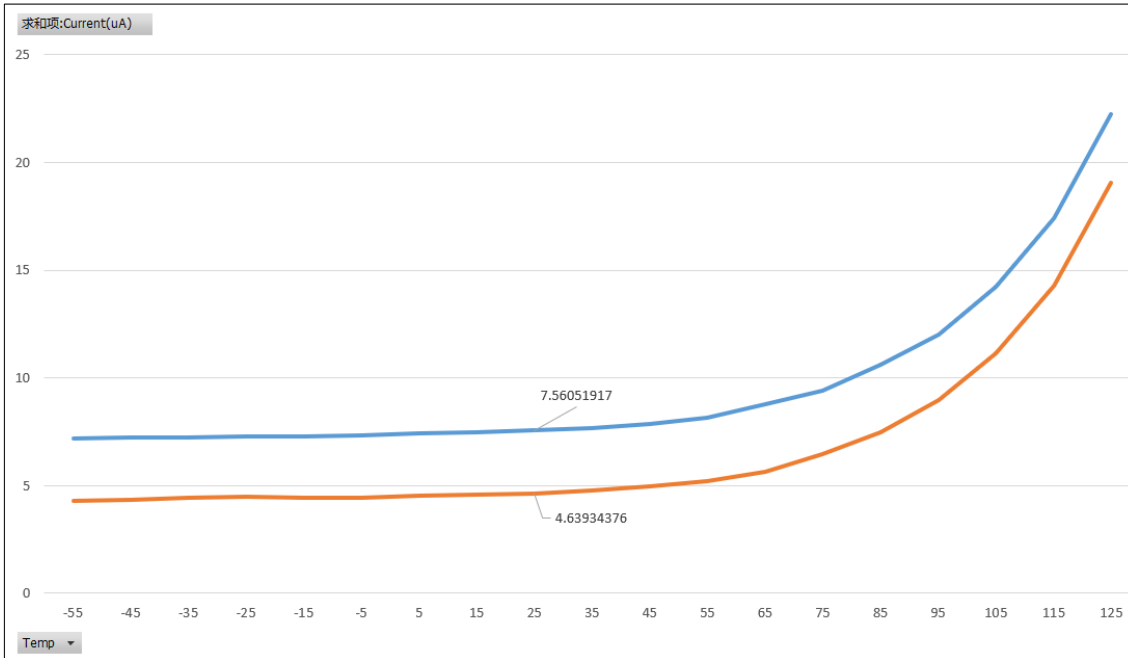
IDD1/2(uA) vs T<sub>OPR</sub>(°C) :



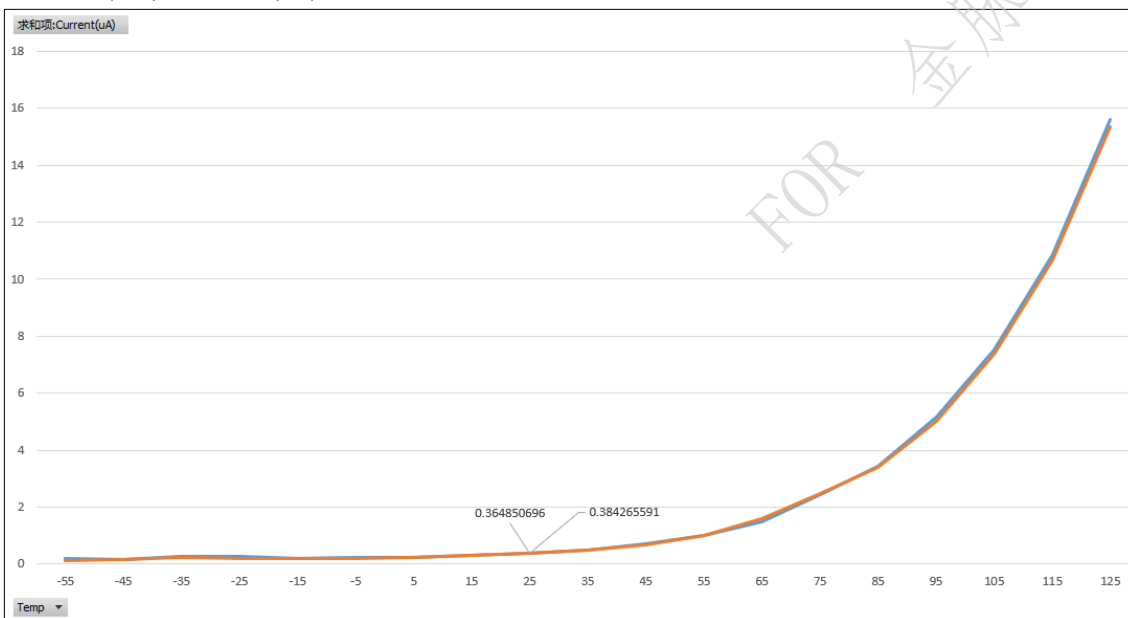
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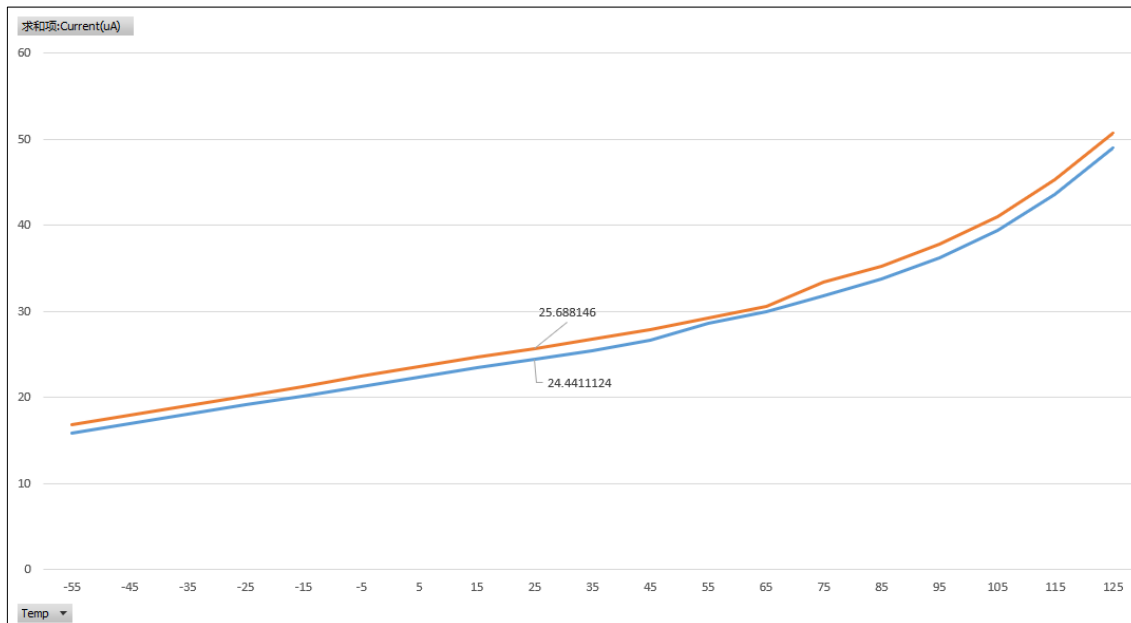
IDD5/6(uA) vs T<sub>OPR</sub>(°C) :



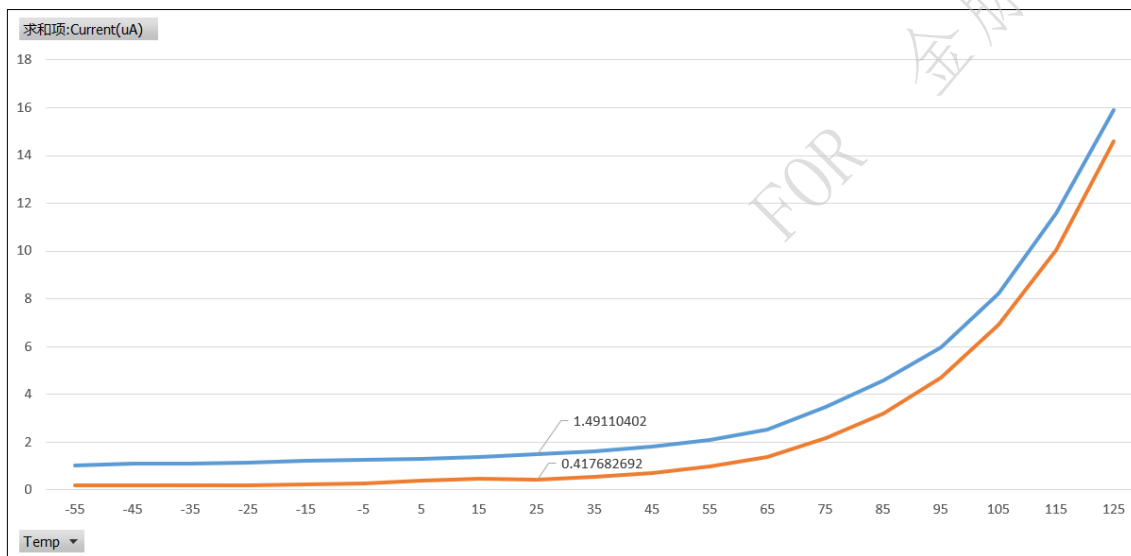
IDD7/8(uA) vs T<sub>OPR</sub>(°C) :



IDD9/10(uA) vs T<sub>OPR</sub>(°C) :



IDD11/12(uA) vs T<sub>OPR</sub>(°C) :



FOR 金脉

## 7 Registers

### 7.1 Register Lists

#### Symbol meaning

Bit name = ○: This bit is not writable, and the read value is always 0.

Bit name = x: This bit is not writable, and the read value is undefined.

Bit name = (GP): This is a general-purpose bit that allows writing 0 and 1 as well as reading the contents.

#### Notes:

- The address values indicate {bank number, address in bank}. (Example: 0x0F = Bank 0, Address 0xF)
- The registers must be accessed in eight-bit units.
- Be sure to avoid writing/reading data to/from an address not listed in the register tables.

| Address | Function             | bit7           | bit6       | bit5        | bit4    | bit3         | bit2 | bit1 | bit0        |
|---------|----------------------|----------------|------------|-------------|---------|--------------|------|------|-------------|
| 0x00    | SEC<br>BCD mode      | ○              | SEC_H[2:0] |             |         | SEC_L[3:0]   |      |      |             |
|         | SEC_BIN0<br>BIN mode | SEC_BIN[7:0]   |            |             |         |              |      |      |             |
| 0x01    | SEC<br>BCD mode      | ○              | MIN_H[2:0] |             |         | MIN_L[3:0]   |      |      |             |
|         | SEC_BIN1<br>BIN mode | SEC_BIN[15:8]  |            |             |         |              |      |      |             |
| 0x02    | HOUR<br>BCD mode     | ○              | ○          | HOUR_H[1:0] |         | HOUR_L[3:0]  |      |      |             |
|         | SEC_BIN2<br>BIN mode | SEC_BIN[23:16] |            |             |         |              |      |      |             |
| 0x03    | WEEK<br>BCD mode     | ○              | WEEK[6:0]  |             |         |              |      |      |             |
|         | SEC_BIN3<br>BIN mode | SEC_BIN[31:24] |            |             |         |              |      |      |             |
| 0x04    | DAY<br>BCD mode      | ○              | ○          | DAY_H[1:0]  |         | DAY_L[3:0]   |      |      |             |
|         | SEC_BIN4<br>BIN mode | ○              | ○          | ○           | ○       | ○            | ○    | ○    | SEC_BIN[32] |
| 0x05    | MONTH<br>BCD mode    | ○              | ○          | ○           | MONTH_H | MONTH_L[3:0] |      |      |             |
|         | NOT USED<br>BIN mode | ○              | ○          | ○           | ○       | ○            | ○    | ○    | ○           |
| 0x06    | YEAR                 | YEAR_H[3:0]    |            |             |         | YEAR_L[3:0]  |      |      |             |
|         | NOT USED<br>BIN mode | ○              | ○          | ○           | ○       | ○            | ○    | ○    | ○           |

|      |                                    |              |             |             |      |             |      |           |        |
|------|------------------------------------|--------------|-------------|-------------|------|-------------|------|-----------|--------|
| 0x07 | ALM_MIN                            | XMAE         | MALM_H[2:0] |             |      | MALM_L[3:0] |      |           |        |
|      | NOT USED<br>BIN mode               | (GP)         | (GP)        | (GP)        | (GP) | (GP)        | (GP) | (GP)      | (GP)   |
| 0x08 | ALM_HOUR                           | XHAE         | (GP)        | HALM_H[1:0] |      | HALM_L[3:0] |      |           |        |
|      | NOT USED<br>BIN mode               | (GP)         | (GP)        | (GP)        | (GP) | (GP)        | (GP) | (GP)      | (GP)   |
| 0x09 | ALM_WEEKDAY                        | XWAE         | WKALM[6:0]  |             |      |             |      |           |        |
|      |                                    |              | (GP)        | DALM_H[1:0] |      | DALM_L[3:0] |      |           |        |
|      | NOT USED<br>BIN mode               | (GP)         | (GP)        | (GP)        | (GP) | (GP)        | (GP) | (GP)      | (GP)   |
| 0x0A | WTCNT_L<br>Timer Counter<br>Low    | WTCNT[7:0]   |             |             |      |             |      |           |        |
| 0x0B | WTCNT_M<br>Timer Counter<br>Medium | WTCNT[15:8]  |             |             |      |             |      |           |        |
| 0x0C | WTCNT_H<br>Timer Counter<br>High   | WTCNT[23:16] |             |             |      |             |      |           |        |
| 0x0D | TCTL<br>Timer Control              | FSEL[1:0]    |             | USEL[0]     | TE   | WADA        | ○    | TSEL[1:0] |        |
| 0x0E | INTF<br>Status Flag                | PORF         | OSCSTPF     | UF          | TF   | AF          | EVF  | VLF       | VTMPLF |
| 0x0F | TSTP_INTE<br>Contrl Register       | CSEL[1:0]    |             | UIE         | TIE  | AIE         | EIE  | ○         | STOP   |

**BANK1**

| Address | Function                    | bit7          | bit6       | bit5        | bit4       | bit3        | bit2 | bit1 | bit0 |
|---------|-----------------------------|---------------|------------|-------------|------------|-------------|------|------|------|
| 0x10    | SUBSEC_L<br>Sub-Second Low  | SUBSEC[1:0]   |            | ○           | ○          | ○           | ○    | ○    | ○    |
| 0x11    | SUBSEC_H<br>Sub-Second High | SUBSEC[9:2]   |            |             |            |             |      |      |      |
| 0x12    | SEC_MIR(0x00)<br>BCD mode   | ○             | SEC_H[2:0] |             | SEC_L[3:0] |             |      |      |      |
|         | SEC_BIN0<br>BIN mode        | SEC_BIN[7:0]  |            |             |            |             |      |      |      |
| 0x13    | MIN_MIR(0x01)<br>BCD mode   | ○             | MIN_H[2:0] |             | MIN_L[3:0] |             |      |      |      |
|         | SEC_BIN1<br>BIN mode        | SEC_BIN[15:8] |            |             |            |             |      |      |      |
| 0x14    | HOUR_MIR(0x02)<br>BCD mode  | ○             | ○          | HOUR_H[1:0] |            | HOUR_L[3:0] |      |      |      |

|      |                                 |                    |           |            |                 |              |            |              |              |
|------|---------------------------------|--------------------|-----------|------------|-----------------|--------------|------------|--------------|--------------|
|      | SEC_BIN2<br>BIN mode            | SEC_BIN[23:16]     |           |            |                 |              |            |              |              |
| 0x15 | WEEK_MIR(0x03)<br>BCD mode      | ○                  | WEEK[6:0] |            |                 |              |            |              |              |
|      | SEC_BIN3<br>BIN mode            | SEC_BIN[31:24]     |           |            |                 |              |            |              |              |
| 0x16 | DAY_MIR(0x04)<br>BCD mode       | ○                  | ○         | DAY_H[1:0] |                 | DAY_L[3:0]   |            |              |              |
|      | SEC_BIN4<br>BIN mode            | ○                  | ○         | ○          | ○               | ○            | ○          | ○            | SEC_BIN[32]  |
| 0x17 | MONTH_MIR(0x05)<br>BCD mode     | ○                  | ○         | ○          | MONTH_H         | MONTH_L[3:0] |            |              |              |
|      | NOT USED<br>BIN mode            | ○                  | ○         | ○          | ○               | ○            | ○          | ○            | ○            |
| 0x18 | YEAR_MIR(0x06)<br>BCD mode      | YEAR_H[3:0]        |           |            |                 | YEAR_L[3:0]  |            |              |              |
|      | NOT USED<br>BIN mode            | ○                  | ○         | ○          | ○               | ○            | ○          | ○            | ○            |
| 0x19 | OFS_SUBSEC_H                    | OFS_<br>SUBSEC[10] | (GP)      | (GP)       | OFS_SUBSEC[9:5] |              |            |              |              |
| 0x1A | OFS_SUBSEC_L                    | OFS_SUBSEC[4:0]    |           |            |                 | ○            | OFSIN      | OFSEN        |              |
| 0x1B | DIG_TRIM_H                      | DTRIM[8:1]         |           |            |                 |              |            |              |              |
| 0x1C | DIG_TRIM_L                      | DTRIM[0]           | ○         | ○          | ○               | ○            | ○          | ○            | DTRIMEN      |
| 0x1D | TCTL_MIR(0x0D)<br>Timer Control | FSEL[1:0]          |           | USEL0      | TE              | WADA         | ○          | TSEL[1:0]    |              |
| 0x1E | INTF_MIR(0x0E)<br>Status Flag   | PORF               | OSCSTPF   | UF         | TF              | AF           | EVF        | VLF          | VTMPLF       |
| 0x1F | CNTSEL<br>Counter Select        | ○                  | ○         | ○          | ○               | ○            | ACC<br>BCD | BINCNT<br>EN | BCDCNT<br>EN |

**BANK2**

| Address | Function                         | bit7 | bit6 | bit5     | bit4          | bit3          | bit2 | bit1        | bit0        |
|---------|----------------------------------|------|------|----------|---------------|---------------|------|-------------|-------------|
| 0x20    | EVIN_EN<br>Event Input Enable    | ○    | ○    | ○        | EVIN2<br>CPEN | EVIN1<br>CPEN | ○    | EVIN2<br>EN | EVIN1<br>EN |
| 0x21    | EVIN1_CFG<br>EVIN1_Configuration | ○    | ○    | ○        | PUPD[2:0]     |               |      | POL[1:0]    |             |
| 0x22    | EVIN1_FLT<br>EVIN1 Noise Filter  | ○    | ○    | FLT[5:0] |               |               |      |             |             |
| 0x23    | EVIN2_CFG<br>EVIN2_Configuration | ○    | ○    | ○        | PUPD[2:0]     |               |      | POL[1:0]    |             |
| 0x24    | EVIN2_FLT<br>EVIN2 Noise Filter  | ○    | ○    | FLT[5:0] |               |               |      |             |             |



|      |                                   |        |             |   |   |   |             |             |            |
|------|-----------------------------------|--------|-------------|---|---|---|-------------|-------------|------------|
| 0x27 | BUF1_CFG1<br>BUF1 Configuration 1 | BINSEL | OVWEN       | ○ | ○ | ○ | FULL<br>IEN | EMPT<br>IEN | OVW<br>IEN |
| 0x28 | BUF1_STAT<br>BUF1 Status          | FULLF  | EMPTF       | ○ | ○ | ○ | ○           | ○           | OVWF       |
| 0x29 | BUF1_CFG2<br>BUF1 Configuration 2 | ○      | SRAM<br>MOD | ○ | ○ | ○ | ○           | ○           | ○          |

**BANK3**

| Address | Function  | bit7            | bit6          | bit5              | bit4         | bit3          | bit2   | bit1          | bit0    |
|---------|---|-----------------|---------------|-------------------|--------------|---------------|--------|---------------|---------|
| 0x30    | ALM_SEC<br>Second Alarm                           | XSAE            | SALM_H[2:0]   |                   | SALM_L[3:0]  |               |        |               |         |
| 0x31    | ALM_MIN_MIR(07)<br>Mirrored Minute Alarm          | XMAE            | MALM_H[2:0]   |                   | MALM_L[3:0]  |               |        |               |         |
| 0x32    | ALM_HOUR_MIR(08)<br>Mirrored Minute Alarm         | XHAE            | (GP)          | HALM_H<br>[1:0]   | HALM_L[3:0]  |               |        |               |         |
| 0x33    | ALM_WEEKDAY_MIR(09)<br>Mirrored Day-of-Week Alarm | XWAE            | WKALM[6:0]    |                   |              |               |        |               |         |
|         |   |                 | (GP)          | DALM_H<br>[1:0]   | DALM_L[3:0]  |               |        |               |         |
| 0x34    | UPDISEL<br>Time Update Interrupt Select           | ○               | ○             | ○                 | ○            | ○             | ○      | USEL[1]       | ○       |
| 0x38    | WTICFG<br>Wakeup Timer Interrupt<br>Configuration | PIN<br>MUX[1:0] |               | RST<br>OPT[1:0]   | WT<br>ONETIM | TSEL2         | WTIOUT | UPDOWN<br>MOD |         |
| 0x39    | WTCTL<br>Wakeup Timer Control                     | WT<br>RST       | EXWT<br>RSTEN | WT<br>RSTWIN[1:0] | WT<br>MODSEL | WT<br>STOPCTL | ○      | WT<br>STOP    |         |
| 0x3A    | WTCNT_L_MIR(0A)<br>Timer Counter Low              | WTCNT[7:0]      |               |                   |              |               |        |               |         |
| 0x3B    | WTCNT_M_MIR(0B)<br>Timer Counter Medium           | WTCNT[15:8]     |               |                   |              |               |        |               |         |
| 0x3C    | WTCNT_H_MIR(0C)<br>Timer Counter High             | WTCNT[23:16]    |               |                   |              |               |        |               |         |
| 0x3D    | TCTL_MIR(0D)<br>Timer Control                     | FSEL[1:0]       |               | USEL0             | TE           | WADA          | ○      | TSEL[1:0]     |         |
| 0x3E    | INTF_MIR(0E)<br>Status Flag                       | PORF            | OSCSTPF       | UF                | TF           | AF            | EVF    | VLF           | VTMP LF |
| 0x3F    | TSTP_INTE_MIR(0F)<br>Contrl Register              | CSEL[1:0]       |               | UIE               | TIE          | AIE           | EIE    | ○             | STOP    |

**BANK4**

| Address | Function | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------|----------|------|------|------|------|------|------|------|------|
|---------|----------|------|------|------|------|------|------|------|------|

|      |  |                        |              |              |                |                      |                        |     |                    |
|------|--|------------------------|--------------|--------------|----------------|----------------------|------------------------|-----|--------------------|
| 0x41 | WRCMD_CFG<br>Write Command Configuration | EVCNT<br>CLREN         | ○            | ○            | BUFIF<br>CLREN | ○                    | ○                      | ○   | CMDTRG<br>EN       |
| 0x42 | WRCMD_TRG<br>Write Command Trigger       | WRTRG[7:0]             |              |              |                |                      |                        |     |                    |
| 0x43 | EVNT_INTE<br>Event interrupt Enable      | ○                      | EVIN2I<br>EN | EVIN1I<br>EN | RSTOIE<br>N    | ○                    | VTMPLI<br>EN           | ○   | OSCSTP<br>I<br>EN  |
| 0x44 | CAP_EN<br>Capture Enable                 | ○                      | ○            | ○            | RSTO<br>CPEN   | ○                    | VTMPL<br>CPEN          | ○   | OSCSTP<br>C<br>PEN |
| 0x45 | INTF_MIR(OE)<br>Status Flag              | PORF                   | OSCST<br>PF  | UF           | TF             | AF                   | EVF                    | VLF | VTMPLF             |
| 0x46 | BUF_INTF<br>Buffer Interrupt Factor      | ○                      | ○            | BUFIF        | RSTOF          | ○                    | ○                      | ○   | ○                  |
| 0x47 | EVNT_INTE<br>Event interrupt Factor      | ○                      | EVIN2F       | EVIN1F       | RSTOEV<br>F    | ○                    | VTMPLE<br>VF           | ○   | OSCSTP<br>E<br>VF  |
| 0x4B | CL_CONTROL_OF<br>FSET                    | CL_CONTROL_OFFSET[7:0] |              |              |                |                      |                        |     |                    |
| 0x4C | TEMP_CL_FLT                              | ○                      | ○            | ○            | ○              | CL_ALFA_CFG[1:<br>0] | TEMP_ALFA_CFG[1:0<br>] |     |                    |
| 0x4D | SOFT_RST1                                | SOFT_RST1[7:0]         |              |              |                |                      |                        |     |                    |
| 0x4E | SOFT_RST2                                | SOFT_RST2[7:0]         |              |              |                |                      |                        |     |                    |

**BANK5**

| Address | Function                           | bit7 | bit6     | bit5       | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------|------------------------------------|------|----------|------------|------|------|------|------|------|
| 0x51    | EVIN1_EVCNT<br>EVIN1 Event Counter | ○    | ○        | EVCNT[5:0] |      |      |      |      |      |
| 0x52    | EVIN2_EVCNT<br>EVIN2 Event Counter | ○    | ○        | EVCNT[5:0] |      |      |      |      |      |
| 0x54    | EVINMON<br>EVIN Monitor            | ○    | EVIN2MON | EVIN1MON   | ○    | ○    | ○    | ○    | ○    |

|      |                         |     |    |   |   |        |           |
|------|-------------------------|-----|----|---|---|--------|-----------|
| 0x55 | SOUTCTL<br>SOUT Control | DCE | DC | ○ | ○ | SIGINV | SOUT[2:0] |
|------|-------------------------|-----|----|---|---|--------|-----------|

**BANK6/7(when reading time stamp(BCD) data in direct mode)**

Setting when time stamp data is captured: BUF1\_CFG1.BINSEL bit=0, CNTSEL.BCDCNTTE bit=1

| Address      | Function   | bit7          | bit6         | bit5         | bit4         | bit3         | bit2          | bit1 | bit0           |  |
|--------------|--|---------------|--------------|--------------|--------------|--------------|---------------|------|----------------|--|
| 0x60<br>0x70 | TIMESTAMP_SUBSEC_L<br>SUBSEC Time Stamp Data<br>Low  | SUBSEC[1:0]   |              | X            | X            | X            | X             | X    | X              |  |
| 0x61<br>0x71 | TIMESTAMP_SUBSEC_H<br>SUBSEC Time Stamp Data<br>High | SUBSEC[9:2]   |              |              |              |              |               |      |                |  |
| 0x62<br>0x72 | TIMESTAMP_SEC<br>SEC Time Stamp Data                 | X             | SEC_H[2:0]   |              |              | SEC_L[3:0]   |               |      |                |  |
| 0x63<br>0x73 | TIMESTAMP_MIN<br>MIN Time Stamp Data                 | X             | MIN_H[2:0]   |              |              | MIN_L[3:0]   |               |      |                |  |
| 0x64<br>0x74 | TIMESTAMP_HOUR<br>HOUR Time Stamp Data               | X             | X            | HOUR_H[2:0]  |              | HOUR_L[3:0]  |               |      |                |  |
| 0x65<br>0x75 | TIMESTAMP_DAY<br>DAY Time Stamp Data                 | X             | X            | DAY_H[2:0]   |              | DAY_L[3:0]   |               |      |                |  |
| 0x66<br>0x76 | TIMESTAMP_MONTH<br>MONTH Time Stamp Data             | X             | X            | X            | MONTH_H      | MONTH_L[3:0] |               |      |                |  |
| 0x67<br>0x77 | TIMESTAMP_YEAR<br>YEAR Time Stamp Data               | YEAR_H[3:0]   |              |              |              | YEAR_L[3:0]  |               |      |                |  |
| 0x68<br>0x78 | TIMESTAMP_EVSTAT<br>Event Status Time Stamp Data     | X             | EVIN2<br>POL | EVIN1<br>POL | X            | RSTO<br>STAT | VTMPL<br>STAT | X    | OSCSTP<br>STAT |  |
| 0x69<br>0x79 | TIMESTAMP_TRG<br>Time Stamp Trigger Factor           | OVWF<br>STAT* | EVIN2<br>TRG | EVIN1<br>TRG | WRCMD<br>TRG | RSTO<br>TRG  | VTMPL<br>TRG  | X    | OSCSTP<br>TRG  |  |

\* OVWFSTAT exists only in Address 0x79 (not exist in Address 0x69).

**BANK6/7(when reading time stamp(BIN) data in direct mode)**

Setting when time stamp data is captured: BUF1\_CFG1.BINSEL bit=1, CNTSEL.BINCNTTE bit=1

| Address      | Function   | bit7        | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|--------------|--|-------------|------|------|------|------|------|------|------|
| 0x60<br>0x70 | TIMESTAMP_SUBSEC_L<br>SUBSEC Time Stamp Data<br>Low  | SUBSEC[1:0] |      | X    | X    | X    | X    | X    | X    |
| 0x61<br>0x71 | TIMESTAMP_SUBSEC_H<br>SUBSEC Time Stamp Data<br>High | SUBSEC[9:2] |      |      |      |      |      |      |      |

|              |  |                |              |              |              |              |               |   |                |
|--------------|--|----------------|--------------|--------------|--------------|--------------|---------------|---|----------------|
| 0x62<br>0x72 | TIMESTAMP_SEC<br>SEC Time Stamp Data             | SUB_BIN[7:0]   |              |              |              |              |               |   |                |
| 0x63<br>0x73 | TIMESTAMP_MIN<br>MIN Time Stamp Data             | SUB_BIN[15:8]  |              |              |              |              |               |   |                |
| 0x64<br>0x74 | TIMESTAMP_HOUR<br>HOUR Time Stamp Data           | SUB_BIN[23:16] |              |              |              |              |               |   |                |
| 0x65<br>0x75 | TIMESTAMP_DAY<br>DAY Time Stamp Data             | SUB_BIN[31:24] |              |              |              |              |               |   |                |
| 0x66<br>0x76 | TIMESTAMP_MONTH<br>MONTH Time Stamp Data         | X              | X            | X            | X            | X            | X             | X | SUB_BIN[32]    |
| 0x67<br>0x77 | TIMESTAMP_YEAR<br>YEAR Time Stamp Data           | X              | X            | X            | X            | X            | X             | X | X              |
| 0x68<br>0x78 | TIMESTAMP_EVSTAT<br>Event Status Time Stamp Data | X              | EVIN2<br>POL | EVIN1<br>POL | X            | RSTO<br>STAT | VTMPL<br>STAT | X | OSCSTP<br>STAT |
| 0x69<br>0x79 | TIMESTAMP_TRG<br>Time Stamp Trigger Factor       | OVWF<br>STAT*  | EVIN2<br>TRG | EVIN1<br>TRG | WRCMD<br>TRG | RSTO<br>TRG  | VTMPL<br>TRG  | X | OSCSTP<br>TRG  |

\* OVWFSTAT exists only in Address 0x79 (not exist in Address 0x69).

### BANK6(SRAM mode)

Setting when accessing to the SRAM: BUF1\_CFG2.SRAMMOD bit=1

| Address | Function          | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------|-------------------|------|------|------|------|------|------|------|------|
| 0x60    | SRAM Address 0x00 | bit7 | bit6 | bit6 | bit4 | bit3 | bit2 | bit1 | bit0 |
| 0x61    | SRAM Address 0x01 |      |      |      |      |      |      |      |      |
| 0x62    | SRAM Address 0x02 |      |      |      |      |      |      |      |      |
| 0x63    | SRAM Address 0x03 |      |      |      |      |      |      |      |      |
| 0x64    | SRAM Address 0x04 |      |      |      |      |      |      |      |      |
| 0x65    | SRAM Address 0x05 |      |      |      |      |      |      |      |      |
| 0x66    | SRAM Address 0x06 |      |      |      |      |      |      |      |      |
| 0x67    | SRAM Address 0x07 |      |      |      |      |      |      |      |      |
| 0x68    | SRAM Address 0x08 |      |      |      |      |      |      |      |      |
| 0x69    | SRAM Address 0x09 |      |      |      |      |      |      |      |      |
| 0x6A    | SRAM Address 0x0A |      |      |      |      |      |      |      |      |
| 0x6B    | SRAM Address 0x0B |      |      |      |      |      |      |      |      |
| 0x6C    | SRAM Address 0x0C |      |      |      |      |      |      |      |      |
| 0x6D    | SRAM Address 0x0D |      |      |      |      |      |      |      |      |
| 0x6E    | SRAM Address 0x0E |      |      |      |      |      |      |      |      |
| 0x6F    | SRAM Address 0x0F |      |      |      |      |      |      |      |      |
| 0x70    | SRAM Address 0x10 | bit7 | bit6 | bit6 | bit4 | bit3 | bit2 | bit1 | bit0 |
| 0x71    | SRAM Address 0x11 |      |      |      |      |      |      |      |      |
| 0x72    | SRAM Address 0x12 |      |      |      |      |      |      |      |      |
| 0x73    | SRAM Address 0x13 |      |      |      |      |      |      |      |      |

|      |                   |  |  |  |  |  |  |  |
|------|-------------------|--|--|--|--|--|--|--|
| 0x74 | SRAM Address 0x14 |  |  |  |  |  |  |  |
| 0x75 | SRAM Address 0x15 |  |  |  |  |  |  |  |
| 0x76 | SRAM Address 0x16 |  |  |  |  |  |  |  |
| 0x77 | SRAM Address 0x17 |  |  |  |  |  |  |  |
| 0x78 | SRAM Address 0x18 |  |  |  |  |  |  |  |
| 0x79 | SRAM Address 0x19 |  |  |  |  |  |  |  |
| 0x7A | SRAM Address 0x1A |  |  |  |  |  |  |  |
| 0x7B | SRAM Address 0x1B |  |  |  |  |  |  |  |
| 0x7C | SRAM Address 0x1C |  |  |  |  |  |  |  |
| 0x7D | SRAM Address 0x1D |  |  |  |  |  |  |  |
| 0x7E | SRAM Address 0x1E |  |  |  |  |  |  |  |
| 0x7F | SRAM Address 0x1F |  |  |  |  |  |  |  |

## 7.2 Details of Registers

[BCD mode] indicates that the register can only be used in BCD mode (CNTSEL.ACCBCD bit = 1, CNTSEL.BCDCNTEN bit = 1).

[BIN mode] indicates that the register can only be used in BIN mode (NTSEL.ACCBCD bit = 0, CNTSEL.BINCNTEN bit = 0).

### 0x00:SEC(Second Data) [BCD mode]

| Bit No.       | bit7 | bit6       | bit5 | bit4 | bit3       | bit2 | bit1 | bit0 |
|---------------|------|------------|------|------|------------|------|------|------|
| Bit Name      | ○    | SEC_H[2:0] |      |      | SEC_L[3:0] |      |      |      |
| Initial value | 0    | 0          | 0    | 0    | 0          | 0    | 0    | 0    |
| R/W           | R    | R/W        | R/W  | R/W  | R/W        | R/W  | R/W  | R/W  |

SEC Valid value: 0x00~0x09, 0x10~0x19, 0x20~0x29, 0x30~0x39, 0x40~0x49, 0x50~0x59;

Bits 6–4: SEC\_H[2:0]

Bits 3–0: SEC\_L[3:0]

The second counter value can be set or read through these bits.

The SEC\_H[2:0] bits are the BCD code (0–5) of the 10-second digit and the SEC\_L[3:0] bits are the BCD code (0–9) of the 1-second digit. Writing second data to this address resets the 1/1024-second counter and clears Registers SUBSEC\_L and SUBSEC\_H to 0.

### 0x01:MIN(Minute Data) [BCD mode]

| Bit No.       | bit7 | bit6       | bit5 | bit4 | bit3       | bit2 | bit1 | bit0 |
|---------------|------|------------|------|------|------------|------|------|------|
| Bit Name      | ○    | MIN_H[2:0] |      |      | MIN_L[3:0] |      |      |      |
| Initial value | 0    | 0          | 0    | 0    | 0          | 0    | 0    | 0    |
| R/W           | R    | R/W        | R/W  | R/W  | R/W        | R/W  | R/W  | R/W  |

MIN Valid value: 0x00~0x09, 0x10~0x19, 0x20~0x29, 0x30~0x39, 0x40~0x49, 0x50~0x59;

Bits 6–4: MIN\_H[2:0]

Bits 3–0: MIN\_L[3:0]

The minute counter value can be set or read through these bits.

The MIN\_H[2:0] bits are the BCD code (0–5) of the 10-minute digit and the MIN\_L[3:0] bits are the BCD code (0–9) of the 1-minute digit.

### 0x02: HOUR(Hour Data) [BCD mode]

| Bit No.       | bit7 | bit6 | bit5        | bit4 | bit3        | bit2 | bit1 | bit0 |
|---------------|------|------|-------------|------|-------------|------|------|------|
| Bit Name      | ○    | ○    | HOUR_H[1:0] |      | HOUR_L[3:0] |      |      |      |
| Initial value | 0    | 0    | 0           | 0    | 0           | 0    | 0    | 0    |
| R/W           | R    | R    | R/W         | R/W  | R/W         | R/W  | R/W  | R/W  |

HOUR Valid value: 0x00~0x09, 0x10~0x19, 0x20~0x23;

Bits 5–4: HOUR\_H[1:0]

Bits 3–0: HOUR\_L[3:0]

The hour counter value can be set or read through these bits.

The HOUR\_H[1:0] bits are the BCD code (0–2) of the 10-hour digit and the HOUR\_L[3:0] bits are the BCD code (0–9) of the 1-hour digit.

### 0x03: WEEKDAY(Day-of-Week Data) [BCD mode]

| Bit No.       | bit7 | bit6      | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------------|------|-----------|------|------|------|------|------|------|
| Bit Name      | ○    | WEEK[6:0] |      |      |      |      |      |      |
| Initial value | 0    | 1         | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W           | R    | R/W       | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |

WEEKDAY Valid value: 0x01, 0x02, 0x04, 0x08, 0x10, 0x20, 0x40;

Bits 6–0: WEEK[6:0]

The day-of-week counter value can be set or read through these bits.

Each WEEK[6:0] bit one-to-one corresponds to a day of the week as the setting example shown below. Therefore, only one bit corresponding to today must be set. The WEEK[6:0] bits are shifted one bit to the left at the same time the day counter is updated (bit 6 is shifted to bit 0).

Example of day of week setting

| WEEK6              | WEEK5            | WEEK4              | WEEK3               | WEEK2              | WEEK1            | WEEK0            |
|--------------------|------------------|--------------------|---------------------|--------------------|------------------|------------------|
| Staurday<br>(0x40) | Friday<br>(0x20) | Thursday<br>(0x10) | Wednesday<br>(0x08) | Thursday<br>(0x04) | Monday<br>(0x02) | Sunday<br>(0x01) |

**0x04: DAY(Day Data) [BCD mode]**

| Bit No.       | bit7 | bit6 | bit5       | bit4 | bit3       | bit2 | bit1 | bit0 |
|---------------|------|------|------------|------|------------|------|------|------|
| Bit Name      | ○    | ○    | DAY_H[1:0] |      | DAY_L[3:0] |      |      |      |
| Initial value | 0    | 0    | 0          | 0    | 0          | 0    | 0    | 1    |
| R/W           | R    | R    | R/W        | R/W  | R/W        | R/W  | R/W  | R/W  |

DAY Valid value:

| Year        | Month           | Valid value                                 |
|-------------|-----------------|---|
| Common Year | 1/3/5/7/8/10/12 | 0x00~0x09, 0x10~0x19, 0x20~0x29, 0x30, 0x31 |
|             | 4/6/8/11        | 0x00~0x09, 0x10~0x19, 0x20~0x29, 0x30       |
|             | 2               | 0x00~0x09, 0x10~0x19, 0x20~0x28             |
| Leap Year   | 2               | 0x00~0x09, 0x10~0x19, 0x20~0x29             |

Bits 5–4: DAY\_H[1:0]

Bits 3–0: DAY\_L[3:0]

The day counter value can be set or read through these bits.

The DAY\_H[1:0] bits are the BCD code (0–3) of the 10-day digit and the DAY\_L[3:0] bits are the BCD code (0–9) of the 1-day digit.

**0x05: MONTH(Month Data) [BCD mode]**

| Bit No.       | bit7 | bit6 | bit5 | bit4    | bit3         | bit2 | bit1 | bit0 |
|---------------|------|------|------|---------|--------------|------|------|------|
| Bit Name      | ○    | ○    | ○    | MONTH_H | MONTH_L[3:0] |      |      |      |
| Initial value | 0    | 0    | 0    | 0       | 0            | 0    | 0    | 1    |
| R/W           | R    | R    | R    | R/W     | R/W          | R/W  | R/W  | R/W  |

MONTH Valid value: 0x00~0x09, 0x10~0x11;

Bit 4: MONTH\_H

Bits 3–0: MONTH\_L[3:0]

The month counter value can be set or read through these bits.

The MONTH\_H bits are the BCD code (0–1) of the 10-month digit and the MONTH\_L[3:0] bits are the BCD code (0–9) of the 1-month digit.

**0x06: YEAR(Year Data) [BCD mode]**

| Bit No.       | bit7        | bit6 | bit5 | bit4 | bit3        | bit2 | bit1 | bit0 |
|---------------|-------------|------|------|------|-------------|------|------|------|
| Bit Name      | YEAR_H[3:0] |      |      |      | YEAR_L[3:0] |      |      |      |
| Initial value | 0           | 0    | 0    | 0    | 0           | 0    | 0    | 0    |
| R/W           | R/W         | R/W  | R/W  | R/W  | R/W         | R/W  | R/W  | R/W  |

YEAR Valid: 0x00~0x09, 0x10~0x19, 0x20~0x29, 0x30~0x39, 0x40~0x49, 0x50~0x59, 0x60~0x69, 0x70~0x79, 0x80~0x89, 0x90~0x99;

Bits 7–4: YEAR\_H[3:0]

Bits 3–0: YEAR\_L[3:0]

The year counter value can be set or read through these bits.

The YEAR\_H[3:0] bits are the BCD code (0–9) of the 10-year digit and the YEAR\_L[3:0] bits are the BCD code (0–9) of the 1-year digit.

**0x07: ALM\_MINUTE(Minute Alarm) [BCD mode]**

| Bit No.       | bit7 | bit6        | bit5 | bit4 | bit3        | bit2 | bit1 | bit0 |
|---------------|------|-------------|------|------|-------------|------|------|------|
| Bit Name      | XMAE | MALM_H[2:0] |      |      | MALM_L[3:0] |      |      |      |
| Initial value | 1    | 0           | 0    | 0    | 0           | 0    | 0    | 0    |
| R/W           | R/W  | R/W         | R/W  | R/W  | R/W         | R/W  | R/W  | R/W  |

Bit 7: XMAE

This bit enables/disables the minute alarm setting.

1 (R/W): Minute alarm is disabled.

0 (R/W): Minute alarm is enabled.

When this bit is set to 1, the setting in this register is disabled and it does not affect alarm generation. When this bit is set to 0, the setting in this register is enabled and coincidence between the minute counter value and the setting value of the MALM\_H[2:0] and MALM\_L[3:0] bits is included in the alarm generation condition.

Bits 6–4: MALM\_H[2:0]

Bits 3–0: MALM\_L[3:0]

These bits set the minute alarm condition in a BCD code.

The MALM\_H[2:0] bits specify the 10-minute digit (0–5) and the MALM\_L[3:0] bits specify 1-minute digit (0–9).

**0x08: ALM\_HOUR(Hour Alarm) [BCD mode]**



| Bit No.       | bit7 | bit6 | bit5        | bit4 | bit3        | bit2 | bit1 | bit0 |
|---------------|------|------|-------------|------|-------------|------|------|------|
| Bit Name      | XHAE | (GP) | HALM_H[1:0] |      | HALM_L[3:0] |      |      |      |
| Initial value | 1    | 0    | 0           | 0    | 0           | 0    | 0    | 0    |
| R/W           | R/W  | R/W  | R/W         | R/W  | R/W         | R/W  | R/W  | R/W  |

Bit 7: XHAE

This bit enables/disables the hour alarm setting.

1 (R/W): Hour alarm is disabled.

0 (R/W): Hour alarm is enabled.

When this bit is set to 1, the setting in this register is disabled and it does not affect alarm generation. When this bit is set to 0, the setting in this register is enabled and coincidence between the hour counter value and the setting value of the HALM\_H[1:0] and HALM\_L[3:0] bits is included in the alarm generation condition.

Bits 5–4: HALM\_H[1:0]

Bits 3–0: HALM\_L[3:0]

These bits set the hour alarm condition in a BCD code.

The HALM\_H[1:0] bits specify the 10-hour digit (0–2) and the HALM\_L[3:0] bits specify 1-hour digit (0–9).

### 0x09: ALM\_WEEKDAY (Day-of-Week Alarm / Day Alarm) [BCD mode]

#### Day-of-Week Alarm

| Bit No.       | bit7 | bit6       | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------------|------|------------|------|------|------|------|------|------|
| Bit Name      | XWAE | WKALM[6:0] |      |      |      |      |      |      |
| Initial value | 1    | 0          | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W           | R/W  | R/W        | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |

#### Day Alarm

| Bit No.       | bit7 | bit6 | bit5        | bit4 | bit3        | bit2 | bit1 | bit0 |
|---------------|------|------|-------------|------|-------------|------|------|------|
| Bit Name      | XWAE | (GP) | DALM_H[1:0] |      | DALM_L[3:0] |      |      |      |
| Initial value | 1    | 0    | 0           | 0    | 0           | 0    | 0    | 0    |
| R/W           | R/W  | R/W  | R/W         | R/W  | R/W         | R/W  | R/W  | R/W  |

#### Note:

This register switches its function according to the TCTL.WADA bit setting.

TCTL.WADA bit = 0: Day-of-Week Alarm

TCTL.WADA bit = 1: Day Alarm

Bit 7: XWAE

This bit enables/disables the day-of-week or day alarm setting.

1 (R/W): Day-of-week/day alarm is disabled.

0 (R/W): Day-of-week/day alarm is enabled.

When this bit is set to 1, the setting in this register is disabled and it does not affect alarm generation. When this bit is set to 0, the setting in this register is enabled and an alarm will be generated if the following condition is met.

TCTL.WADA bit = 0: The same bit in the day-of-week counter as one that has been set within WKALM[6:0] is set.

TCTL.WADA bit = 1: The day counter value matches with the DALM\_H[1:0]/DALM\_L[3:0] bit setting value. Bits 6–0: WKALM[6:0] (Day-of-Week Alarm)

These bits set the day-of-week alarm condition.

More than one bit can be set to specify two or more days of the week.

Bits 5–4: DALM\_H[1:0] (Day Alarm)

Bits 3–0: DALM\_L[3:0] (Day Alarm)

These bits set the day alarm condition in a BCD code.

The DALM\_H[1:0] bits specify the 10-day digit (0–3) and the DALM\_L[3:0] bits specify 1-day digit (0–9).

**0x0A: WTCNT\_L (Wakeup Timer Counter Low)**

**0x0B: WTCNT\_M (Wakeup Timer Counter Middle)**

**0x0C: WTCNT\_H (Wakeup Timer Counter High)**

**Wakeup Timer Counter Low**

|               |            |      |      |      |      |      |      |      |
|---------------|------------|------|------|------|------|------|------|------|
| Bit No.       | bit7       | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| Bit Name      | WTCNT[7:0] |      |      |      |      |      |      |      |
| Initial value | 0          | 0    | 0    | 0    | 0    | 0    | 0    | 1    |
| R/W           | R/W        | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |

**Wakeup Timer Counter Middle**

|               |             |      |      |      |      |      |      |      |
|---------------|-------------|------|------|------|------|------|------|------|
| Bit No.       | bit7        | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| Bit Name      | WTCNT[15:8] |      |      |      |      |      |      |      |
| Initial value | 0           | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W           | R/W         | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |

**Wakeup Timer Counter High**

|               |              |      |      |      |      |      |      |      |
|---------------|--------------|------|------|------|------|------|------|------|
| Bit No.       | bit7         | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| Bit Name      | WTCNT[23:16] |      |      |      |      |      |      |      |
| Initial value | 0            | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

|     |     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|

Bits 7–0: WTCNT[7:0] (Wakeup Timer Counter Low)

WTCNT[15:8] (Wakeup Timer Counter Middle)

WTCNT[23:16] (Wakeup Timer Counter High)

**Notes:**

- Make sure the TCTL.TE bit = 0 (wakeup timer disabled) before setting a preset value.
- The preset data cannot be set to 0x000000. If 0x000000 is written to Registers WTCNT\_L, WTCNT\_M, and WTCNT\_H, the wakeup timer cannot perform counting up/down and an interrupt does not occur.

When reading

When the TCTL.TE bit = 1 (wakeup timer enabled), the current counter value is read out from these registers. This counter has a read buffer function, so the correct value can be obtained in any time by reading these three registers successively even if the wakeup timer is operating. When the TCTL.TE bit = 0 (wakeup timer disabled), the currently set preset value is read out.

**0x0D: TCTL (Timer Control)**

| Bit No.       | bit7      | bit6 | bit5  | bit4 | bit3 | bit2 | bit1      | bit0 |
|---------------|-----------|------|-------|------|------|------|-----------|------|
| Bit Name      | FSEL[1:0] |      | USEL0 | TE   | WADA | ○    | TSEL[1:0] |      |
| Initial value | 0         | 0    | 0     | 0    | 0    | 0    | 1         | 0    |
| R/W           | R/W       | R/W  | R/W   | R/W  | R/W  | R/W  | R/W       | R/W  |

Bits 7–6: FSEL[1:0]

These bits select an FOUT frequency.

FOUT Output Clock Selections

| TCTL.FSEL[1:0] | Output clock       |
|----------------|--------------------|
| 0b00           | 32.867kHz(default) |
| 0b01           | 1024Hz             |
| 0b10           | 1Hz                |
| 0b11           | Off                |

Bit 5: USEL0

This bit selects a time update interrupt event by using in conjunction with the UPDISEL.USEL1 bit.

Time Update Interrupt Event Selections

| UPDISEL.USEL1 | TCTL.USEL0 | Interrupt event                 |
|---------------|------------|---------------------------------|
| 0             | 0          | Second counter update (default) |

|   |   |                       |
|---|---|-----------------------|
| 0 | 1 | Minute counter update |
| 1 | 0 | Hour counter update   |
| 1 | 1 | No interrupt event    |

Bit 4: TE

This bit enables/disables wakeup timer interrupts.

1 (R/W): Wakeup timer interrupts are enabled.

0 (R/W): Wakeup timer interrupts are disabled.

Bit 3: WADA

This bit selects either day-of-week alarm or day alarm to be used as an alarm generation condition.

1 (R/W): Day alarm

0 (R/W): Day-of-week alarm

Bits 1–0: TSEL[1:0]

These bits select an internal clock used as the source clock of the wakeup timer.

Wakeup Timer Source Clock Selections

| WTICFG.TSEL2 | TCTL.TSEL[1:0] | Source clock                      |
|--------------|----------------|-----------------------------------|
| 0            | 0b00           | 1024Hz                            |
| 0            | 0b01           | 64Hz                              |
| 0            | 0b10           | 1Hz(default)                      |
| 0            | 0b11           | 1/60Hz                            |
| 1            | 0b'xx          | External clock input of EVIN2 pin |

This setting is effective when the WTICFG.TSEL2 bit = 0. When the WTICFG.TSEL2 bit = 1, the external clock input to the EVIN2 pin is used as the source clock.

**0x0E: INTF (Status Flag)**

| Bit No.       | bit7 | bit6    | bit5 | bit4 | bit3 | bit2 | bit1 | bit0   |
|---------------|------|---------|------|------|------|------|------|--------|
| Bit Name      | PORF | OSCSTPF | UF   | TF   | AF   | EVF  | VLF  | VTMPLF |
| Initial value | 1    | 1       | 0    | 0    | 0    | 0    | 1    | 1      |
| R/W           | R/W  | R/W     | R/W  | R/W  | R/W  | R/W  | R/W  | R/W    |

Bit 7: PORF

This is a self-monitoring flag that indicates whether a power-on-reset is executed after power is turned on or not.

1 (R): Power-on-reset has been detected.

0 (R): No power-on-reset has been detected.

1 (W): Ineffective

0 (W): Flag clear (effective only when power-on reset has been cancelled)

Bit 6: OSCSTPF

OSCSTPF This is a self-monitoring flag that indicates whether the oscillation of the crystal oscillator has stopped or not.

1 (R): Oscillation stop state has been detected.

0 (R): Oscillator stop state has not been detected.

1 (W): Ineffective

0 (W): Flag clear (effective only when an oscillation stop state has not been detected)

Bit 5: UF

Bit 4: TF

Bit 3: AF

Bit 2: EVF

They are interrupt flags that indicate occurrence of an RTC interrupt event.

1 (R): Interrupt event has occurred.

0 (R): No interrupt event has occurred.

1 (W): Ineffective

0 (W): Flag clear (except for EVF)

The following shows the correspondence between the bit and interrupt:

UF: Time update interrupt

TF: Wakeup timer interrupt

AF: Alarm interrupt

EVF: Time stamp event detection interrupt

Bit 1: VLF

This is a self-monitoring flag that indicates an abnormality.

1 (R): There is an abnormality. (PORF bit = 1 or OSCSTPF bit = 1)

0 (R): No abnormality

1 (W): Ineffective

0 (W): Flag clear (effective only when power-on reset has been cancelled and an oscillation stop state has not been detected)

Bit 0: VTMLPF

This is a self-monitoring flag that indicates the history of a VDD voltage drop to the temperature compensation update stop voltage or less ( $VDD \leq V_{TEMP}$ ).

1 (R): Voltage drop has been detected.

0 (R): Voltage drop has not been detected.

1 (W): Ineffective

0 (W): Flag clear (effective only when the VDD voltage is normal)

**0x0F: TSTP\_INTE (Timer Stop and Interrupt Enable)**

| Bit No.       | bit7      | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------------|-----------|------|------|------|------|------|------|------|
| Bit Name      | CSEL[1:0] |      | UIE  | TIE  | AIE  | EIE  | ○    | STOP |
| Initial value | 0         | 1    | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W           | R/W       | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |

Bits 7–6: CSEL[1:0]

These bits set the execution interval of the temperature sensor measurement operation.

Execution Interval of Temperature Sensor Measurement Operation

| TSTP_INTE.CSEL[1:0] | Execution interval   |
|---------------------|----------------------|
| 0b00                | 0.5 seconds          |
| 0b01                | 2.0 seconds(default) |
| 0b10                | 10.0 seconds         |
| 0b11                | 30.0 seconds         |

Bit 5: UIE

Bit 4: TIE

Bit 3: AIE

Bit 2: EIE

These bits enable the interrupts output to /INT pin.

1 (R/W): Interrupts output to /INT pin are enabled.

0 (R/W): Interrupts output to /INT pin are disabled.

Each bit corresponds to an interrupt as shown below.

UIE: Time update interrupt

TIE: Wakeup timer interrupt

AIE: Alarm interrupt

EIE: Time stamp event detection interrupt

**Bit 0: STOP**

This bit controls the timer counter operations.

1 (W): Stops operating of the counters.

0 (W): Starts operating of the counters.

1 (R): The timer is idle.

0 (R): The timer is operating.

The STOP bit stops the following operations:

1) Stop sub\_sec(1/1024), second, minute, day, day of week, month, and year counters, and binary second counter. Thus, a time update interrupt and an alarm interrupt do not occur. The time stamp function uses the time at the point the counters stop as the clock data.

2) Wakeup timer interrupt: The wakeup timer stops and does not generate an interrupt.

3) FOUT output: The FOUT output fixed at H or L when 1 Hz output is selected. When 32.768 kHz or 1024 Hz is selected, the output continues even if the STOP bit = 1.

**Note:**

If the timer is stopped by the STOP bit when reading clock/calendar data, time error is increased. Therefore, do not stop the counter using the STOP bit when reading the clock/calendar registers.

**0x10: SUBSEC\_L (Sub-Second Data Low)**

**0x11: SUBSEC\_H (Sub-Second Data High)**

**Sub-Second Data Low**

| Bit No.       | bit7        | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------------|-------------|------|------|------|------|------|------|------|
| Bit Name      | SUBSEC[1:0] |      | ○    | ○    | ○    | ○    | ○    | ○    |
| Initial value | 0           | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W           | R/W         | R/W  | R    | R    | R    | R    | R    | R    |

**Sub-Second Data High**

| Bit No.       | bit7        | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------------|-------------|------|------|------|------|------|------|------|
| Bit Name      | SUBSEC[9:2] |      |      |      |      |      |      |      |
| Initial value | 0           | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W           | R/W         | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |

SUB-SECOND Valid value: 0x00 0000 0000 ~ 0xFF FFFF FFFF;

Bits 7–6: SUBSEC[1:0] (Sub-Second Data Low)

Bits 7–0: SUBSEC[9:2] (Sub-Second Data High)

These bits are used to set and read the 1/1024-second counter, which is a 10-bit binary counter. The SUBSEC\_L.SUBSEC[1:0] bits are the low-order 2 bits of the 1/1024-second counter and the SUBSEC\_H.

SUBSEC[9:2] bits are the high-order 8 bits.

SUBSEC[9:0] bits

| Bit                        | SUBSEC9 | SUBSEC8 | SUBSEC7 | SUBSEC6 | SUBSEC5 | SUBSEC4 | SUBSEC3 | SUBSEC2 | SUBSEC1 | SUBSEC0 |
|----------------------------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| Count value (1024Hz) cycle | 512     | 256     | 128     | 64      | 32      | 16      | 8       | 4       | 2       | 1       |

Writing data to Register SEC (Address 0x00, BCD mode) resets the 1/1024-second counter, as a result, Registers SUBSEC\_L and SUBSEC\_H are cleared to 0. On the other hand, writing data to Register SEC\_MIR (Address 0x12), which is the mirror address of Register SEC, does not reset the 1/1024-second counter.

**0x12: SEC\_MIR (Mirrored Second Data, = 0x00) [BCD mode]**

| Bit No.       | bit7 | bit6       | bit5 | bit4 | bit3       | bit2 | bit1 | bit0 |
|---------------|------|------------|------|------|------------|------|------|------|
| Bit Name      | ○    | SEC_H[2:0] |      |      | SEC_L[3:0] |      |      |      |
| Initial value | 0    | 0          | 0    | 0    | 0          | 0    | 0    | 0    |
| R/W           | R    | R/W        | R/W  | R/W  | R/W        | R/W  | R/W  | R/W  |

This is a mirror register of Register SEC. For more information, refer to “0x00: SEC (Second Data).” However, writing to this address does not reset the 1/1024-second counter.

**0x13: MIN\_MIR (Mirrored Minute Data, = 0x0h) [BCD mode]**

| Bit No.       | bit7 | bit6       | bit5 | bit4 | bit3       | bit2 | bit1 | bit0 |
|---------------|------|------------|------|------|------------|------|------|------|
| Bit Name      | ○    | MIN_H[2:0] |      |      | MIN_L[3:0] |      |      |      |
| Initial value | 0    | 0          | 0    | 0    | 0          | 0    | 0    | 0    |
| R/W           | R    | R/W        | R/W  | R/W  | R/W        | R/W  | R/W  | R/W  |

This is a mirror register of Register MIN. For more information, refer to “0x01: MIN (Minute Data).”

**0x14: HOUR\_MIR (Mirrored Hour Data, = 0x02) [BCD mode]**

| Bit No.       | bit7 | bit6 | bit5        | bit4 | bit3        | bit2 | bit1 | bit0 |
|---------------|------|------|-------------|------|-------------|------|------|------|
| Bit Name      | ○    | ○    | HOUR_H[1:0] |      | HOUR_L[3:0] |      |      |      |
| Initial value | 0    | 0    | 0           | 0    | 0           | 0    | 0    | 0    |
| R/W           | R    | R    | R/W         | R/W  | R/W         | R/W  | R/W  | R/W  |

This is a mirror register of Register HOUR. For more information, refer to “0x02: HOUR (Hour Data).”

**0x15: WEEKDAY\_MIR (Mirrored Day-of-Week Data, = 0x03) [BCD mode]**

| Bit No. | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------|------|------|------|------|------|------|------|------|
|---------|------|------|------|------|------|------|------|------|



|               |   |           |     |     |     |     |     |     |
|---------------|---|-----------|-----|-----|-----|-----|-----|-----|
| Bit Name      | ○ | WEEK[6:0] |     |     |     |     |     |     |
| Initial value | 0 | 1         | 0   | 0   | 0   | 0   | 0   | 0   |
| R/W           | R | R         | R/W | R/W | R/W | R/W | R/W | R/W |

This is a mirror register of Register WEEKDAY. For more information, refer to “0x03: WEEKDAY (Day-of Week Data).”

**0x16: DAY\_MIR (Mirrored Day Data, = 0x04) [BCD mode]**

|               |      |      |            |      |            |      |      |      |
|---------------|------|------|------------|------|------------|------|------|------|
| Bit No.       | bit7 | bit6 | bit5       | bit4 | bit3       | bit2 | bit1 | bit0 |
| Bit Name      | ○    | ○    | DAY_H[1:0] |      | DAY_L[3:0] |      |      |      |
| Initial value | 0    | 0    | 0          | 0    | 0          | 0    | 0    | 1    |
| R/W           | R    | R    | R/W        | R/W  | R/W        | R/W  | R/W  | R/W  |

This is a mirror register of Register DAY. For more information, refer to “0x04: DAY (Day Data).”

**0x17: MONTH\_MIR (Mirrored Month Data, = 0x05) [BCD mode]**

|               |      |      |      |         |              |      |      |      |
|---------------|------|------|------|---------|--------------|------|------|------|
| Bit No.       | bit7 | bit6 | bit5 | bit4    | bit3         | bit2 | bit1 | bit0 |
| Bit Name      | ○    | ○    | ○    | MONTH_H | MONTH_L[3:0] |      |      |      |
| Initial value | 0    | 0    | 0    | 0       | 0            | 0    | 0    | 1    |
| R/W           | R    | R    | R    | R/W     | R/W          | R/W  | R/W  | R/W  |

This is a mirror register of Register MONTH. For more information, refer to “0x05: MONTH (Month Data).”

**0x18: YEAR\_MIR (Mirrored Year Data, = 0x06) [BCD mode]**

|               |             |      |      |      |             |      |      |      |
|---------------|-------------|------|------|------|-------------|------|------|------|
| Bit No.       | bit7        | bit6 | bit5 | bit4 | bit3        | bit2 | bit1 | bit0 |
| Bit Name      | YEAR_H[3:0] |      |      |      | YEAR_L[3:0] |      |      |      |
| Initial value | 0           | 0    | 0    | 0    | 0           | 0    | 0    | 0    |
| R/W           | R/W         | R/W  | R/W  | R/W  | R/W         | R/W  | R/W  | R/W  |

This is a mirror register of Register YEAR. For more information, refer to “0x06: YEAR (Year Data).”

**0x00 / 0x12: SEC\_BIN0 (Second Binary Data 0) [BIN mode]**
**0x01 / 0x13: SEC\_BIN1 (Second Binary Data 1) [BIN mode]**
**0x02 / 0x14: SEC\_BIN2 (Second Binary Data 2) [BIN mode]**
**0x03 / 0x15: SEC\_BIN3 (Second Binary Data 3) [BIN mode]**
**0x04 / 0x16: SEC\_BIN4 (Second Binary Data 4) [BIN mode]**
**Second Binary Data 0**

|         |      |      |      |      |      |      |      |      |
|---------|------|------|------|------|------|------|------|------|
| Bit No. | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------|------|------|------|------|------|------|------|------|

|               |              |     |     |     |     |     |     |     |
|---------------|--------------|-----|-----|-----|-----|-----|-----|-----|
| Bit Name      | SEC_BIN[7:0] |     |     |     |     |     |     |     |
| Initial value | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| R/W           | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Second Binary Data 1**

|               |               |      |      |      |      |      |      |      |
|---------------|---------------|------|------|------|------|------|------|------|
| Bit No.       | bit7          | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| Bit Name      | SEC_BIN[15:8] |      |      |      |      |      |      |      |
| Initial value | 0             | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W           | R/W           | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |

**Second Binary Data 2**

|               |                |      |      |      |      |      |      |      |
|---------------|----------------|------|------|------|------|------|------|------|
| Bit No.       | bit7           | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| Bit Name      | SEC_BIN[23:16] |      |      |      |      |      |      |      |
| Initial value | 0              | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W           | R/W            | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |

**Second Binary Data 3**

|               |                |      |      |      |      |      |      |      |
|---------------|----------------|------|------|------|------|------|------|------|
| Bit No.       | bit7           | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| Bit Name      | SEC_BIN[31:24] |      |      |      |      |      |      |      |
| Initial value | 0              | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W           | R/W            | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |

**Second Binary Data 4**

|               |      |      |      |      |      |      |      |             |
|---------------|------|------|------|------|------|------|------|-------------|
| Bit No.       | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0        |
| Bit Name      | ○    | ○    | ○    | ○    | ○    | ○    | ○    | SEC_BIN[32] |
| Initial value | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0           |
| R/W           | R    | R    | R    | R    | R    | R    | R    | R/W         |

Bits 7–0: SEC\_BIN[7:0] (Second Binary Data 0) , Valid value: 0x00 ~ 0xFF;

SEC\_BIN[15:8] (Second Binary Data 1) , Valid value: 0x00 ~ 0xFF;

SEC\_BIN[23:16] (Second Binary Data 2) , Valid value: 0x00 ~ 0xFF;

SEC\_BIN[31:24] (Second Binary Data 3) , Valid value: 0x00 ~ 0xFF;

Bit 0: SEC\_BIN[32] (Second Binary Data 4) , Valid value: 0x0 ~ 0x1;

The BIN counter value can be set or read through these bits. Writing second data to these registers does not clear Registers SUBSEC\_L and SUBSEC\_H to 0. These registers can be accessed when Register CNTSEL = 0x3 or 0x2.

**0x19: OFS\_SUBSEC\_H (Offset Sub-Second Data High)**

**0x1A: OFS\_SUBSEC\_L (Offset Sub-Second Data Low)**

Offset Sub-Second Data High

| Bit No.       | bit7           | bit6 | bit5 | bit4            | bit3 | bit2 | bit1 | bit0 |
|---------------|----------------|------|------|-----------------|------|------|------|------|
| Bit Name      | OFS_SUBSEC[10] | (GP) | (GP) | OFS_SUBSEC[9:5] |      |      |      |      |
| Initial value | 0              | 0    | 0    | 0               | 0    | 0    | 0    | 0    |
| R/W           | R/W            | R/W  | R/W  | R/W             | R/W  | R/W  | R/W  | R/W  |

**Offset Sub-Second Data Low**

| Bit No.       | bit7            | bit6 | bit5 | bit4 | bit3 | bit2 | bit1  | bit0  |
|---------------|-----------------|------|------|------|------|------|-------|-------|
| Bit Name      | OFS_SUBSEC[4:0] |      |      |      |      | ○    | OFSIN | OFSIN |
| Initial value | 0               | 0    | 0    | 0    | 0    | 0    | 1     | 0     |
| R/W           | R/W             | R/W  | R/W  | R/W  | R/W  | R    | R     | R/W   |

Bit 7: OFS\_SUBSEC[10] (Offset Sub-Second Data High)

Bits 4–0: OFS\_SUBSEC[9:5] (Offset Sub-Second Data High)

Bits 7–3: OFS\_SUBSEC[4:0] (Offset Sub-Second Data Low)

These bits are used to set the offset value for adjusting 1/1024-second time. To directly add the offset value to the 1/1024-second counter, it must be calculated as a 2's complement value with 11-bit data length and set the Bit 10 to the OFS\_SUBSEC [10] bit and Bits 9 to 0 to the OFS\_SUBSEC[9:0] bits.

Bit 1 OFSFIN (Offset Sub-Second Data Low)

This bit indicates the operation status of the 1/1024-second offset correction.

1 (R): Offset correction has completed. Ready for offset correction.

0 (R): Offset correction is in progress.

Bit 0 OFSEN (Offset Sub-Second Data Low)

This bit starts a 1/1024-second offset correction.

1 (W): Start offset correction

0 (W): Ineffective

The offset value will be reflected to the 1/1024-second counter when the second counter is updated immediately

**0x1B: DIG\_TRIM\_H (Digital Trimming Data High)**

**0x1C: DIG\_TRIM\_L (Digital Trimming Data Low)**

**Digital Trimming Data High**

| Bit No.       | bit7       | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------------|------------|------|------|------|------|------|------|------|
| Bit Name      | DTRIM[8:1] |      |      |      |      |      |      |      |
| Initial value | 0          | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W           | R/W        | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |

**Digital Trimming Data Low**

| Bit No. | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------|------|------|------|------|------|------|------|------|
|---------|------|------|------|------|------|------|------|------|

|               |          |   |   |   |   |   |   |         |
|---------------|----------|---|---|---|---|---|---|---------|
| Bit Name      | DTRIM[0] | ○ | ○ | ○ | ○ | ○ | ○ | DTRIMEN |
| Initial value | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0       |
| R/W           | R/W      | R | R | R | R | R | R | R/W     |

Bits 7–0: DTRIM[8:1] (Digital Trimming Data High)

Bit 7: DTRIM[0] (Digital Trimming Data Low)

Bit 0: DTRIMEN :

1 (R/W): Theoretical regulation function is enabled.

0 (R/W): Theoretical regulation function is disabled.

| DTRIM[8:0] Setting Value<br>(1 uint = 0.954ppm) | Theoretical regulation result |
|---|-------------------------------|
| 0x0FF=+255                                      | +243.186ppm                   |
| 0x0FE=+254                                      | +242.232ppm                   |
| ...   |                               |
| 0x003=+3  | 2.861ppm                      |
| 0x002=+2  | 1.907ppm                      |
| 0x001=+1  | 0.954ppm                      |
| 0x000=0   | 0ppm                          |
| 0x1FF=-1  | -0.954ppm                     |
| 0x1FE=-2  | -1.907ppm                     |
| 0x1FD=-3  | -2.861ppm                     |
| ...   |                               |
| 0x102   | -242.232ppm                   |
| 0x101   | -243.186ppm                   |
| 0x100   | Setting prohibited            |

**0x1D: TCTL\_MIR (Mirrored Timer Control, = 0x0D)**

|               |           |      |       |      |      |      |           |      |
|---------------|-----------|------|-------|------|------|------|-----------|------|
| Bit No.       | bit7      | bit6 | bit5  | bit4 | bit3 | bit2 | bit1      | bit0 |
| Bit Name      | FSEL[1:0] |      | USEL0 | TE   | WADA | ○    | TSEL[1:0] |      |
| Initial value | 0         | 0    | 0     | 0    | 0    | 0    | 1         | 0    |
| R/W           | R/W       | R/W  | R/W   | R/W  | R/W  | R    | R/W       | R/W  |

This is a mirror register of Register TCTL. For more information, refer to “0x0D: TCTL (Timer Control).”

**0x1E: INTF\_MIR (Mirrored Status Flag, = 0x0E)**

| Bit No.       | bit7 | bit6    | bit5 | bit4 | bit3 | bit2 | bit1 | bit0   |
|---------------|------|---------|------|------|------|------|------|--------|
| Bit Name      | PORF | OSCSTPF | UF   | TF   | AF   | EVF  | VLF  | VTMPLF |
| Initial value | 1    | 1       | 0    | 0    | 0    | 0    | 1    | 1      |
| R/W           | R/W  | R/W     | R/W  | R/W  | R/W  | R/W  | R/W  | R/W    |

This is a mirror register of Register INTF. For more information, refer to “0x0E: INTF (Status Flag).”

**0x1F: CNTSEL (Counter Select)**

| Bit No.       | bit7 | bit6 | bit5 | bit4 | bit3 | bit2   | bit1     | bit0     |
|---------------|------|------|------|------|------|--------|----------|----------|
| Bit Name      | ○    | ○    | ○    | ○    | ○    | ACCBCD | BINCNTEN | BCDCNTEN |
| Initial value | 0    | 0    | 0    | 0    | 0    | 1      | 1        | 1        |
| R/W           | R    | R    | R    | R    | R    | R/W    | R/W      | R/W      |

**Bit 2: ACCBCD**

This bit selects a clock/calendar counter access mode (selects whether to access the BCD counters [Registers SEC to YEAR] or BIN counter [Registers SEC\_BINn]).

1 (R/W): BCD mode (to read/write the BCD counters)

0 (R/W): BIN mode (to read/write the BIN counter)

**Bit 1: BINCNTEN**

This bit enables/disables the BIN counter to operate.

1 (R/W): BIN counter is enabled.

0 (R/W): BIN counter is disabled.

**Bit 0: BCDCNTEN**

This bit enables/disables the BCD counters to operate.

1 (R/W): BCD counters are enabled.

0 (R/W): BCD counters are disabled.

**0x20: EVIN\_EN (Event Input Enable)**

| Bit No.       | bit7 | bit6 | bit5 | bit4      | bit3      | bit2 | bit1    | bit0    |
|---------------|------|------|------|-----------|-----------|------|---------|---------|
| Bit Name      | ○    | ○    | ○    | EVIN2CPEN | EVIN1CPEN | ○    | EVIN1EN | EVIN1EN |
| Initial value | 0    | 0    | 0    | 0         | 0         | 0    | 0       | 0       |
| R/W           | R    | R    | R    | R/W       | R/W       | R    | R/W     | R/W     |

**Bit 4 EVIN2CPEN**

Bit 3 EVIN1CPEN

These bits enable/disable external event trigger inputs from the EVINn pin to capture time stamp data to the buffer.

1 (R/W): EVINn is enabled to capture time stamp data.

0 (R/W): EVINn is disabled to capture time stamp data.

The EVINnCPEN bit setting is effective when the EVINnEN bit (described below) = 1.

Bit 1 EVIN2EN

Bit 0 EVIN1EN

These bits enable/disable the EVINn pin to input external event triggers.

1 (R/W): EVINn is enabled to input event triggers.

0 (R/W): EVINn is disabled to input event triggers.

**0x21: EVIN1\_CFG (EVIN1 Configuration)**

**0x23: EVIN2\_CFG (EVIN2 Configuration)**

| Bit No.       | bit7 | bit6 | bit5 | bit4      | bit3 | bit2 | bit1     | bit0 |
|---------------|------|------|------|-----------|------|------|----------|------|
| Bit Name      | ○    | ○    | ○    | PUPD[2:0] |      |      | POL[1:0] |      |
| Initial value | 0    | 0    | 0    | 0         | 1    | 0    | 0        | 0    |
| R/W           | R    | R    | R    | R/W       | R/W  | R/W  | R/W      | R/W  |

Bits 4–2: PUPD[2:0]

These bits select an internal pull-up or pull-down resistor to be connected to the EVINn pin.

EVINn Pin Pull-Up/Pull-Down Resistor Selections

| EVINn_CFG.PUPD[2:0] | Pull-up/down resistor           |
|---------------------|---------------------------------|
| 0b000               | No pull-up/pull-down resistor   |
| 0b001               | Pull-up resistor 500 kΩ         |
| 0b010               | Pull-up resistor 1 MΩ (default) |
| 0b011               |                                 |
| 0b100               | Pull-down resistor 500 kΩ       |
| Other               | No pull-up/pull-down resistor   |

Bits 1–0: POL[1:0]

These bits select the EVINn input signal detection edge polarity that captures time stamp data.

Selecting EVINn Input Signal Detection Edge Polarity

| EVINn_CFG.POL[1:0] | Pull-up/down resistor |
|--------------------|-----------------------|
|                    |                       |

|      |                         |
|------|-------------------------|
| 0b00 | Falling edge (default)  |
| 0b01 | Rising edge             |
| 0b10 | Falling and Rising edge |
| 0b11 |                         |

**0x22: EVIN1\_FLT (EVIN1 Noise Filter)**
**0x24: EVIN2\_FLT (EVIN2 Noise Filter)**

| Bit No.       | bit7 | bit6 | bit5     | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------------|------|------|----------|------|------|------|------|------|
| Bit Name      | ○    | ○    | FLT[5:0] |      |      |      |      |      |
| Initial value | 0    | 0    | 0        | 0    | 0    | 0    | 0    | 0    |
| R/W           | R    | R    | R/W      | R/W  | R/W  | R/W  | R/W  | R/W  |

Bits 5–0: FLT[5:0]

These bits set the noise filtering time for the EVINn input signals.

**Noise Filtering Time for EVINn Input**

| EVINn_FLT.FLT[5:0]                | Uncertain EVINn pulse width<br>(Whether the edge input is detected or not depends on the relationship between the edge input timing and the sampling timing in 125 ms cycles.) | Valid EVINn pulse width<br>(The edge input is always detected.) |
|-----------------------------------|--|---|
| 0x00                              | ○  | 1 ms or more  |
| 0x01 (Setting prohibited)         | ○  | ○   |
| 0x02                              | 125 ms or more and less than 250 ms  | 250 ms or more  |
| 0x03                              | 125 ms or more and less than 250 ms  | 375 ms or more  |
| :                                 | :  | :   |
| 0x27                              | 125 ms or more and less than 250 ms  | 4875 ms or more   |
| 0x28                              | 125 ms or more and less than 250 ms  | 5000 ms or more   |
| 0x29 or more (Setting prohibited) | ○  | ○   |

**0x27: BUF1\_CFG1 (BUF1 Configuration 1)**

| Bit No.       | bit7   | bit6  | bit5 | bit4 | bit3 | bit2    | bit1    | bit0   |
|---------------|--------|-------|------|------|------|---------|---------|--------|
| Bit Name      | BINSEL | OVWEN | ○    | ○    | ○    | FULLIEN | EMPTIEN | OVWIEN |
| Initial value | 0      | 0     | 0    | 0    | 0    | 0       | 0       | 0      |
| R/W           | R/W    | R/W   | R    | R    | R    | R/W     | R/W     | R/W    |

**Bit 7: BINSEL**

This bit selects either the BCD counter or the BIN counter to capture date and time data to be recorded to the buffer when an event occurs.

1 (R/W): BIN counter data is captured.

0 (R/W): BCD counter data is captured.

**Bit 6: OVWEN**

This bit sets the write mode after the buffer becomes full (after captured data is written to Bank 7).

1 (R/W): Overwrite mode (Bank 7 is overwritten.)

0 (R/W): Overwrite Inhibit mode (recording stops in buffer full state, captured data are discarded.)

**Bit 2: FULLIEN**

This bit enables/disables buffer full interrupts.

1 (R/W): Buffer full interrupts are enabled.

0 (R/W): Buffer full interrupts are disabled.

When this bit is set to 1, the interrupt flag (BUF1\_STAT.FULLF bit) will be set to 1 if a buffer full status occurs.

**Bit 1: EMPTIEN**

This bit enables/disables buffer not empty interrupts.

1 (R/W): Buffer not empty interrupts are enabled.

0 (R/W): Buffer not empty interrupts are disabled.

When this bit is set to 1, the interrupt flag (BUF1\_STAT.EMPTF bit) will be set to 1 if time stamp data is written to the buffer in empty status.

**Bit 0: OVWIEN** This bit enables/disables buffer overwrite interrupts.

1 (R/W): Buffer overwrite interrupts are enabled.

0 (R/W): Buffer overwrite interrupts are disabled.

When this bit is set to 1, the interrupt flag (BUF1\_STAT.OVWF bit) will be set to 1 if a time stamp is captured while the buffer is in full status.

**0x28: BUF1\_STAT (BUF1 Status)**

| Bit No.       | bit7  | bit6  | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------------|-------|-------|------|------|------|------|------|------|
| Bit Name      | FULLF | EMPTF | ○    | ○    | ○    | ○    | ○    | OVWF |
| Initial value | 0     | 1     | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W           | R/W   | R/W   | R    | R    | R    | R    | R    | R/W  |

**Bit 7: FULLF**

This flag indicates whether the buffer is in full status or not.

1 (R): Buffer full status

0 (R):Free space available in the buffer

This flag is set to 1 if a newly captured time stamp data is written to the Bank 7 buffer when data has



been written to the Bank 6 buffer only.

**Bit 6: EMPTF**

This flag indicates whether the buffer is in empty status or not.

1 (R): Buffer empty status

0 (R): Buffer data available

This flag is initially set to 1 and cleared to 0 when the 1st captured time stamp data is written to the Bank 6 buffer.

**Bit 0: OVWF**

This flag indicates whether a new time stamp data is captured or not while the buffer is in full status. Overwrite Inhibit mode

1 (R): Data has been captured while the buffer is in full status (the latest data was destroyed).

0 (R): Data has not been captured after the buffer becomes full.

Overwrite mode

1 (R): Overwriting has occurred (Bank 7 was overwritten with the latest data).

0 (R): Overwriting has not occurred.

This flag is set to 1 when a new time stamp data is captured while the buffer is in full status.

**Note:**

The flags in this register cannot be reset by reading the buffer. To reset the flags, it is necessary to issue a command trigger (writing to Register WRCMD\_TRG) with the WRCMD\_CFG.BUF1FCLREN bit set to 1.

**0x29: BUF1\_CFG2 (BUF1 Configuration 2)**

| Bit No.       | bit7 | bit6    | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------------|------|---------|------|------|------|------|------|------|
| Bit Name      | ○    | SRAMMOD | ○    | ○    | ○    | ○    | ○    | ○    |
| Initial value | 0    | 0       | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W           | R    | R/W     | R    | R    | R    | R    | R    | R    |

**Bit 6: SRAMMOD**

This bit enables/disables SRAM mode for reading/writing from/to the buffer.

1 (R/W): SRAM mode is enabled.

0 (R/W): SRAM mode is disabled.

**0x30: ALM\_SEC (Second Alarm)**

| Bit No.       | bit7 | bit6        | bit5 | bit4 | bit3        | bit2 | bit1 | bit0 |
|---------------|------|-------------|------|------|-------------|------|------|------|
| Bit Name      | XSAE | SALM_H[2:0] |      |      | SALM_L[3:0] |      |      |      |
| Initial value | 0    | 0           | 0    | 0    | 0           | 0    | 0    | 0    |
| R/W           | R/W  | R/W         | R/W  | R/W  | R/W         | R/W  | R/W  | R/W  |

Bit 7: XSAE

This bit enables/disables the second alarm setting.

1 (R/W): Second alarm is disabled.

0 (R/W): Second alarm is enabled.

Bits 3–0: SALM\_L[3:0]

Bits 6-4: SALM\_H[2:0]

These bits set the second alarm condition in a BCD code.

The SALM\_H[2:0] bits specify the 10-second digit (0–5) and the SALM\_L[3:0] bits specify 1-second digit (0–9).

### 0x31: ALM\_MIN\_MIR (Mirrored Minute Alarm, = 0x07)

| Bit No.       | bit7 | bit6        | bit5 | bit4 | bit3        | bit2 | bit1 | bit0 |
|---------------|------|-------------|------|------|-------------|------|------|------|
| Bit Name      | XMAE | MALM_H[2:0] |      |      | MALM_L[3:0] |      |      |      |
| Initial value | 1    | 0           | 0    | 0    | 0           | 0    | 0    | 0    |
| R/W           | R/W  | R/W         | R/W  | R/W  | R/W         | R/W  | R/W  | R/W  |

This is a mirror register of Register ALM\_MIN. For more information, refer to “0x07: ALM\_MIN (Minute Alarm).”

### 0x32: ALM\_HOUR\_MIR (Mirrored Hour Alarm, = 0x08)

| Bit No.       | bit7 | bit6 | bit5        | bit4 | bit3        | bit2 | bit1 | bit0 |
|---------------|------|------|-------------|------|-------------|------|------|------|
| Bit Name      | XHAE | (GP) | HALM_H[1:0] |      | HALM_L[3:0] |      |      |      |
| Initial value | 1    | 0    | 0           | 0    | 0           | 0    | 0    | 0    |
| R/W           | R/W  | R/W  | R/W         | R/W  | R/W         | R/W  | R/W  | R/W  |

This is a mirror register of Register ALM\_HOUR. For more information, refer to “0x08: ALM\_HOUR (Hour Alarm).”

### 0x33: ALM\_WEEKDAY\_MIR (Mirrored Day-of-Week Alarm / Day Alarm, = 0x09)

#### Mirrored Day-of-Week Alarm

| Bit No.       | bit7 | bit6       | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------------|------|------------|------|------|------|------|------|------|
| Bit Name      | XWAE | WKALM[6:0] |      |      |      |      |      |      |
| Initial value | 1    | 0          | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W           | R/W  | R/W        | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |

### Mirrored Day Alarm

| Bit No.       | bit7 | bit6 | bit5        | bit4 | bit3        | bit2 | bit1 | bit0 |
|---------------|------|------|-------------|------|-------------|------|------|------|
| Bit Name      | XWAE | (GP) | DALM_H[1:0] |      | DALM_L[3:0] |      |      |      |
| Initial value | 1    | 0    | 0           | 0    | 0           | 0    | 0    | 0    |
| R/W           | R/W  | R/W  | R/W         | R/W  | R/W         | R/W  | R/W  | R/W  |

This is a mirror register of Register ALM\_WEEKDAY. For more information, refer to “0x09: ALM\_WEEKDAY (Day-of-Week Alarm / Day Alarm).”

### 0x34: UPDISEL (Time Update Interrupt Select)

| Bit No.       | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1  | bit0 |
|---------------|------|------|------|------|------|------|-------|------|
| Bit Name      | ○    | ○    | ○    | ○    | ○    | ○    | USEL1 | ○    |
| Initial value | 0    | 0    | 0    | 0    | 0    | 0    | 0     | 0    |
| R/W           | R    | R    | R    | R    | R    | R    | R/W   | R    |

#### Bit 1: USEL1

This bit selects a time update interrupt event by using it together with the TCTL.USEL0 bit

### 0x38: WTICFG (Wakeup Timer Interrupt Configuration)

| Bit No.       | bit7        | bit6 | bit5        | bit4 | bit3    | bit2  | bit1   | bit0      |
|---------------|-------------|------|-------------|------|---------|-------|--------|-----------|
| Bit Name      | PINMUX[1:0] |      | RSTOPT[1:0] |      | WTNETIM | TSEL2 | WTIOUT | UPDOWNMOD |
| Initial value | 0/1         | 0/1  | 0           | 0    | 0       | 0     | 0      | 0         |
| R/W           | R/W         | R/W  | R/W         | R/W  | R/W     | R/W   | R/W    | R/W       |

#### Bits 7–6: PINMUX[1:0]

Be sure to avoid changing these bits from the initial value, otherwise, unexpected pin functions may be assigned.

WTICFG.PINMUX[1:0] Bit Initial Value of Each Product

#### Bits 5–4: RSTOPT[1:0]

These bits select whether to disable the inputs/outputs or not while the reset signal (/RST) is being output. When the input pins are disabled, they can be placed into a Hi-Z state. When the output pins are disabled, they go into a Hi-Z state. Disable: Inputs/outputs are disabled while /RST = L (power supply voltage drop is detected). Enable: Inputs/outputs are not disabled while /RST = L (power supply voltage drop is detected). This function is effective only in the models with the /RST pin function.

#### Selecting Reset Output Option

| WTICFG. RSTOPT[1:0] | FOE, CE, CLK, DI (DIO), SCL, SDA pin inputs DO pin output | FOUT, /INT, SOUT pin outputs |
|---------------------|---|------------------------------|
| 0b00                | Disabled(default)   | Disabled(default)            |

|      |          |          |
|------|----------|----------|
| 0b01 | Disabled | Enabled  |
| 0b10 | Enabled  | Disabled |
| 0b11 | Enabled  | Enabled  |

**Bit 3: WTONETIM Enabled**

This bit selects whether to automatically negate the /INT output or not after a wakeup timer interrupt occurs.

1 (R/W): Not negated automatically (low output)

0 (R/W): Negated automatically (7.812 ms width low pulse output)

**Bit 2: TSEL2**

This bit selects an external clock as the wakeup timer source clock.

1 (R/W): External clock input to the EVIN2 pin

0 (R/W): Internal clock selected with the TCTL.TSEL[1:0] bits

**Bit 1: WTIOOUT**

This bit selects the wakeup timer interrupt signal output pin.

1 (R/W): Output from the FOUT pin (CMOS buffer output)

0 (R/W): Output from the /INT pin (Open drain output)

**Note:**

When using the FOUT pin only for the wakeup timer interrupt signal output, set the TCTL.FSEL[1:0] bits to 0b11 to disable the FOUT output.

**Bit 0: UPDOWNMOD**

This bit sets the wakeup timer count mode.

1 (R/W): Count-up mode

0 (R/W): Count-down mode

**0x39: WTCTL (Wakeup Timer Control)**

| Bit No.       | bit7  | bit6      | bit5          | bit4 | bit3     | bit2      | bit1 | bit0   |
|---------------|-------|-----------|---------------|------|----------|-----------|------|--------|
| Bit Name      | WTRST | EXWTRSTEN | WTRSTWIN[1:0] |      | WTMODSEL | WTSTOPCTL | ○    | WTSTOP |
| Initial value | 0/1   | 0/1       | 0             | 0    | 0        | 0         | 0    | 0      |
| R/W           | R/W   | R/W       | R/W           | R/W  | R/W      | R/W       | R    | R/W    |

**Bit 7: WTRST**

This bit reloads the preset value to the wakeup timer.

1 (W): Timer is preset.

0 (W): Ineffective

Writing 1 to this bit reloads the preset value to the wakeup timer counter in Count-down mode or reloads 1 in Count-up mode, and then restarts the count operation. This makes it possible to use the wakeup timer as a watchdog timer.

This bit is always read as 0 even after writing 1.

Bit 6: EXWTRSTEN

This bit enables/disables resetting the wakeup timer by an external input signal.

1 (W): External input reset is enabled.

0 (W): External input reset is disabled.

When the EXWTRSTEN bit is set to 1, the wakeup timer is reset by inputting a high pulse to the EVIN2 pin. This external input reset can be used in combination with the WTRST bit reset.

Bits 5–4: WTRSTWIN[1:0]

These bits specify the reset acceptance period (reset window) for the wakeup timer set into Count-down mode. This limitation of reset acceptance period is applied to both resets by the WTRST bit and external signal input.

Reset Window Settings

| WTCTL. WTRSTWIN[1:0] | Reset acceptance period (Count-down mode) |
|----------------------|---|
| 0b00                 | Whole period (default)                    |
| 0b01                 | Counter value = 2 to 1                    |
| 0b10                 | Counter value = 16 to 1                   |
| 0b11                 | Counter value = 64 to 1                   |

Bit 3: WTMODSEL

This bit restricts the wakeup timer to operate either in Normal mode (reset output is cancelled) or Safe mode (during reset output).

When WTSTOPCTL is set to 1.

1 (R/W): The timer work on Normal mode.

0 (R/W): The timer work on Safe mode.

When WTSTOPCTL is set to 0, this bit is disabled. Timer work on Normal mode and Safe mode.

Bit 2: WTSTOPCTL

This bit enables/disables the WTMODSEL and WTSTOP bit functions.

1 (R/W): WTMODSEL is enabled and WTSTOP is disabled.

0 (R/W): WTMODSEL is disabled and WTSTOP is enabled.

Bit 0: WTSTOP

This bit temporarily stops the wakeup timer.

1 (R/W): The wakeup timer is stopped.

0 (R/W): The wakeup timer stop state is cancelled (the wakeup timer is operating normally).

### 0x3A: WTCNT\_L\_MIR (Mirrored Wakeup Timer Counter Low, = 0x0A)

### 0x3B: WTCNT\_M\_MIR (Mirrored Wakeup Timer Counter Middle, = 0x0B)

### 0x3C: WTCNT\_H\_MIR (Mirrored Wakeup Timer Counter High, = 0x0C)

#### Mirrored Wakeup Timer Counter Low

| Bit No.       | bit7       | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------------|------------|------|------|------|------|------|------|------|
| Bit Name      | WTCNT[7:0] |      |      |      |      |      |      |      |
| Initial value | 0          | 0    | 0    | 0    | 0    | 0    | 0    | 1    |
| R/W           | R/W        | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |

#### Mirrored Wakeup Timer Counter Middle

| Bit No.       | bit7        | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------------|-------------|------|------|------|------|------|------|------|
| Bit Name      | WTCNT[15:8] |      |      |      |      |      |      |      |
| Initial value | 0           | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W           | R/W         | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |

#### Mirrored Wakeup Timer Counter High

| Bit No.       | bit7         | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------------|--------------|------|------|------|------|------|------|------|
| Bit Name      | WTCNT[23:16] |      |      |      |      |      |      |      |
| Initial value | 0            | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W           | R/W          | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |

These are mirror registers of Registers WTCNT\_L, WTCNT\_M, and WTCNT\_H. For more information, refer to “0x0A–0x0C: WTCNT\_L/WTCNT\_M/WTCNT\_H (Wakeup Timer Counter Low/Middle/High).”

### 0x3D: TCTL\_MIR (Mirrored Timer Control, = 0x0D)

| Bit No.       | bit7      | bit6 | bit5  | bit4 | bit3 | bit2 | bit1      | bit0 |
|---------------|-----------|------|-------|------|------|------|-----------|------|
| Bit Name      | FSEL[1:0] |      | USEL0 | TE   | WADA | ○    | TSEL[1:0] |      |
| Initial value | 0         | 0    | 0     | 0    | 0    | 0    | 1         | 0    |
| R/W           | R/W       | R/W  | R/W   | R/W  | R/W  | R/W  | R/W       | R/W  |

This is a mirror register of Register TCTL. For more information, refer to “0x0D: TCTL (Timer Control).”

### 0x3E: INTF\_MIR (Mirrored Status Flag, = 0x0E)

| Bit No. | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------|------|------|------|------|------|------|------|------|
|---------|------|------|------|------|------|------|------|------|

| Bit Name      | PORF | OSCSTPF | UF  | TF  | AF  | EVF | VLF | VTMPLF |
|---------------|------|---------|-----|-----|-----|-----|-----|--------|
| Initial value | 1    | 1       | 0   | 0   | 0   | 0   | 1   | 1      |
| R/W           | R/W  | R/W     | R/W | R/W | R/W | R/W | R/W | R/W    |

This is a mirror register of Register INTF. For more information, refer to “0x0E: INTF (Status Flag).”

### 0x3F: TSTP\_INTE\_MIR (Mirrored Timer Stop and Interrupt Enable, = 0x0F)

| Bit No.       | bit7      | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------------|-----------|------|------|------|------|------|------|------|
| Bit Name      | CSEL[1:0] |      | UIE  | TIE  | AIE  | EIE  | ○    | STOP |
| Initial value | 0         | 1    | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W           | R/W       | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |

This is a mirror register of Register TSTP\_INTE. For more information, refer to “0x0F: TSTP\_INTE (Timer Stop and Interrupt Enable).”

### 0x41: WRCMD\_CFG (Write Command Configuration)

| Bit No.       | bit7       | bit6 | bit5 | bit4       | bit3 | bit2 | bit1 | bit0     |
|---------------|------------|------|------|------------|------|------|------|----------|
| Bit Name      | EVCNTCLREN | ○    | ○    | BUF1FCLREN | ○    | ○    | ○    | CMDTRGEN |
| Initial value | 0          | 0    | 0    | 0          | 0    | 0    | 0    | 0        |
| R/W           | R/W        | R    | R    | R/W        | R    | R    | R    | R/W      |

#### Note:

This register specifies the functions that will be executed when any data is written to Register WRCMD\_TRG (Address 0x42).

#### Bit 7: EVCNTCLREN

This bit specifies whether to initialize the event counters or not when a command trigger is executed by writing to Register WRCMD\_TRG.

1 (R/W): Event counter is initialized.

0 (R/W): Event counter is not initialized.

Executing a command trigger with this bit set to 1 initializes the EVIN1 and 2 event input counters shown below to clear to 0.

EVIN1\_EVCNT.EVCNT[5:0] bits (EVIN1 event counter)

EVIN2\_EVCNT.EVCNT[5:0] bits (EVIN2 event counter)

#### Bit 4: BUF1FCLREN

This bit specifies whether to initialize the buffer status flags when a command trigger is executed.

1 (R/W): Buffer status flag is initialized.

0 (R/W): Buffer status flag is not initialized.

Executing a command trigger with this bit set to 1 initializes the buffer status flags shown below to set the buffer into empty status.

BUF1\_STAT.FULLF bit (Buffer full flag)

BUF1\_STAT.EMPTF bit (Buffer empty flag)

BUF1\_STAT.OVWF bit (Buffer overwrite flag)

Bit 0: CMDTRGEN

This bit specifies whether to issue a time stamp trigger when a command trigger is executed.

1 (R/W): Time stamp trigger is issued.

0 (R/W): Time stamp trigger is not issued.

**0x42: WRCMD\_TRG (Write Command Trigger)**

| Bit No.       | bit7       | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------------|------------|------|------|------|------|------|------|------|
| Bit Name      | WRTRG[7:0] |      |      |      |      |      |      |      |
| Initial value | 0          | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W           | R/W        | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |

Bits 7–0:WRTRG[7:0]

By writing any value to this address, a command trigger is issued to execute the command configured in Register WRCMD\_CFG (Address 0x41).

**0x43: EVNT\_INTE (Event Interrupt Enable)**

| Bit No.       | bit7 | bit6     | bit5     | bit4    | bit3 | bit2    | bit1 | bit0      |
|---------------|------|----------|----------|---------|------|---------|------|-----------|
| Bit Name      | ○    | EVIN2IEN | EVIN1IEN | RSTOIEN | ○    | VTMPIEN | ○    | OSCSTPIEN |
| Initial value | 0    | 0        | 0        | 0       | 0    | 0       | 0    | 0         |
| R/W           | R    | R/W      | R/W      | R/W     | R    | R/W     | R    | R/W       |

Bit 6: EVIN2IEN

Bit 5: EVIN1IEN

These bits enable/disable the EVINn event input to generate interrupts.

1 (R/W): EVINn event input interrupts are enabled.

0 (R/W): EVINn event input interrupts are disabled.

Bit 4: RSTOIEN

This bit enables/disables the reset output function (to detect if the VDD voltage drops below the VDD drop detection voltage) to issue event triggers. This bit is effective only in the models with the /RST pin.



1 (R/W): Reset output event trigger is enabled.

0 (R/W): Reset output event trigger is disabled.

If this bit has been set to 1, an event flag (EVNT\_INTF.RSTOEVF bit) is set to 1 when a reset output is started (VDD voltage drop below the VDD drop detection voltage is detected).

**Bit 2: VTMP LIEN**

This bit enables/disables the  $V_{TEMP}$  voltage drop detection function (to detect if the VDD voltage drops below the lower limit of temperature compensation operating voltage for the oscillator circuit) to issue event triggers.

1 (R/W):  $V_{TEMP}$  voltage drop detection event trigger is enabled

0 (R/W):  $V_{TEMP}$  voltage drop detection event trigger is disabled.

If this bit has been set to 1, an event flag (EVNT\_INTF.VTMP LEVF bit) is set to 1 when a  $V_{TEMP}$  voltage drop is detected.

**Bit 0: OSCSTPIEN**

This bit enables/disables the oscillation stop detection function to issue event triggers.

1 (R/W): Oscillation stop detection event trigger is enabled.

0 (R/W): Oscillation stop detection event trigger is disabled.

If this bit has been set to 1, an event flag (EVNT\_INTF.OSCSTPEVF bit) is set to 1 when an oscillation stoppage is detected.

**0x44: CAP\_EN (Capture Enable)**

| Bit No.       | bit7 | bit6 | bit5 | bit4     | bit3 | bit2      | bit1 | bit0       |
|---------------|------|------|------|----------|------|-----------|------|------------|
| Bit Name      | ○    | ○    | ○    | RSTOCPEN | ○    | VTMPLCPEN | ○    | OSCSTPCPEN |
| Initial value | 0    | 0    | 0    | 0        | 0    | 0         | 0    | 0          |
| R/W           | R    | R    | R    | R/W      | R    | R/W       | R    | R/W        |

**Bit 4: RSTOCPEN**

This bit enables/disables the reset output (to detect if the VDD voltage drops below the VDD drop detection voltage) event trigger to capture time stamp data.

1 (R/W): Reset output time stamp capturing is enabled.

0 (R/W): Reset output time stamp capturing is disabled.

**Bit 2: VTMPLCPEN**

This bit enables/disables the VDET2 voltage drop detection (to detect if the VDD voltage drops below the lower limit of temperature compensation operating voltage for the oscillator circuit) event trigger to capture time stamp data.

1 (R/W):  $V_{TEMP}$  voltage drop detection time stamp capturing is enabled.

0 (R/W): V<sub>TEMP</sub> voltage drop detection time stamp capturing is disabled.

Bit 0: OSCSTPCPEN

This bit enables/disables the oscillation stop detection event trigger to capture time stamp data.

1 (R/W): Oscillation stop detection time stamp capturing is enabled.

0 (R/W): Oscillation stop detection time stamp capturing is disabled.

**0x45: INTF\_MIR (Mirrored Status Flag, = 0x0E)**

| Bit No.       | bit7 | bit6    | bit5 | bit4 | bit3 | bit2 | bit1 | bit0   |
|---------------|------|---------|------|------|------|------|------|--------|
| Bit Name      | PORF | OSCSTPF | UF   | TF   | AF   | EVF  | VLF  | VTMPLF |
| Initial value | 1    | 1       | 0    | 0    | 0    | 0    | 1    | 1      |
| R/W           | R/W  | R/W     | R/W  | R/W  | R/W  | R    | R/W  | R/W    |

This is a mirror register of Register INTF. For more information, refer to “0x0E: INTF (Status Flag).”

**0x46: BUF\_INTF (Buffer Interrupt Factor)**

| Bit No.       | bit7 | bit6 | bit5  | bit4  | bit3 | bit2 | bit1 | bit0 |
|---------------|------|------|-------|-------|------|------|------|------|
| Bit Name      | ○    | ○    | BUF1F | RSTOF | ○    | ○    | ○    | ○    |
| Initial value | 0    | 0    | 0     | 1     | 0    | 0    | 0    | 0    |
| R/W           | R    | R    | R     | R/W   | R    | R    | R    | R    |

Bit 5: BUF1F

These flags indicate that a time stamp buffer event trigger input interrupt factor has occurred.

1 (R): An event trigger input has occurred.

0 (R): No event trigger input has occurred.

This flag is set to 1 when a buffer full occurred.

The BUF1F bit is cleared to 0 when a command trigger for resetting these flags (BUF1\_STAT.FULLF bit = 0, BUF1\_STAT.EMPTF bit = 1, BUF1\_STAT.OVWF bit = 0) is issued. This flag must be cleared to accept the subsequent event and to output an interrupt.

Bit 4: RSTOF

This flag is set when a reset output has started (VDD voltage drop below the VDD drop detection voltage is detected).

1 (R): Reset output has started. (VDD voltage drop below -V<sub>DET</sub> has been detected.)

0 (R): Reset output has not started. (No VDD voltage drop has been detected.)

1 (W): Ineffective

0 (W): Flag clear (Takes effect after the VDD voltage is restored.)

If a VDD voltage drop status is being continued, this flag cannot be cleared by writing 0. This flag must be cleared to accept the subsequent event and to output an interrupt.

**0x47: EVNT\_INTF (Event Interrupt Factor)**

| Bit No.       | bit7 | bit6   | bit5   | bit4    | bit3 | bit2     | bit1 | bit0      |
|---------------|------|--------|--------|---------|------|----------|------|-----------|
| Bit Name      | ○    | EVIN2F | EVIN1F | RSTOEVF | ○    | VTMPLEVF | ○    | OSCSTPEVF |
| Initial value | 0    | 0      | 0      | 0       | 0    | 0        | 0    | 0         |
| R/W           | R    | R/W    | R/W    | R/W     | R    | R/W      | R    | R/W       |

Bit 6: EVIN2F

Bit 5: EVIN1F

These flags indicate that an event input has occurred to EVINn.

1 (R): An EVINn event input has occurred.

0 (R): No EVINn event input has occurred.

1 (W): Ineffective

0 (W): Flag clear

Bit 4: RSTOEVF

This flag indicates that a reset output event (the VDD voltage drops below the VDD drop detection voltage) has occurred.

1 (R): Reset output event has occurred.

0 (R): No reset output event has occurred.

1 (W): Ineffective

0 (W): Flag clear

Bit 2: VTMPLEVF

This flag indicates that a VDET2 voltage drop detection event (the VDD voltage drops below the lower limit of temperature compensation operating voltage for the oscillator circuit) has occurred.

1 (R): A VDET2 voltage drop detection event has occurred.

0 (R): No VDET2 voltage drop detection event has occurred.

1 (W): Ineffective

0 (W): Flag clear

Bit 0: OSCSTPEVF

This flag indicates that an oscillation stop detection event has occurred.

1 (R): An oscillation stop detection event has occurred.

0 (R): No oscillation stop detection event has occurred.

1 (W): Ineffective

0 (W): Flag clear

When an oscillation stop detection event has occurred, time stamp data will be captured after the oscillation restarts.

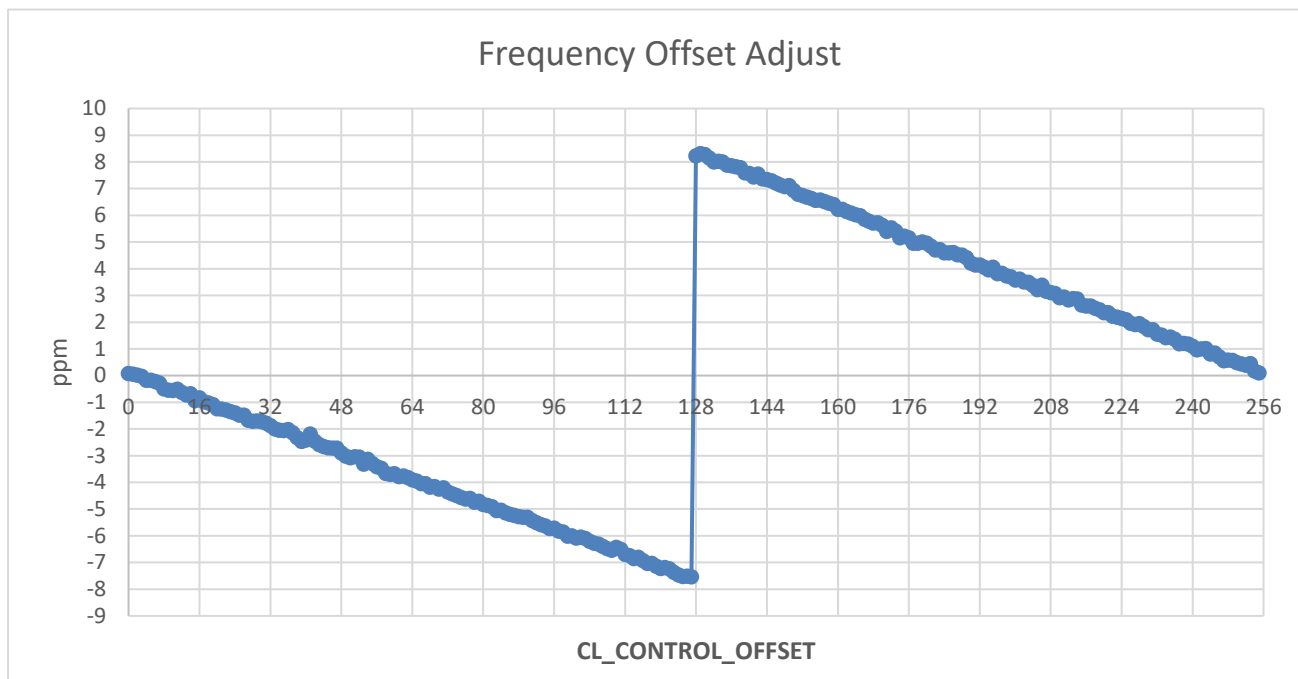
**0x4B: CL\_CONTROL\_OFFSET**

| Bit No.       | bit7                   | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------------|------------------------|------|------|------|------|------|------|------|
| Bit Name      | CL_CONTROL_OFFSET[7:0] |      |      |      |      |      |      |      |
| Initial value | 0                      | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W           | R/W                    | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |

As the frequency offset adjust register, step is about 0.063ppm.

| CL_CONTROL_OFFSET[7:0] | The adjusted ppm of the theory |
|------------------------|--------------------------------|
| 0x7F                   | 8.001ppm                       |
| 0x7E                   | 7.938ppm                       |
| 0x7D                   | 7.875ppm                       |
| ...                    |                                |
| 0x03                   | 0.189ppm                       |
| 0x02                   | 0.126ppm                       |
| 0x01                   | 0.063ppm                       |
| 0x00                   | 0ppm                           |
| 0xFF                   | -0.063ppm                      |
| 0xFE                   | -0.126ppm                      |
| 0xFD                   | -0.189ppm                      |
| ...                    |                                |
| 0x83                   | -7.875ppm                      |
| 0x82                   | -7.938ppm                      |
| 0x81                   | -8.001ppm                      |
| 0x80                   | Setting prohibited             |

frequency offset adjust data for reference:



**0x4C: TEMP\_CL\_FIT**

| Bit No.       | bit7 | bit6 | bit5 | bit4 | bit3             | bit2 | bit1               | bit0 |
|---------------|------|------|------|------|------------------|------|--------------------|------|
| Bit Name      | ○    | ○    | ○    | ○    | CL_ALFA_CFG[1:0] |      | TEMP_ALFA_CFG[1:0] |      |
| Initial value | 0    | 0    | 0    | 0    | 0                | 0    | 0                  | 0    |
| R/W           | R/W  | R/W  | R/W  | R/W  | R/W              | R/W  | R/W                | R/W  |

Bit 3-2 CL\_ALFA\_CFG:

Temperature-compensated capacitive filtering.

| CL_ALFA_CFG[1:0] | Description  |
|------------------|--|
| 2b'00            | The proportion of the new CL: 100%, filtering has no effect. |
| 2b'01            | The proportion of the new CL: 1/8.                           |
| 2b'10            | The proportion of the new CL: 1/4.                           |
| 2b'11            | The proportion of the new CL: 1/2.                           |

Bit 1-0 TEMP\_ALFA\_CFG:

Temperature-compensated temperature filtering.

| TEMP_ALFA_CFG[1:0] | Description   |
|--------------------|---|
| 2b'00              | The proportion of the new temperature: 100%, filtering has no effect. |
| 2b'00              | The proportion of the new temperature: 1/2.                           |
| 2b'00              | The proportion of the new temperature: 1/4.                           |
| 2b'00              | The proportion of the new temperature: 1/8.                           |

**0x4D: SOFT\_RST1**

| Bit No.       | bit7           | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------------|----------------|------|------|------|------|------|------|------|
| Bit Name      | SOFT_RST1[7:0] |      |      |      |      |      |      |      |
| Initial value | 0              | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W           | R/W            | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |

**0x4E: SOFT\_RST2**

| Bit No.       | bit7           | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------------|----------------|------|------|------|------|------|------|------|
| Bit Name      | SOFT_RST2[7:0] |      |      |      |      |      |      |      |
| Initial value | 0              | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W           | R/W            | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |

Soft reset function:

This function is used to reset the chip by software, after chip reset, all registers will set to its default value.

Please write below registers to reset chip:

0x4D = 0x00, 0x4E = 0x00; 0x4D = 0xA5, 0x4E = 0xD7;

**0x51: EVIN1\_EVCNT (EVIN1 Event Counter)**
**0x52: EVIN2\_EVCNT (EVIN2 Event Counter)**

| Bit No.       | bit7 | bit6 | bit5       | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------------|------|------|------------|------|------|------|------|------|
| Bit Name      | ○    | ○    | EVCNT[5:0] |      |      |      |      |      |
| Initial value | 0    | 0    | 0          | 0    | 0    | 0    | 0    | 0    |
| R/W           | R    | R    | R          | R    | R    | R    | R    | R    |

Bits 5–0: EVCNT[5:0]

These bits indicate the event count (0 to 63 times) input to the EVINn pin.

If the input count exceeds 63 times, the counter reverts to 0 and continues counting. The EVINn event

counter does not operate when the EVIN\_EN.EVINnEN bit = 0.

**0x54: EVINMON (EVIN Monitor)**

| Bit No.       | bit7 | bit6     | bit5     | bit4 | bit3 | bit2 | bit1 | bit0 |
|---------------|------|----------|----------|------|------|------|------|------|
| Bit Name      | ○    | EVIN2MON | EVIN1MON | ○    | ○    | ○    | ○    | ○    |
| Initial value | 0    | 0        | 0        | 0    | 0    | 0    | 0    | 0    |
| R/W           | R    | R        | R        | R    | R    | R    | R    | R    |

Bit 6: EVIN2MON

Bit 5: EVIN1MON

These bits indicate the current input level on the EVINn pin.

1 (R): High level

0 (R): Low level

**0x55: SOUTCTL (SOUT Control)**

| Bit No.       | bit7 | bit6 | bit5 | bit4 | bit3   | bit2      | bit1 | bit0 |
|---------------|------|------|------|------|--------|-----------|------|------|
| Bit Name      | DCE  | DC   | ○    | ○    | SIGINV | SOUT[2:0] |      |      |
| Initial value | 0    | 0    | 0    | 0    | 0      | 0         | 0    | 0    |
| R/W           | R/W  | R/W  | R    | R    | R/W    | R/W       | R/W  | R/W  |

Bit 7: DCE

This bit enables/disables DC output from the SOUT pin.

1 (R/W): DC output is enabled.

0 (R/W): DC output is disabled (status flag output or Hi-Z state)

Bit 6: DC

This bit sets the DC level output from the SOUT pin when the DCE bit = 1.

1 (R/W): High level

0 (R/W): Low level

The two-bit combination of DCE and DC allows selection of an SOUT output status as shown in the table below.

**SOUT Output Selections**

| SOUTCTL.DCE | SOUTTCL.DC | SOUT pin out status                            |
|-------------|------------|--|
| 0b0         | 0b0        | Hi-Z   |
| 0b0         | 0b1        | According to SIGINV and SOUT[2:0] bit settings |
| 0b1         | 0b0        | Low output                                     |
| 0b1         | 0b1        | High output                                    |

Bit 3: SIGINV

This bit selects whether the output level is inverted or not when a status flag is output from the SOUT pin.

1 (R/W): Inverted output (When the flag = 1: Low level output; when the flag = 0: High level output)

0 (R/W): Non-inverted output (When the flag = 1: High level output; when the flag = 0: Low level output) The invert setting with this bit is ineffective when the DCE bit = 1.

Bits 2–0: SOUT[2:0]

These bits select the status flag to be output from the SOUT pin. This selection is effective only when the DCE bit = 0.

SOUT Output table Internal Status Flags

| SOUTCTL.SOUT[2:0] | Status flag  |
|-------------------|--|
| 0b000             | INTF.TF bit (Wakeup timer interrupt flag)                                |
| 0b001             | INTF.AF bit (Alarm interrupt flag)                                       |
| 0b010             | INFF.UF bit (Time update interrupt flag)                                 |
| 0b011             | INTF.EF bit (Event detection interrupt flag)                             |
| 0b100             | INTF.VTMPLF bit (Temperature compensation operation stop detection flag) |
| 0b101             | INTF.VLF bit (Invalid date and time data warning flag)                   |
| 0b110-0b111       | Reserved   |

## 8 SPI interface

### 8.1 Pin description

For Option D/E SPI interface pins

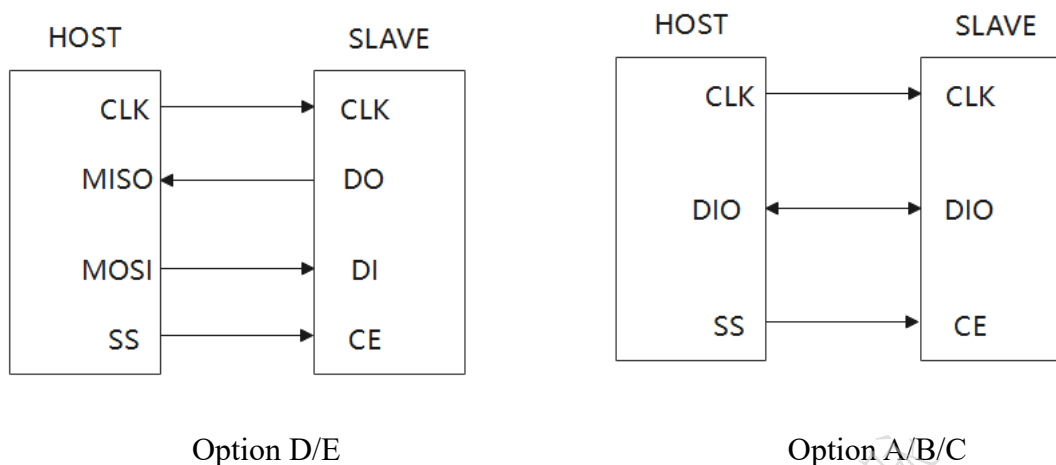
| PIN | Description                           |
|-----|---------------------------------------|
| DI  | SPI data in pin                       |
| DO  | SPI data out pin                      |
| CLK | SPI clock input pin                   |
| CE  | SPI slave select pin(300KΩ pull down) |

For Option A/B/C SPI interface pins



|     |                                       |
|-----|---------------------------------------|
| PIN | Description                           |
| DIO | SPI data in/out pin                   |
| CLK | SPI clock input pin                   |
| CE  | SPI slave select pin(300KΩ pull down) |

INS5A4000 is a slave driver. Below pictures show INS5A4000 connect to HOST.



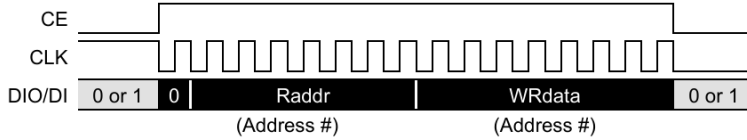
## 8.2 Write data

INS5A4000 is select as slave driver when the host sets the CE signal to high. Then it starts outputting a clock and an 8-bit address data (register address to which the first data is written) including a bit8 to specify write mode via DIO/DI, and write data follows in eight-bit units. Below shows the bit configuration of the address.

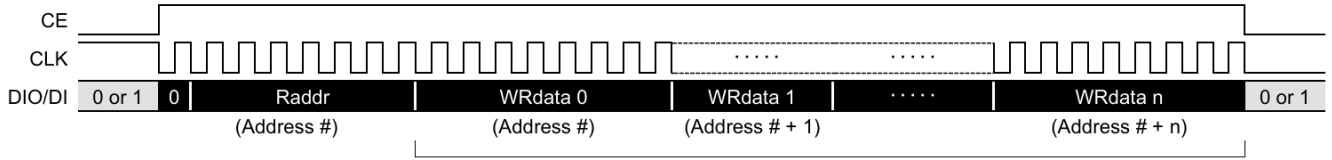
| BIT7                          | BIT6                                  | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|-------------------------------|---------------------------------------|------|------|------|------|------|------|
| 0: Write mode<br>1: Read mode | 7-bit address (0b000 0000–0b111 1111) |      |      |      |      |      |      |

Below shows INS5A4000 register data write operations. 1bit Write/Read mode + 7bits Address + 8bits Write Value +.....+ (7bits Address+1) + 8bits Write Value..... The low 4 bits of address will increase automatically from 0x0 to 0xF, then reset to 0x0. The high 3 bits of address don't increase automatically. Therefor to change the high 3 bits should restart CE signal, and change address.

Single register write operation



Continuous register write operation



The register address is incremented by writing data to a register.

### 8.3 Read data

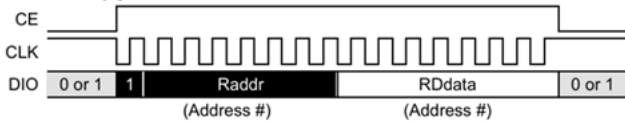
In this mode, INS5A4000 address bit8 should be set to 1.

| BIT7                          | BIT6                                  | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|-------------------------------|---------------------------------------|------|------|------|------|------|------|
| 0: Write mode<br>1: Read mode | 7-bit address (0b000 0000–0b111 1111) |      |      |      |      |      |      |

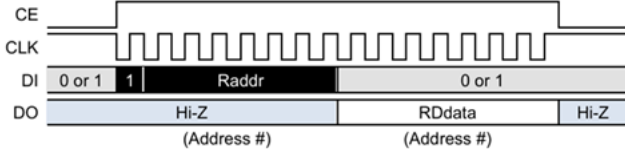
Below shows INS5A4000 register data read operations. The low 4 bits of address will increase automatically from 0x0 to 0xF, then reset to 0x0. The high 3 bits of address don't increase automatically. Therefore to change the high 3 bits should restart CE signal, and change address.

Single register read operation

INS5A4000 Option A/B/C

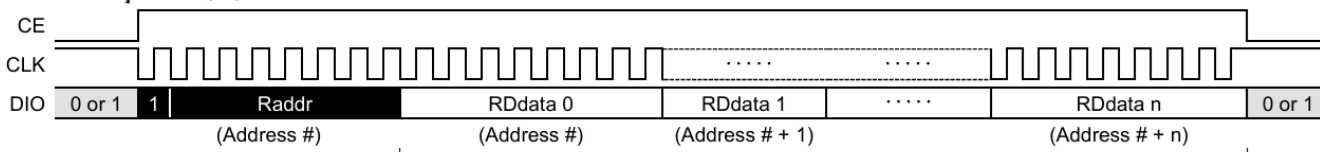


INS5A4000 Option D/E



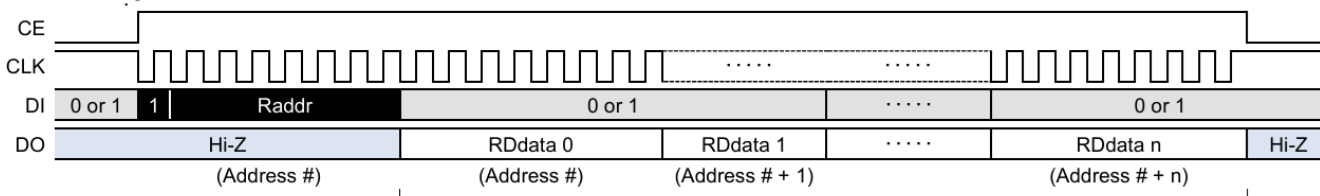
Continuous register read operation

INS5A4000 Option A/B/C



The register address is incremented by reading data from a register.

INS5A4000 Option D/E



The register address is incremented by reading data from a register.

## 9 Reflow Soldering Curve

Standard: IPC/JEDEC J-STD-020

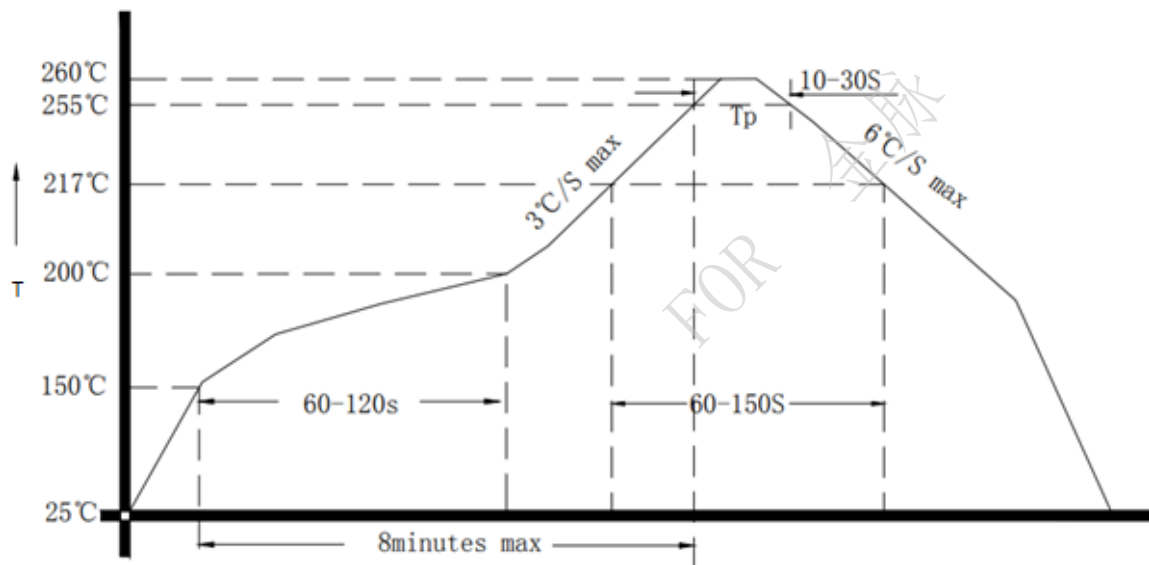


Figure 3. Reflow Soldering Curve

Note: It is suggested to solder IC under the condition shown in the curve above. Must pay attention to the temperature and time when manual soldering, if the temperature over +260°C, or you will make the xo performance bad, even damage it.

# 10 Dimensions

| Dimension/mm | Sym. | Min. | Typ. | Max. |
|--------------|------|------|------|------|
|              | A    | 3.0  | 3.2  | 3.4  |
|              | B    | 2.3  | 2.5  | 2.7  |
|              | C    | 0.9  | 1.0  | 1.1  |
|              | E    | -    | 0.3  | -    |
|              | F    | -    | 0.4  | -    |
|              | G    | -    | 0.6  | -    |
|              | H    | -    | 1.3  | -    |
|              | F1   | -    | 0.45 | -    |
|              | F2   | -    | 0.3  | -    |

| Soldering Pattern/mm | Sym. | Max. |
|----------------------|------|------|
|                      | A    | 0.9  |
|                      | B    | 1.1  |
|                      | C    | 0.4  |
|                      | D    | 0.3  |
|                      | E    | 0.7  |

● Marking

|  |             |          |                               |
|--|-------------|----------|-------------------------------|
|  | Frist Line  | 5A4000   | Part Num                      |
|  |             | X        | Option A/B/C/D/E              |
|  | Second Line | XXXXXXXX | Tracking codes and date codes |
|  | Third Line  | XXX      | Internal codes                |
|  | Fourth Line | ●        | Pin 1                         |

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# 11 Package

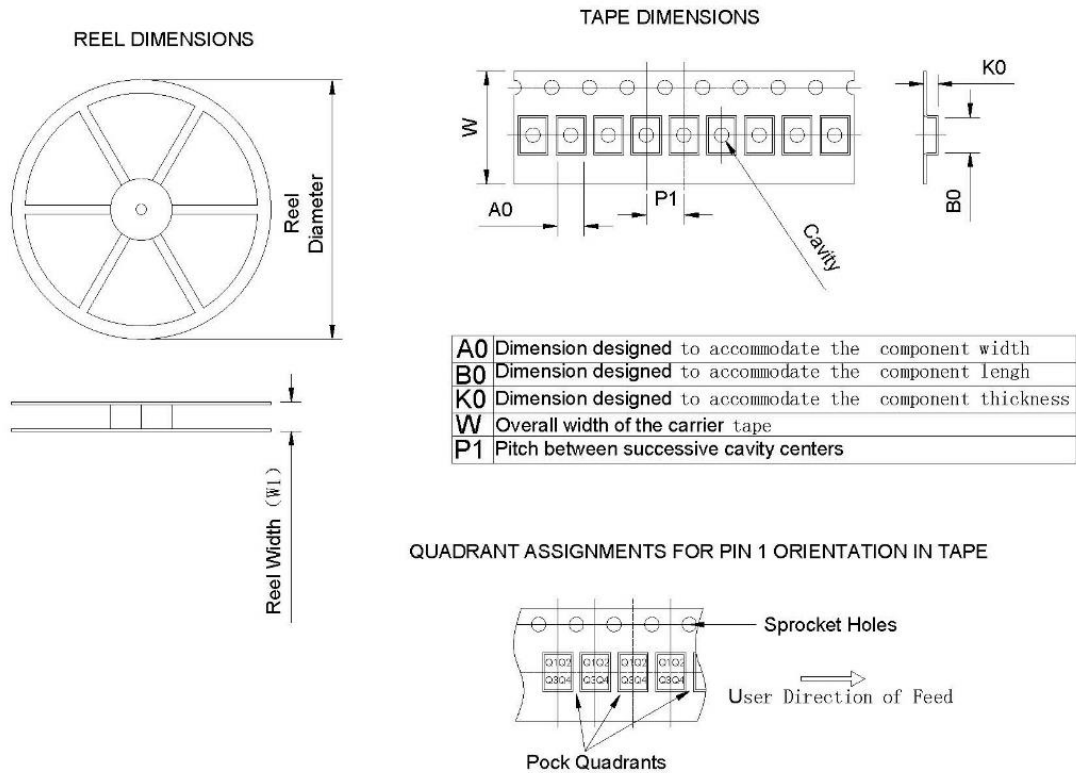


Figure 4. Package

| Device    | Package Type | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1(mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | PIN1 Quadrant |
|-----------|--------------|------|------|--------------------|-------------------|---------|---------|---------|---------|--------|---------------|
| INS5A4000 | LGA          | 10   | 3000 | 180                | 11.6±2.0          | 3.00    | 3.70    | 1.50    | 4       | 8.00   | Q1            |

## 12 Revision History

| Version | Change Contents | Prepared by | Revised Date |
|---------|-----------------|-------------|--------------|
| 1.0     | First Issued    |             | 2025.01.14   |
|         |                 |             |              |
|         |                 |             |              |
|         |                 |             |              |
|         |                 |             |              |

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