To Customer：

Realtime Clock Module

INS5T8111

Datasheet

Document Version 1.0

Released on June 20th, 2024

Ordering Information

Manufacture Part Number	Product Name	Description
INS5T8111CFY	INS5T8111	±23ppm @ 25℃, 250nA(Typ), Ceramic 3225
INS5T8111SFY	INS5T8111	±23ppm @ 25℃, 250nA(Typ), SMD 3225
INS5T8111CFZ	INS5T8111	±11.5ppm @ 25℃, 250nA(Typ), Ceramic 3225
INS5T8111SFZ	INS5T8111	±11.5ppm @ 25℃, 250nA(Typ), SMD 3225

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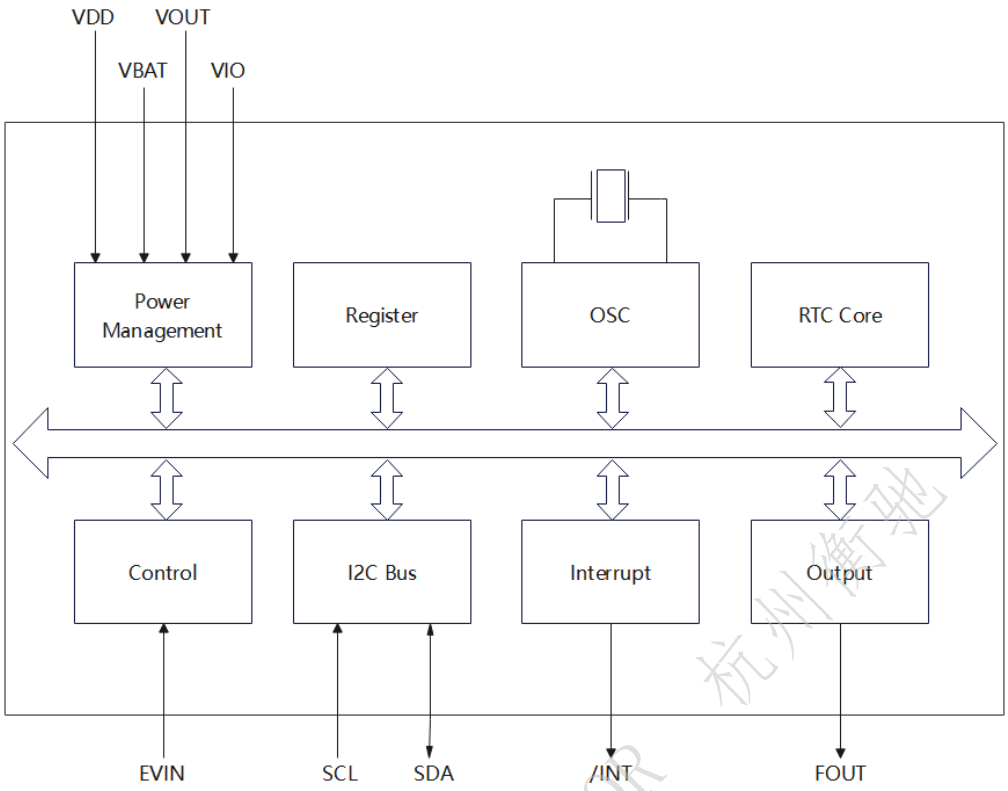
1 Overview

INS5T8111 is an ultra-low power consumption I2C bus interface real-time clock. It embeds a 32.768KHz Crystal. It supports calendar (year, month, day, hour, minute, second), clock and timer functions etc.

2 Block Diagram



3 Key Features

- Ultra-Low current consumption:250nA(Typ.)
- High stability:
  ±11.5ppm / ±23ppm @ 25℃
  -120ppm~10ppm @ -20℃~70℃, refer to 25℃
- Build-in Cystal: 32.768KHz
- Communication Interface: I2C bus
- RoHS2.0, REACH & Halogen-free compliant
- Power Supply Voltage: 1.6V~5.5V
- Time Keeping Voltage: 1.2V~5.5V
- Operation Temperature Range: -40℃~+85℃
- Leap years auto correction
- Backup battery switchover function
- Timer output function with adjustable period
- Size:3.2mm × 2.5mm × 0.9mm

4 Pin definition

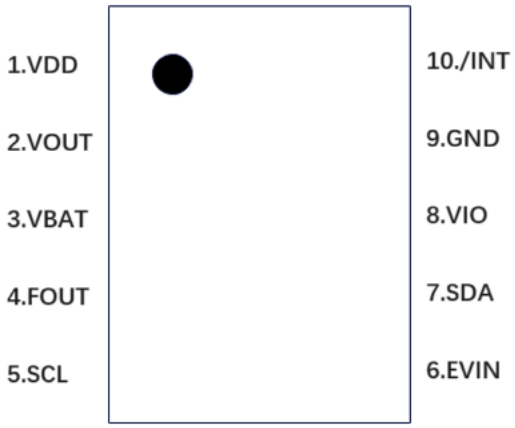
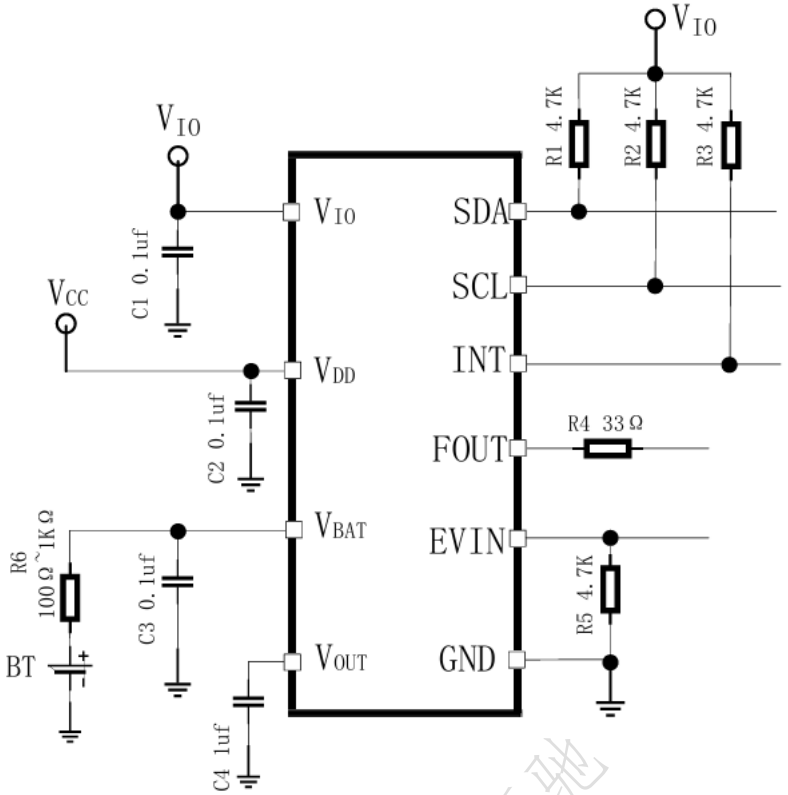
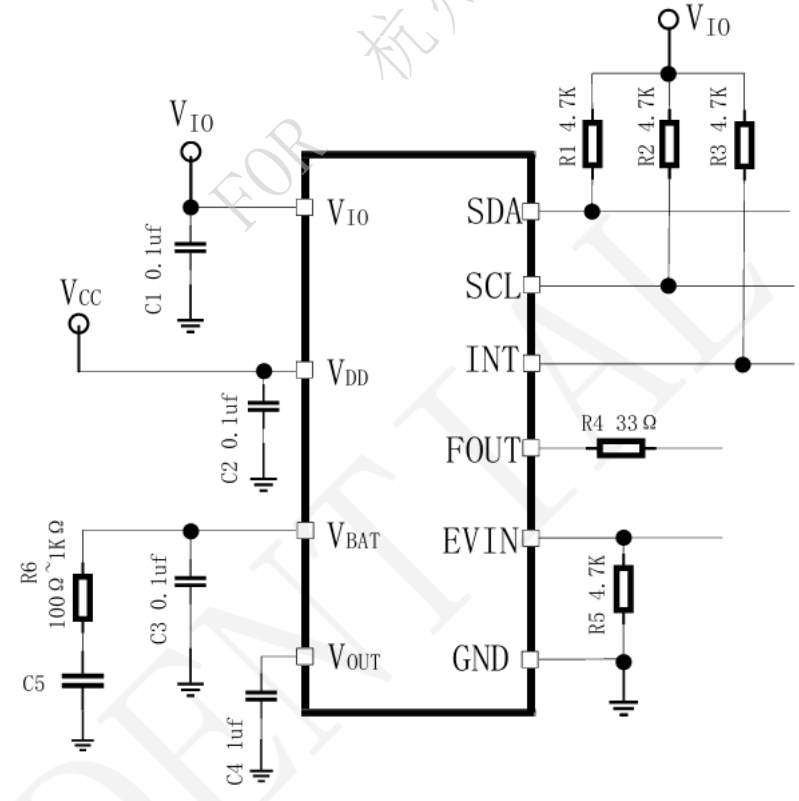
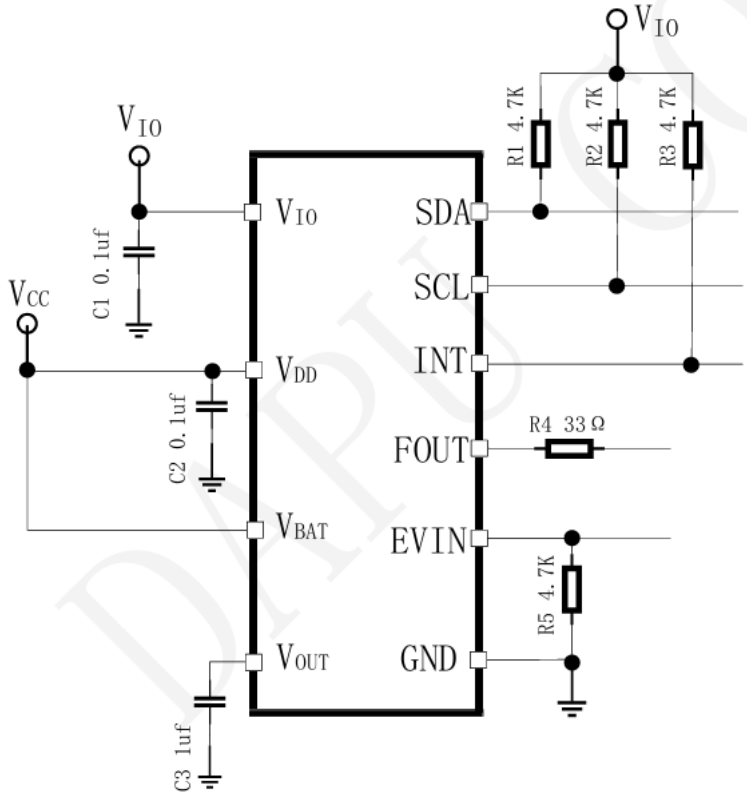


Table1. Pin Definition

Pin Number	Pin Name	I/O	Description
1	V_{DD}	-	Power supply
2	V_{OUT}		Internal voltage output pin. Connect bypass capacitor of 1.0 μF.
3	V_{BAT}	-	Backup battery pin. Connect to large-capacity capacitors or a backup battery. Connect to V_{DD} when switchover function is not necessary
4	FOUT	Out	Frequency output. Controlled by V_{IO}. Frequency can be set by FSEL bits.
5	SCL	In	I^2Cclock signal
6	EVIN	In	Trigger input terminal for time stamps.
7	SDA	In/Out	I^2C data signal
8	V_{IO}	-	Power supply for IO
9	GND	-	Ground
10	/INT	Out	Interrupt Output, Open-Drain

5 Typical application circuit diagram

VBAT with non-rechargeable battery, CHGEN = 0	
VBAT with rechargeable battery or large capacity, CHGEN = 1, INIEN=1	

Single Power supply mode	

Note:

1. Time of VDD from 0V to 2.5V < 50ms.
2. Recommend EVIN pin pull down to GND when not use EVIN function.
3. Remove R5 when using EVIN function.
4. The value of R & C is just for your reference, please adjust it according to your design.

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Table2. Absolute Maximum Ratings GND=0V

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage	Pwr	-0.3		6.5	V	V_{DD}/V_{BAT}/ V_{OUT} /V_{IO}
Input Voltage 1	V_{IN1}	-0.3		6.5	V	SCL/SDA
Input Voltage 2	V_{IN2}	-0.3		V_{OUT}+0.3	V	EVIN
Output Voltage 1	V_{OUT1}	-0.3		V_{IO}+0.3	V	FOUT

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Output Voltage 2	V_{OUT2}	-0.3		6.5	V	SDA, /INT
Storage temperature	T_{STG}	-55		125	℃	

6.2 Recommended Operating Conditions

Table3. Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage (Start Up)	V_{DD}	2.5	3.0	5.5	V	See Note 1
Power Supply Voltage (Operating)	V_{BAT} / V_{DD}	1.2	3.0	5.5	V	
Clock supply voltage	V_{CLK}	V_{DET}	3.0	5.5	V	
Interface Supply Voltage	V_{IO}	1.6	3.0	5.5	V	V_{DD}=1.6 ~ 5.5V
Current consumption	I_{DD}		0.25		uA	Using Battery supply only, @25℃
Operation temperature	T_{OPR}	-40	25	125	℃	

Note:

1. During the power on and oscillation starting time, a voltage of more than 2.5V must be provided to ensure the oscillation circuit to a stable state.
2. After the power supply is removed or power off, ensure that VDD=GND for more than 10 seconds before next power on cycle.
3. If there is no special indication, the test conditions are GND =0V, VDD=1.6V~5.5V, Ta=-40°C~+85°C

6.3 Frequency Characteristics

Table4. Frequency Characteristics

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Oscillation Frequency	fo		32.768		kHz	
Frequency stability	Δf/f	-23	0	+23	ppm	@+25°C, VDD=3.0V INS5T8111CFY INS5T8111SFY
		-11.5	0	+11.5		@+25°C, VDD=3.0V INS5T8111CFZ INS5T8111SFZ
Frequency Temperature Characteristics	fo-Tc	-120		+10	ppm	@-20°C~+70°C, +25°Creference
Oscillation start time	t_{STA}			1	s	@+25°C, V_{DD}=2.5~5.5V
Year Aging	f_a	-5		+5	ppm	@+25°C, V_{DD}=3.0V, First year

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
FOUT duty cycle	$t_{w/t}$	40	50	60	%	

Note：If there is no special indication, the test conditions are GND = 0V, V_{DD} = V_{BAT}= 1.6V ~ 5.5V, Ta =-40℃~+85℃

6.4 DC Characteristics

Table5. DC Characteristics

Parameter	Symbol	Value			Unit	Notes	
		Min.	Typ.	Max.			
Average Current consumption1	I_{DD1}		0.25	1.4	uA	SCL = SDA = High, FOUT = OFF, /INT = OFF, VDD = VOUT = VBAT = 3.0V, VIO = 3.0 V, -40 °C ~ +85 °C, CHGEN = 0b, INIEN = 0b	
Average Current consumption2	I_{DD2}		3.5	7	uA	SCL = SDA = High, FOUT = 32.768 kHz, /INT = OFF, VDD = VIO = 3.0V, -40 °C ~ +85 °C, FOUT pin CL = 15pF, CHGEN = 0b, INIEN = 1b	
Average Current consumption3	I_{BAT}		0.25	1.4	uA	SCL = SDA = Low, FOUT = OFF, /INT = OFF, VBAT = 3.0V, VDD = VIO = 0	
Detection voltage of VDD rise up	$+V_{DET1}$	1.4	1.65	1.9	V	Switch voltage of V_{DD} from V_{BAT}	
Detection voltage of VDD fall down	$-V_{DET1}$	1.35	1.6	1.85	V	Switch voltage of V_{BAT} from V_{DD}	
Detection voltage of V_{BAT} Low	V_{LOW}	1.0	1.2	1.4	V	V_{BAT} low detection voltage	
VOUT voltage 1	V_{VOUT1}		V_{DD}-0.12		V	V_{DD}=3.0V, I_{OUT}=1mA	
VOUT voltage 2	V_{VOUT2}		V_{BAT}-0.04		V	V_{BAT}=3.0V, I_{OUT}=0.1mA	
High-level input voltage	V_{IH}	0.8*V_{IO}		5.5	V	SCL, SDA	
		0.8*V_{OUT}		V_{OUT} +0.3	V	EVIN	
Low-level input voltage	V_{IL}	GND-0.3		0.2*V_{IO}	V	SCL, SDA	
		GND-0.3		0.2*V_{OUT}	V	EVIN	
High-level output voltage	V_{OH1}	4.5		5.5	V	V_{IO}=5.5V, I_{OH} = -1mA	FOUT
	V_{OH2}	2.2		3.0		V_{IO} =3.0V, I_{OH} = -1mA	
	V_{OH3}	2.9		3.0		V_{IO} =3.0V, I_{OH} = -100uA	
Low-level output voltage	V_{OL1}	GND		GND+0.5	V	V_{IO} =5.5V, I_{OL} = 1mA	FOUT
	V_{OL2}	GND		GND+0.8		V_{IO} =3.0V, I_{OL} = 1mA	
	V_{OL3}	GND		GND+0.1		V_{IO} =3.0V, I_{OL} = 100uA	
	V_{OL4}	GND		GND+0.25	V	V_{OUT}=5.5V, I_{OL} = 1mA	/INT
	V_{OL5}	GND		GND+0.4		V_{OUT} =3.0V, I_{OL} = 1mA	
	V_{OL6}	GND		GND+0.4	V	V_{IO}≥2.0V, I_{OL} = 3mA	SDA

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Input leakage current	I_{LK1}	-0.5		0.5	uA	SDA, SCL, $V_{IN} = V_{IO}$ or GND
	I_{LK2}	-0.5		0.5	uA	EVIN, V_{IN}=GND
Output leakage current 1	I_{OZ1}	-0.5		0.5	uA	FOUT, SDA, $V_{OUT} = V_{IO}$ or GND
Output leakage current 2	I_{OZ2}	-0.5		0.5	uA	/INT, $V_{OUT} = V_{OUT}$ or GND
V_{BAT} from V_{DD} Off leak current	I_{SW1}			50	nA	V_{BAT}=5.5, V_{DD}=0V
V_{OUT} from V_{BAT} Off leak current	I_{SW2}			50	nA	V_{BAT}=5.5, V_{OUT}=0V
V_{DD} from V_{BAT} Off leak current	I_{SW23}			50	nA	V_{BAT}=5.5, V_{OUT}=3V
SW ON current of V_{OUT} from V_{DD}	I_{SWON1}	1		10	mA	SW ON of V_{DD} and V_{OUT} ΔV =＋0.1V, V_{OUT} = 5.5V, V_{DD} = 5.4V, ΔV =＋0.1V, VOUT = 3.0V, VDD = 2.9V, R_{SWON1} = 20 Ω ~ 200 Ω
SW ON current of V_{OUT} from V_{BAT}	I_{SWON2}	0.5		6	mA	SW ON of VBAT and VOUT ΔV = ＋0.1 V, VOUT = 5.5 V, VBAT = 5.4 V ΔV = ＋0.1V, VOUT = 3.0 V, VBAT = 2.9 V RSWON1 = 33 Ω ~ 400 Ω

Note: If there is no special indication, the test conditions are GND=0V, VDD=1.6V~5.5V, Ta=-40°C~+85°C.

6.5 AC Characteristics

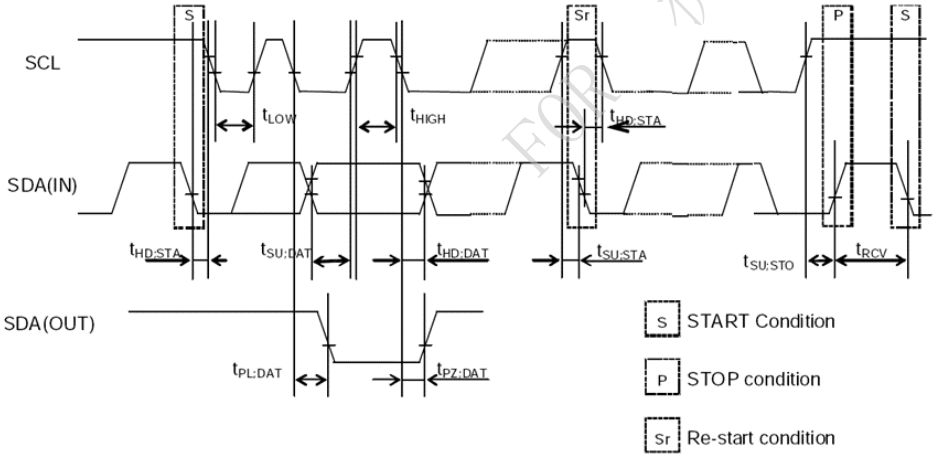


Figure 1. I^2C bus Timing Chart

Table6. AC Characteristics

V_{DD}=2.5V~5.5V;Ta=-40℃~+85℃

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}			400	kHz

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
SCL low level time	t_{LOW}	1.3			us
SCL high level time	t_{HIGH}	0.6			us
Start condition setup time	$t_{HD;STA}$	0.6			us
Start condition hold time	$t_{SU;STA}$	0.6			us
Stop condition setup time	$t_{SU;STO}$	0.6			us
Bus idle time between start condition and stop condition	t_{RCV}	1.3			us
Data setup time	$t_{SU;DAT}$	100			ns
Data hold time	$t_{HD;DAT}$	0			ns
SCL, SDA rising time	t_r			0.3	us
SCL, SDA falling time	t_f			0.3	us

Note: when the master accesses the equipment through I2C bus, all communication from sending start condition to sending stop shall be completed within 1 second. If it exceeds 1 second, the I2C bus interface will be reset through the internal bus timeout function.

7 Registers

7.1 Register Lists

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W	Default Value
0x10	SEC	○	40	20	10	8	4	2	1	R/W	0x00
0x11	MIN	○	40	20	10	8	4	2	1	R/W	0x00
0x12	HOUR	○	○	20	10	8	4	2	1	R/W	0x00
0x13	WEEK	○	6	5	4	3	2	1	0	R/W	0x40
0x14	DAY	○	○	20	10	8	4	2	1	R/W	0x01
0x15	MONTH	○	○	○	10	8	4	2	1	R/W	0x01
0x16	YEAR	80	40	20	10	8	4	2	1	R/W	0x00
0x17	MIN Alarm	AE	40	20	10	8	4	2	1	R/W	0x00
0x18	HOUR Alarm	AE	●	20	10	8	4	2	1	R/W	0x00
0x19	WEEK Alarm	AE	6	5	4	3	2	1	0	R/W	0x00

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W	Default Value
	DAY Alarm	AE	●	20	10	8	4	2	1	R/W	0x00
0x1A	Timer Counter 0	128	64	32	16	8	4	2	1	R/W	0x00
0x1B	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256	R/W	0x00
0x1C	Timer Counter 2	8388608	4194304	2097152	1048576	524288	262144	131072	65536	R/W	0x00
0x1D	Extension Register	FSEL1	FSEL0	USEL	TE	WADA	ETS	TSEL [1]	TSEL [0]	R/W	0x02
0x1E	Flag Register	POR	○	UF	TF	AF	EVF	VLF	XST	R/W	0x80
0x1F	Control Register	○	○	UIE	TIE	AIE	EIE	○	STOP	R/W	0x00
0x20	time stamp 1/1024s	○	○	○	○	○	○	1/512	1/1024	R	0x00
0x21	time stamp 1/256s	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256	R	0x00
0x22	time stamp sec	○	40	20	10	8	4	2	1	R	0x00
0x23	time stamp min	○	40	20	10	8	4	2	1	R	0x00
0x24	time stamp hour	○	○	20	10	8	4	2	1	R	0x00
0x25	time stamp week	○	6	5	4	3	2	1	0	R	0x00
0x26	time stamp day	○	○	20	10	8	4	2	1	R	0x00
0x27	time stamp month	○	○	○	10	8	4	2	1	R	0x00
0x28	time stamp year	80	40	20	10	8	4	2	1	R	0x00
0x29	status stamp	○	○	VLOW	VCMP	VDET	○	XST	○	R	0x00

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W	Default Value
0x2A	RSV	Reserved								R/W	0x23
0x2B	EVIN setting	EHL	ET1	ET0	PDN	PU1	PU0	OVW	○	R/W	0x00
0x2C	sec alarm	AE	40	20	10	8	4	2	1	R/W	0x00
0x2D	timer control	○	○	○	○	TBKON	TBKE	TMPIN	TSTP	R/W	0x00
0x2E	timestamp ctrl	○	○	○	○	○	○	○	COMTG	R/W	0x00
0x2F	Command trigger	○	○	○	○	○	○	○	○	R/W	0x00

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W	Default value
0x30	No Function	○	○	○	○	○	○	○	○	R	0x00
0x31	No Function	○	○	○	○	○	○	○	○	R	0x00
0x32	power switch ctrl	CHGEN	INIEN	○	○	SWSEL[1:0]		SMPT[1:0]		R/W	0x48
0x33	evin monitor	Reserved	EVIN	○	○	VCMP	○	VLOW	Reserved	R	0x00
0x34	time stamp control1	○	○	○	○	○	EISEL	TSCEL	TSRAM	R/W	0x00
0x35	time stamp control2	●	○	○	○	ECMP	EVDET	EVLOW	EXST	R/W	0x00
0x36	time stamp contro3	○	○	○	TSFULL	TSEMP	TSAD[2:0]			R	0x0F
0x37	RAM	○	○	○	●	○	○	○	●	R/W	0x00
0x38	RSV	○	Reserved							R/W	0x00
0x39	RSV	○	○	○	○	○	○	Reserved		R/W	0x00
0x3a	RSV	○	○	○	○	○	○	○	Reserved	R/W	0x01

0x3b	No Function	○	○	○	○	○	○	○	○	R	0x00
0x3c	No Function	○	○	○	○	○	○	○	○	R	0x00
0x3d	No Function	○	○	○	○	○	○	○	○	R	0x00
0x3e	No Function	○	○	○	○	○	○	○	○	R	0x00
0x3f	TEST	TEST	○	○	○	○	○	○	○	R/W	0x00

Address Hex	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W	Default value
40,50,60,70	Time stamp 1/256s	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256	R/W	0x00
41,51,61,71	Time stamp SEC	●	40	20	10	8	4	2	1	R/W	0x00
42,52,62,72	Time stamp MIN	●	40	20	10	8	4	2	1	R/W	0x00
43,53,63,73	Time stamp HOUR	●	●	20	10	8	4	2	1	R/W	0x00
44,54,64,74	Time stamp DAY	●	●	20	10	8	4	2	1	R/W	0x00
45,55,65,75	Time stamp MONTH	●	●	●	10	8	4	2	1	R/W	0x00
46,56,66,76	Time stamp YEAR	80	40	20	10	8	4	2	1	R/W	0x00
47,57,67,77	Status stamp	●	●	VLOW	VC MP	VDET	●	XST	●	R/W	0x00
48,58,68,78	Time stamp 1/256s Function	1	2	4	8	16	32	64	128	R/W	0x00
49,59,69,79	Time stamp SEC	●	40	20	10	8	4	2	1	R/W	0x00
4A,5A,6A,7A	Time stamp MIN	●	40	20	10	8	4	2	1	R/W	0x00
4B,5B,6B,7B	Time stamp HOUR	●	●	20	10	8	4	2	1	R/W	0x00

4C,5C,6C,7C	Time stamp DAY	●	●	20	10	8	4	2	1	R/W	0x00
4D,5D,6D,7D	Time stamp MONTH	●	●	●	10	8	4	2	1	R/W	0x00
4E,5E,6E,7E	Time stamp YEAR	80	40	20	10	8	4	2	1	R/W	0x00
4F,5F,6F,7F	Status stamp	●	●	VLOW	VCMP	VDET	●	XST	●	R/W	0x00

Note:

1. The bits marked with "○" can be read out "0" only after initializing.
2. The bits marked with "●" are RAM bits which can be used to write or read any data.
3. Make sure "0" to be written for TEST bits which are used for testing only.
4. Reserved bit should not write, and it's value is unknow.

7.2 Details of Registers

7.2.1 Clock counter registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x10	SEC	○	40	20	10	8	4	2	1	R/W
0x11	MIN	○	40	20	10	8	4	2	1	R/W
0x12	HOUR	○	○	20	10	8	4	2	1	R/W
0x13	WEEK	○	6	5	4	3	2	1	0	R/W
0x14	DAY	○	○	20	10	8	4	2	1	R/W
0x15	MONTH	○	○	○	10	8	4	2	1	R/W
0x16	YEAR	80	40	20	10	8	4	2	1	R/W
0x1F	Control Register	○	○	UIE	TIE	AIE	EIE	○	STOP	R/W

SEC: BCD format, Value: 0~59

MIN: BCD format, Value: 0~59

HOUR: BCD format, Value: 0~23

WEEK: Value 01h, 02h, 04h, 08h, 10h, 20h, 40h. Only one bit can be set to 1 each time, all others must be set to 0.

Table7. WEEK Register

WEEK	Data	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sunday	01h	0	0	0	0	0	0	0	1
Monday	02h	0	0	0	0	0	0	1	0
Tuesday	04h	0	0	0	0	0	1	0	0
Wednesday	08h	0	0	0	0	1	0	0	0
Thursday	10h	0	0	0	1	0	0	0	0
Friday	20h	0	0	1	0	0	0	0	0
Saturday	40h	0	1	0	0	0	0	0	0

DAY: BCD format, the value range will be adjusted automatically according to the month setting and if a leap year or not .

Table8. DAY Register Value

Month	Day Value Range
1, 3, 5, 7, 8, 10, 12	1~31
4, 6, 9, 11	1~30
February in normal year	1~28
February in leap year	1~29

MONTH: BCD format, Value1~12

YEAR: BCD format, Value0~99(2000~2099)

STOP: Stop calendar from 1/256s to year, and stop timer source clock of “64Hz / 1Hz / 1/60Hz”. When STOP=”1”, 32768Hz and 1024Hz output is possible, but 1Hz output is disabled.

Example: 2020/01/01 Wednesday 21:18:36

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x10	SEC	○	0	1	1	0	1	1	0
0x11	MIN	○	0	0	1	1	0	0	0
0x12	HOUR	○	○	1	0	0	0	0	1
0x13	WEEK	○	0	0	0	1	0	0	0
0x14	DAY	○	○	0	0	0	0	0	1

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x15	MONTH	○	○	○	0	0	0	0	1
0x16	YEAR	0	0	1	0	0	0	0	0

7.2.2 Alarm Interrupt Function

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x17	MIN Alarm	**AE**	**40**	**20**	**10**	**8**	**4**	**2**	**1**	R/W
0x18	HOUR Alarm	**AE**	●	**20**	**10**	**8**	**4**	**2**	**1**	R/W
0x19	WEEK Alarm	**AE**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	R/W
	DAY Alarm	**AE**	●	**20**	**10**	**8**	**4**	**2**	**1**	R/W
0x1D	Extension Register	FSEL1	FSEL0	USEL	TE	**WADA**	ETS	TSEL [1]	TSEL [0]	R/W
0x1E	Flag Register	POR	○	UF	TF	**AF**	EVF	VLF	XST	R/W
0x1F	Control Register	○	○	UIE	TIE	**AIE**	EIE	○	STOP	R/W
0x2C	SEC Alarm	**AE**	**40**	**20**	**10**	**8**	**4**	**2**	**1**	R/W

1) WADA bit (Week Alarm / Day Alarm Select)

The alarm interrupt function uses either "Day" or "Week" as its target. The WADA bit is used to specify either WEEK or DAY as the target for alarm interrupt events.

WADA	Value	Description
Write / Read	0	Set WEEK as target of alarm function
	1	Set DAY as target of alarm function

2) AF (Alarm Flag)

Alarm Flag bit. When an alarm interrupt event occurs, it will be set to “1” and keeps “1” until a “0” is written to it.

AF	Value	Description
Write	0	Clearing this bit to 0 enables /INTS low output to be canceled when an alarm interrupt event has occurred.
	1	Invalid
Read	0	-
	1	Alarm interrupt events are detected. (Result is retained until this bit is cleared to zero)

3) AIE Bit (Alarm Interrupt Enable)

Alarm Interrupt Enable bit: When AF changes from "0" to "1", this bit controls if an interrupt signal is generated. 0-disenable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).

AIE	Value	Description
Write	0	1) When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status remains Hi-Z). 2) When an alarm interrupt event occurs, the interrupt signal is canceled (/INT status changes from low to Hi-Z).
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low).

4) Example of alarm settings

✧ Example of alarm settings when "WEEK" has been specified (WADA=0)

	BIT7 AE	BIT6 Saturday	BIT5 Friday	BIT4 Thursday	BIT3 Wednesday	BIT2 Tuesday	BIT1 Monday	BIT0 Sunday	HOUR Alarm	MIN Alarm	SEC Alarm
Monday to Friday, at 6:00 AM 1 minute alarm	0	0	1	1	1	1	1	0	0x06	0x00	0x80
Every Monday, for 30 minutes each hour, Hour value is ignored	0	0	0	0	0	0	1	0	0x80	0x30	0x00
Every day, at 7:20:15 PM	0	1	1	1	1	1	1	1	0x19	0x20	0x15

✧ Example of alarm settings when "DAY" has been specified (WADA=1)

	BIT7 AE	BIT6	BIT5 20	BIT4 10	BIT3 08	BIT2 04	BIT1 02	BIT0 01	HOUR Alarm	MIN Alarm	SEC Alarm
5th of each month, at 8:00 AM 1 minute alarm. Second value is ignored	1	0	0	0	0	1	0	1	0x08	0x00	0x80
15th of each month, for 30 minute each month. Hour value is ignored.	1	0	0	1	0	1	0	1	0x80	0x30	0x00
Every day, at 7:20:15 PM	1	X	X	X	X	X	X	X	0x19	0x20	0x15

7.2.3 Wake-up Timer Interrupt Function

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x1A	Timer Counter 0	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**	R/W

0x1B	Timer Counter 1	**32768**	**16384**	**8192**	**4096**	**2048**	**1024**	**512**	**256**	R/W
0x1C	Timer Counter 2	**8388608**	**4194304**	**2097152**	**1048576**	**524288**	**262144**	**131072**	**65536**	R/W
0x1D	Extension Register	FSEL1	FSEL0	USEL	**TE**	WADA	ETS	**TSEL[1]**	**TSEL[0]**	R/W
0x1E	Flag Register	POR	○	UF	**TF**	AF	EVF	VLF	XST	R/W
0x1F	Control Register	○	○	UIE	**TIE**	AIE	EIE	○	STOP	R/W
0x2D	timer control	○	○	○	○	**TBKON**	**TBKE**	**TMPIN**	**TSTP**	R/W

1) Timer counter 2, 1, 0

Preset values of timer counter. Any value from 1(0x000001h) to 16777216 (0xFFFFFFh) can be set. Please ensure TE & TIE write "0" before writing timer counter

2) TE

This bit is use to control timer start / stop

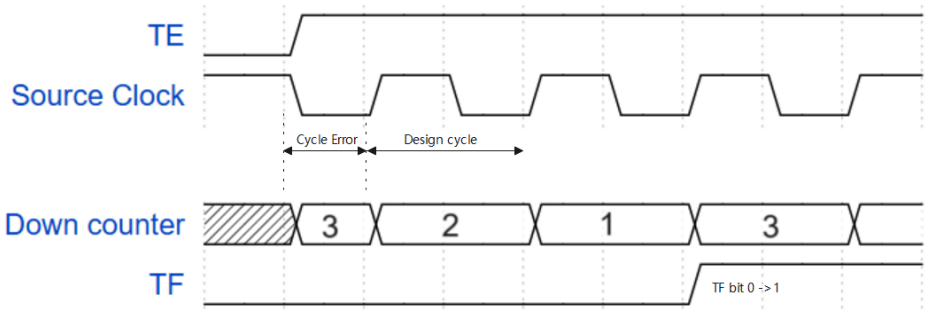
TE	Data	Description
Write/ Read	0	Timer is stop.
	1	Timer is start.

3) TSEL[1], TSEL[0]

This bits be used to set the source clock of timer count down period.

TESL[1]	TSEL[0]	Source Clock	Auto Reset Time(tRTN)
0	0	4096 Hz, once per 244.14us	122us
0	1	64 Hz, once per 15.625ms	7.813ms
1	0	1 Hz, once per 1 second	7.813ms
1	1	1/60 Hz, once per minute	7.813ms

Below shows an error of first countdown: Timer counter value is 3h



Timer initialization cycle error

4) TF

Timer Flag bit. When a fixed-cycle timer interrupt event occurs, it will be set to "1" and keeps "1" until a "0" is written to it.

TF	Data	Description
Write	0	The TF bit is cleared to 0 to prepare for the next status detection. Clearing this bit to 0 is not enable the /INT low output status to Hi-Z.
	1	Invalid
Read	0	
	1	Wake-up timer interrupt events are detected. This bit will keep “1” until software to write “0”.

5) TIE

Timer Interrupt Enable bit: When TF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disenable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).

TIE	Value	Description
Write	0	1.When a wake-up timer interrupt event occurs, an interrupt signal is not generated. When a wake-up timer interrupt event occurs, the interrupt signal is canceled. (/INT status change from low to Hi-Z).
	1	When a wake-up timer interrupt event occurs, an interrupt signal is generated. (/INT status changes from Hi-Z to low)

6) TBKON, TBKE (Timer Backup ON, Timer Backup/normal Enable)

This bit set operation timer with the main power supply or the backup power supply.

	TBKE	TBKON	Description
Write/Read	0	X	This setting counts at normal mode and backup mode.
	1	0	This setting counts at normal mode (V_{DD} Operation).
	1	1	This setting counts at backup mode (V_{BAT} Operation).

7) TMPIN

This timer interrupt output can be assigned to FOUT pin.

To output only the interrupt on FOUT pin, set the FOUT output setting to FSEL[1:0] = 11b, FOUT is stopped.

TMPIN	Value	Description
Write	0	Timer interruption is output from /INT pin. (Open Drain)
	1	Timer interruption is output from FOUT pin. (CMOS)

8) TSTP (Timer Stop)

This bit is used to stop wake-up timer count down.

TE	STOP	TBKE	TSTP	Description
1	ble9. 0	0	0	Write a “0”, it will cancels stop status (restart timer counts down).
			1	Write a “1”, it will stop timer counts down.
		1	X	Write a “1” is invalid. Timer count does not stop even if set TSTP=”1”
	1	X	X	The count stops at the timer of the setting of 64Hz, 1Hz, 1/60Hz
0	X	X	X	It doesn’t start counting.

7.2.4 Time Update Interrupt Function

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x1D	Extension Register	FSEL1	FSEL0	**USEL**	TE	WADA	ETS	TSEL [1]	TSEL [0]	R/W
0x1E	Flag	POR	○	**UF**	TF	AF	EVF	VLF	XST	R/W

	Register									
0x1F	Control Register	○	○	**UIE**	TIE	AIE	EIE	○	STOP	R/W

Before entering settings for operations, it is recommended writing a "0" to the UIE bit.
When the STOP bit value is "1" time update interrupt events do not occur.
Time update interrupt function cannot be inactive. User can set /INT output inactive by UIE=”0” to prevented from changing the /INT pin status to low.

1) USEL (Update Selection)
This bit is used to select "second" update or "minute" update as the timing for generation of time update interrupt events.

USEL	Value	Description
Write / Read	0	Selects “Second update” (once per second) as the timing for generation of interrupt events.
	1	Selects “Minute update” (once per minute) as the timing for generation of interrupt events.

2) UF (Update Flag)
This flag bit value changes from "0" to "1" when a time update interrupt event occurs.

UF	Value	Description
Write	0	Clearing this bit to zero enables /INT low output to be canceled (/INT remains Hi-Z) when a time update interrupt event has occurred.
	1	Invalid
Read	0	-
	1	Time update interrupt events are detection. Keeping “1” until software to write “0”.

3) UIE (Update Interrupt Enable)
This bit selects whether to generate an interrupt signal or not generate it.

TIE	Value	Description
Write / Read	0	Does not output an interrupt signal when a time update interrupt event occurs.
	1	Time update interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low).

7.2.5 Self-Monitor Detection

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x1E	Flag Register	**POR**	○	UF	TF	AF	EVF	**VLF**	**XST**	R/W
0x33	Evin Monitor	Reserved	**EVIN**	○	○	**VCMP**	○	**VLOW**	Reserved	R

Self-Monitor is a function of detecting RTC status and holding the result.

1) POR bit (Power On Reset)

This bit detect power on reset operation.

POR	Value	Description
Write	0	Clear flag and waiting for the next power on reset detection.
	1	Invalid.
Read	0	No power on reset detection.
	1	Power on reset is detected. Keeping the result until software write “0”. All registers are set into default when power on reset.

2) VLF (Voltage Low Flag)

This bit is use to detect the status of VOUT low voltage.

VLF	Value	Description
Write	0	Clear flag and waiting for the next low voltage detection.
	1	Invalid.
Read	0	No low voltage detection.
	1	VOUT low voltage is detected. Keeping the result until software write “0”. The RTC is working abnormally. Unser can check the RTC status and initialize by software.

3) XST (X’tal Oscillation Stop)

This bit is use to detect the status of internal X’tal stopping.

XST	Value	Description
Write	0	Clear flag and waiting for the next internal X’tal stopping detection.
	1	Invalid.
Read	0	No internal X’tal stopping detection.
	1	Internal X’tal stopping is detected. Keeping the result until software write “0”.

4) EVIN bit (Input level monitor of EVIN terminal)

This bit is use to monitor EVIN terminal input voltage.

EVIN	Value	Description
Read	0	EVIN terminal input voltage is LOW.
	1	EVIN terminal input voltage is HIGH.

5) VCMP bit

This bit is use to monitor the status of the comparison between VDD and VBAT during battery is being recharged.

VCMP	Value	Description
Read	0	VBAT < VDD
	1	VBAT > VDD, Recharging suspended.

6) VLOW bit

This bit is use to monitor the result of VLOW.

VLOW	Value	Description
Read	0	VBAT > VLOW
	1	VBAT < VLOW

7.2.6 Clock Output Function

This function can output a Configurable signal.

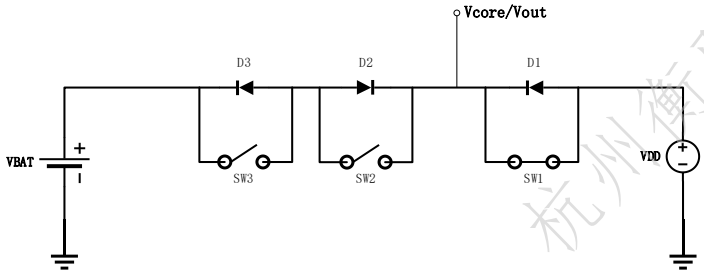
Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x1D	Extension Register	**FSEL1**	**FSEL0**	USEL	TE	WADA	ETS	TSEL[1]	TSEL[0]	R/W

When FOUT function is needed, TMPIN should be set to “0”.

FSEL0	FSEL1	Output
0	0	32768Hz
0	1	1024Hz
1	0	1Hz
1	1	OFF

Note: When STOP = “1”, 32768Hz & 1024Hz is possible, but 1Hz is disabled.

7.2.7 Battery backup switchover function



Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x32	power switch ctrl	CHGEN	INIEN	○	○	SWSEL[1:0]		SMPT[1:0]		R/W

1) CHGEN Bit (Charge Enable)

This bit is use to control entering recharging mode.

CHGEN	Value	Description
Write/Read	0	Recharge inactive
	1	Recharge active.

To set CHGEN active, user should set INIEN=”1”.

2) INIEN

This bit is use to control SW (Switch between VDD pin & VOUT pin, Switch between VBAT pin and VOUT pin)

When INIEN=”0”, VDD<VDET1, I2C is inactive.

INIEN	Value	Description
Write/Read	0	SW(SW1 / SW2 / SW3) are controlled by SWSEL[1:0].
	1	SW(SW1 / SW2 / SW3) are auto control.

3) SWSEL0, SWSEL1

This bit is use to control SW1 / SW2 / SW3.

INIEN	CHGEN	SWSEL1	SWSEL0	SW3	SW2	SW1
0	X	0	0	Close	Close	Open
0	X	0	1	Close	Open	Open
0	X	1	0	Open	Open	Close
0	X	1	1			
1	0	X	X	SW Auto control		
1	1	X	X	SW Auto control		

4) SMPT0, SMPT1

These two bits control SW1 OFF period and user can check much precision voltage by preventing reverse current from VBAT to VDD when main VDD shuts down.

VDD voltage low detection (VDET1) is active anytime, so lower voltage detection moves RTC into backup mode immediately regardless SW1 OFF time.

These SW1 OFF occur every second.

SMPT1	SMPT2	SW1 OFF period
0	0	Always ON
0	1	2ms
1	0	128ms
1	1	256ms

7.2.8 Time Stamp Function

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x1D	Extension Register	FSEL1	FSEL0	USEL	TE	WADA	**ETS**	TSEL [1]	TSEL [0]	R/W
0x1E	Flag Register	POR	○	UF	TF	AF	**EVF**	VLF	XST	R/W
0x1F	Control Register	○	○	UIE	TIE	AIE	**EIE**	○	STOP	R/W
0x2B	EVIN setting	**EHL**	**ET1**	**ET0**	**PDN**	**PU1**	**PU0**	**OVW**	○	R/W
0x2E	timestamp ctrl	○	○	○	○	○	○	○	**COMTG**	R/W
0x2F	Command trigger	○	○	○	○	○	○	○	○	R/W
0x34	time stamp control1	○	○	○	○	○	**EISEL**	**TSCEL**	**TSRAM**	R/W
0x35	time stamp	○	○	○	○	**ECMP**	**EVDET**	**EVLO**	**EXST**	R/W

	control2							**W**		
0x36	time stamp contro3	○	○	○	**TSFULL**	**TSEMP**	**TSAD[2:0]**			R/W

7.2.8.1 Time stamp function triggered by EVIN pin input

1) ETS Bit

This register controls time stamp (triggered by EVIN pin input) ON/OFF.

ETS	Value	Description
Write/Read	0	Time stamp function OFF
	1	Time stamp function ON

2) EVF Bit (Event Flag)

EVF	Value	Description
Write	0	Clear event flag, /INT set to Hi-Z
	1	Invalid
Read	0	-
	1	EVIN input is detected.

3) EIE Bit (Event Interrupt Enable)

This register control /INT interrupt output at the moment of the event (EVF, "0" → "1").

EIE	Value	Description
Write	0	1) No /INT interrupt output 2) Release /INT interrupt output
	1	Detect event interrupt

4) EHL Bit (Event High / Low)

This register controls EVIN input voltage level.

EHL	Value	Description
Write/Read	0	Treg by low level.
	1	Treg by high level.

5) ET0, ET1 Bits

These bits select chattering filter period of input from EVIN.

ET1	ET0	Description
0	0	No chattering filter.
0	1	3.9ms (256 Hz)
1	0	15.6ms (64 Hz)
1	1	25ms (8 Hz)

6) PDN, PU1, PU0 Bits

These registers controls EVIN pin input internal Pull-up/Pull-down resistor value. Pull-up resistor is connected to VOUT, Pull-down resistor to GND.

Condition	PDN	PU1	PU0	Resistor value
No connection	0	0	0	Hi-Z
Pull-up	0	0	1	500kΩ
	0	1	0	1MΩ
	0	1	1	1MΩ

Pull-down	1	0	0	500kΩ
No connection	1	1	0	Don't select these combinations, EVIN changed to Hi-Z
	1	0	1	
	1	1	1	

7) OVW Bit (Over Write)

OVW	Value	Description
Write/Read	0	Time stamp records 8 times, and no update. T0→T1→T2……T8.
	1	Time stamp records 8 times continuously. T0→T1→T2……T8→T0→T1→T2……T8……..

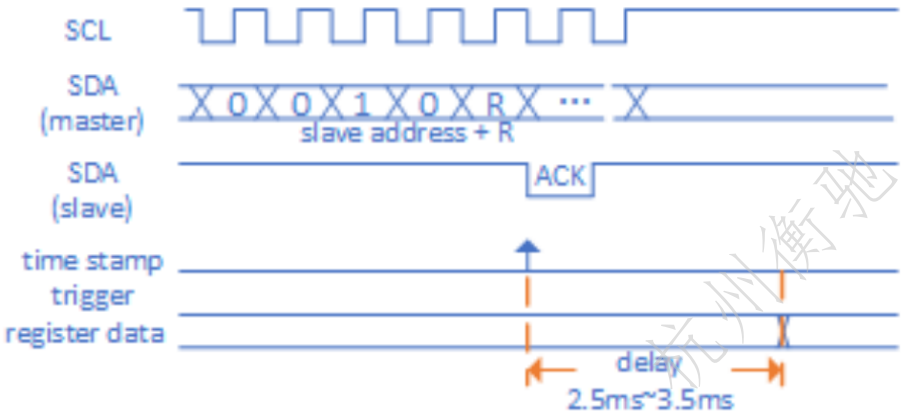
7.2.8.2 Time stamp function triggered by i2c access

This register control Time stamp trigger by I2C access ON/OFF.

1) COMTG Bit

COMTG	Value	Description
Write	0	Time stamp function triggered by i2c OFF.
	1	Time stamp function triggered by i2c ON.

Time stamp access timing Time stamp processing is done as below timing diagram:



7.2.8.3 Time stamp stored registers

Address	Function	Stored
0x20	Time stamp 1/1024s	256Hz, 512Hz
0x21	Time stamp 1/256s	1Hz~128Hz
0x22	Time stamp second	Second
0x23	Time stamp minutes	Minutes
0x24	Time stamp hour	Hour
0x25	Time stamp week	Week
0x26	Time stamp day	Day
0x27	Time stamp month	Month
0x28	Time stamp year	Year
0x29	Status stamps	RTC Internal status

7.2.8.4 Status Stamps Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x29	status stamp	○	○	VLOW	VCMP	VDET	○	XST	○	R

1) VLOW (Time Stamp VLOW)

This bit records the comparison result of VBAT vs VLOW at the moment of event.

VLOW	Value	Description
Read	0	VBAT > VLOW
	1	VBAT < VLOW

2) VCMP (Time Stamp VCMP)

This bit records the comparison result of VDD vs VBAT (VCMP status) at the moment of event.

VCMP	Value	Description
Read	0	VDD > VBAT
	1	VDD < VBAT

3) VDET (Time Stamp VDET)

This bit records the comparison result of VDD vs VDET1 at the moment of event.

VDET	Value	Description
Read	0	VDD > VDET1
	1	VDD < VDET1

4) XST (Time Stamp X'tal Oscillation Stop)

This bit records either internal Crystal oscillation stop or not stop at the moment of event.

XST	Value	Description
Read	0	Normal Internal Crystal oscillation
	1	Internal Crystal oscillation stops

7.2.8.5 RTC Internal Event Triggered Time Stamp, Multiple Time Stamp

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x34	time stamp control1	○	○	○	○	○	EISEL	TSCEL	TSRAM	R/W
0x35	time stamp control2	●	○	○	○	ECMP	EVDET	EVLOW	EXST	R/W
0x36	time stamp contro3	○	○	○	TSFULL	TSEMP	TSAD[2:0]			R

■ Time stamp by self-monitor detection of RTC

1）ECMP bit (Enable VCMP)

This bit controls time stamp (VCMP) ON/OFF.

ECMP	Value	Description
Write	0	Time stamp (VCMP) OFF
	1	Time stamp (VCMP) ON

2）EVDET bit (Enable VDET)

This bit controls time stamp (VDET) ON/OFF.

EVDET	Value	Description
Write	0	Time stamp (VDET) OFF
	1	Time stamp (VDET) ON

3）EVLOW bit (Enable VLOW)

This bit controls time stamp (VLOW) ON/OFF.

EVLOW	Value	Description
Write	0	Time stamp (VLOW) OFF
	1	Time stamp (VLOW) ON

EXST bit (Enable X'tal Oscillation Stop)

This bit controls time stamp (XST) ON/OFF.

XST	Value	Description
Write	0	Time stamp (XST) OFF
	1	Time stamp (XST) ON

■ Multiple time stamp is available with following registers management.

The record area (40h ~ 7Fh) all the time stamp is recorded except 1/1024 sec, 1/512 sec, WEEK.

1) TSRAM bit

This bit control RAM (40h~7Fh) the usage time stamp recording or normal RAM.

TSRAM	Value	Description
Write	0	40h~7Fh is used a normal (Read/Write enable). Time stamp data is recorded into 20h-28h at event timing.
	1	40h~7Fh is used a time stamp recording memory. (Read/Write enable). User can modify directly RAM data via I2C if necessary.

2) TSCLR bit

The operation of writing "1" to this bit makes address 36h clear to initialize and this bit be reset to "0" automatically. Time stamp function should be disenabled by resetting ETS to "0" before this operation (Time stamp clear).

TSCLR	Value	Description
Write	0	Invalid
	1	Initializing address 36h register. TSFUL: 0, TSEMP: 1 TSAD2: 1, TSAD1: 1, TSAD0: 1

3) EISEL bit (Event Interrupt Select)

This bit controls time stamp event interrupt selection.

EISEL	Value	Description
Write	0	Every time stamp event triggering makes interrupt output.
	1	In case of 8 times record (of time stamp) interrupt output occurs.

■ Multiple time stamp recording function

1) TSFUL bit (Time Stamp Full)

This bit is reflected by 8 times time stamp recording.

TSFUL	Value	Description
Read	0	There is (are) empty RAM area.
	1	RAM area is fully occupied by 8 times time stamp recording.

2) TSEMP bit (Time Stamp Empty)

This bit is monitoring bit of RAM empty.

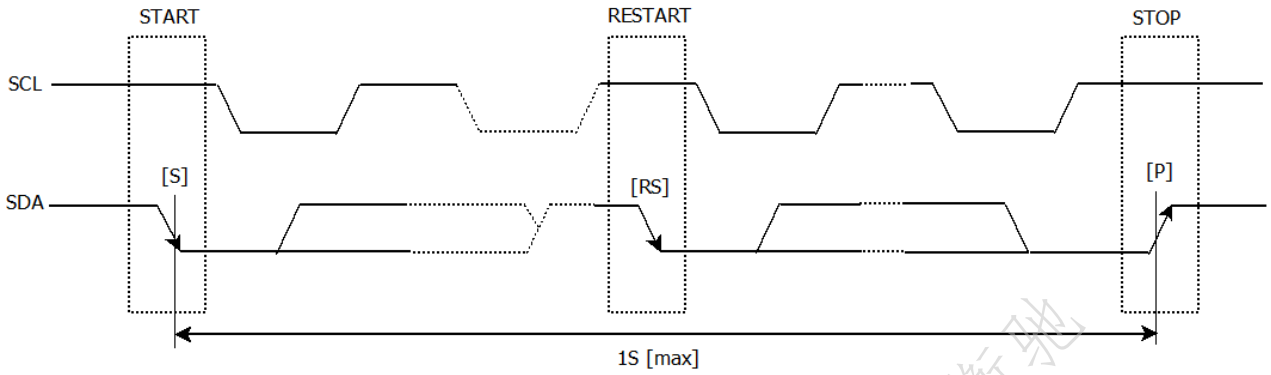
TSEMP	Value	Description
Read	0	There is some data recording in the RAM area (40h ~ 7fh).
	1	There is no data recording in the RAM area (40h ~ 7fh).

3) TSAD2, TSAD1, TSAD0bit (Time Stamp Address)

These bits are monitoring register of the latest time stamp RAM address.

TSAD	TSAD2	TSAD1	TSAD0	Address pointer
Read	0	0	0	0x40~0x47
	0	0	1	0x48~0x4f
	0	1	0	0x50~0x57
	0	1	1	0x58~0x5f
	1	0	0	0x60~0x67
	1	0	1	0x68~0x6f
	1	1	0	0x70~0x77
	1	1	1	0x78~0x7f

8 I2C Bus Interface



I2C bus supports bi-directional communications through a serial clock line SCL and a serial data line SDA. I2C bus device can be defined as “Master” and “Slave”. INS5T8111 can only be used as Slave.

8.1 Cautions

I2C bus includes START, RESTART, STOP conditions, the duration between START and STOP must be less than 1 second just in case the bus to be set to standby mode automatically. If the time is more than 1S, INS5T8111 will reset I2C Interface.

INS5T8111 I2C bus interface supports single byte read/write operations as well as multiple bytes incremental access. After 0xFF address, the next one will be 0x00.

8.2 Slave Address

Table10. I2C Bus Slave Address

Transfer data	Slave address							R/W
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
65h (Read)	0	1	1	0	0	1	0	1 (Read)
64h (Write)								0 (Write)

INS5T8111 I2C bus Slave Address is [0110 010*].

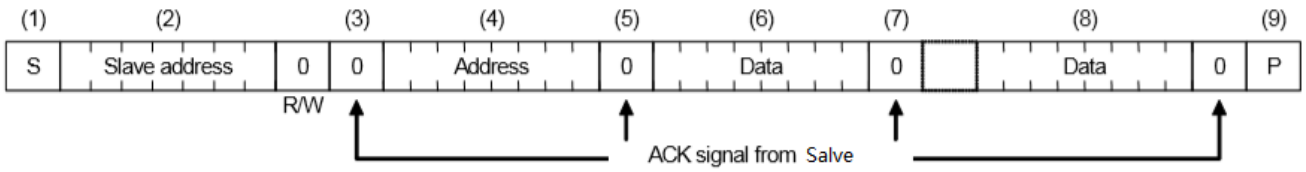
8.3 I2C bus protocol

It is assumed CPU is master and INS5T8111 is slave in this section.

8.3.1 Write process

I2C bus includes an address auto-increment function, once the initial address has been specified, the INS5T8111 increments (+1) the address automatically after each data is sent, then to write next data.

1. CPU sends start condition[S]
2. CPU sends INS5T8111's slave address with R/W bit to set to write mode
3. CPU verifies ACK signal from INS5T8111
4. CPU sends write address to INS5T8111
5. CPU verifies ACK signal from INS5T8111
6. CPU sends write data to the address specified at step (4)
7. CPU verifies ACK signal from INS5T8111
8. Repeat (6) (7) if multiple bytes need to be written, address will be incremented automatically
9. CPU ends stop condition[P]

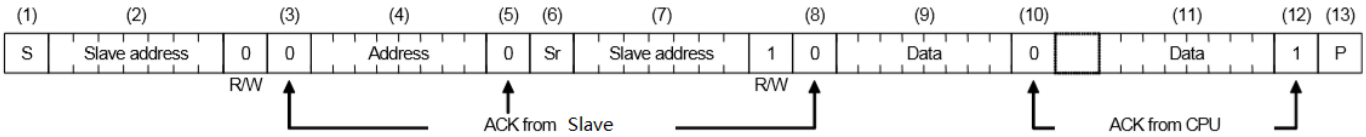


8.3.2 Read process

Writing the address to be read with write mode firstly, then reading the data with read mode.

1. CPU sends start condition[S]

2. CPU sends INS5T8111's slave address with R/W bit to set to write mode
3. CPU verifies ACK signal from INS5T8111
4. CPU sends address for reading from INS5T8111
5. CPU verifies ACK signal from INS5T8111
6. CPU sends RESTART condition [Sr]
7. CPU sends INS5T8111's slave address with R/W bit to set to read mode
8. CPU verifies ACK signal from INS5T8111
9. CPU reads data from the specified address in step (4)
10. CPU sends ACK signal for "0"
11. Repeat (9) (10) if multiple bytes need to be read, address will be incremented automatically
12. CPU sends ACK signal for "1"
13. CPU sends stop condition[P]



9 Reflow Soldering Curve

Standard: IPC/JEDEC J-STD-020

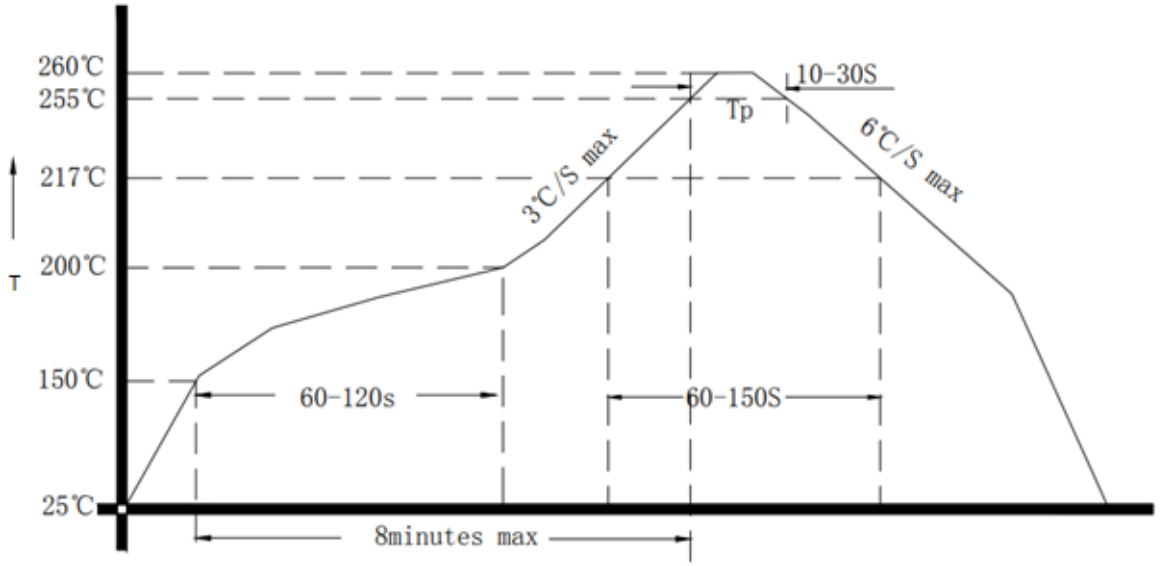


Figure 2. Reflow Soldering Curve

Note: It is suggested to solder IC under the condition shown in the curve above. Must pay attention to the temperature and time when manual soldering, if the temperature over +260℃, or you will make the xo performance bad, even damage it.

10 Dimensions

MPN: INS5T8111CFY / INS5T8111CFZ

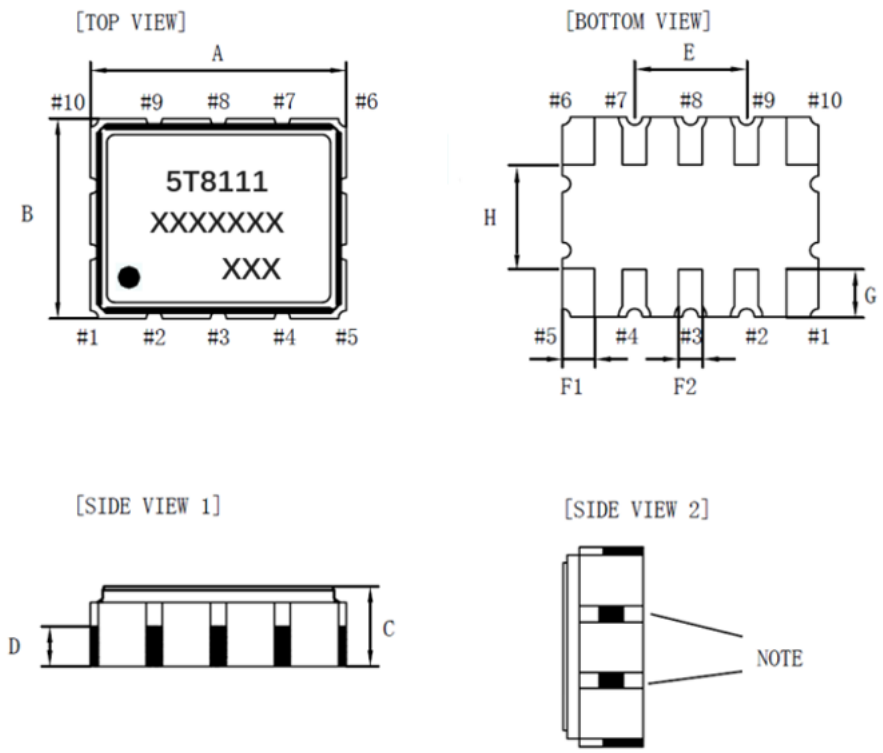


Figure 3. Dimensions

Dimension Unit: mm	Min.	Typ.	Max.
A	3.1	3.2	3.3
B	2.4	2.5	2.6
C	0.8	0.9	1.0
D	--	0.45	--
E	--	1.4	--
F1	--	0.4	--
F2	--	0.3	--
G	--	0.6	--
H	--	1.3	--

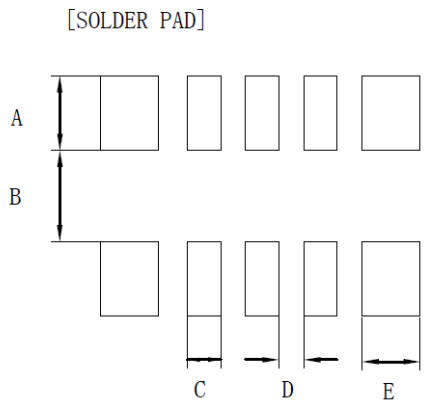


Figure 4. Recommended Solder Pad

Dimension Unit: mm	Recommend
A	0.9
B	1.1
C	0.4
D	0.3
E	0.7

Note:

1. The metal surface on the side shown in the figure is used for crystal test. Please avoid short circuit caused by contact between the metal surface and other electrical networks or other device surfaces during design and assembly.
2. The unnoted tolerance is ±0.1mm.

MPN: INS5T8111SFY / INS5T8111SFZ

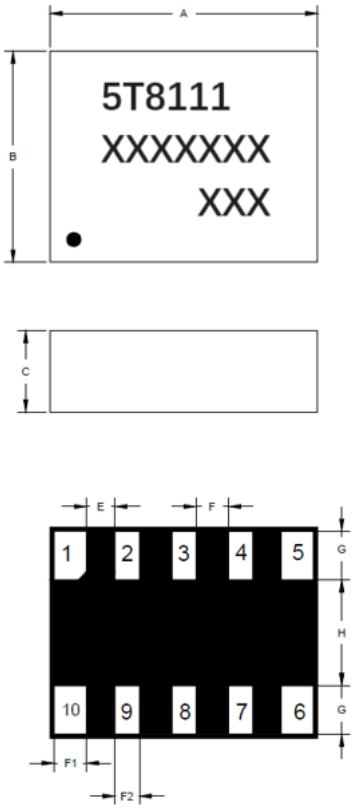


Figure 5. Dimension

Dimension Unit: mm	Min.	Typ.	Max.
A	3.0	3.2	3.4
B	2.3	2.5	2.7
C	--	1.0	--
E	--	0.3	--
F	--	0.4	--
G	--	0.6	--
H	--	1.3	--
F1	--	0.45	--
F2	--	0.3	--

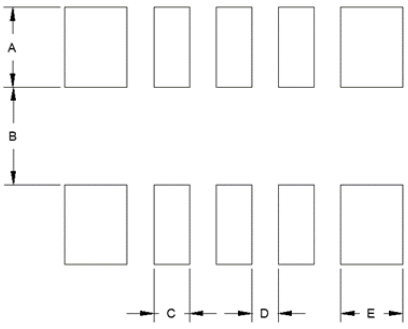


Figure 6. Recommended Soldering Pattern

Dimension	Max.
A	0.9
B	1.1
C	0.4
D	0.3
E	0.7

11 Package

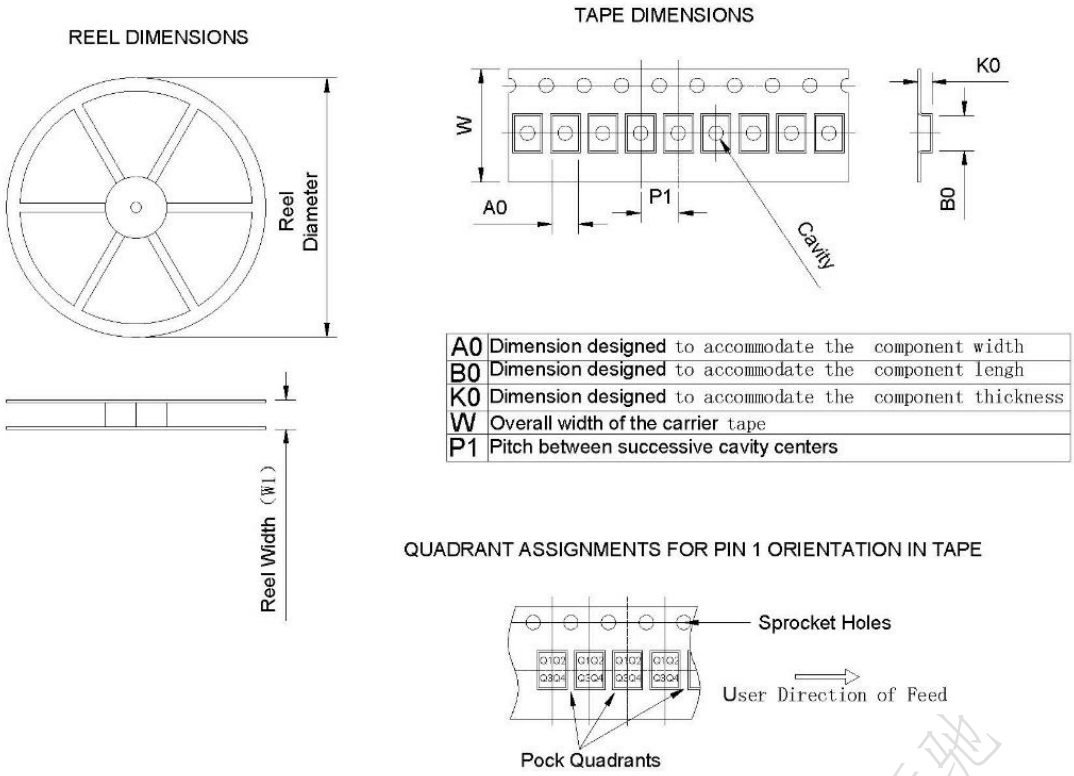


Figure 7. Package

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	PIN1 Quadrant
INS5T8111CFY	Ceramic	10	3000	180	11.6±2.0	3.00	3.70	1.50	4	8.00	Q1
INS5T8111CFZ	Ceramic	10	3000	180	11.6±2.0	3.00	3.70	1.50	4	8.00	Q1
INS5T8111SFY	LGA	10	3000	180	11.6±2.0	3.00	3.70	1.50	4	8.00	Q1
INS5T8111SFZ	LGA	10	3000	180	11.6±2.0	3.00	3.70	1.50	4	8.00	Q1

Revision History

Version	Change Contents	Prepared by	Revised Date
V1.0	First Issued		2024.06.20