



# INS5T8025 —Low Power Consumption High Accuracy I<sup>2</sup>C RTC

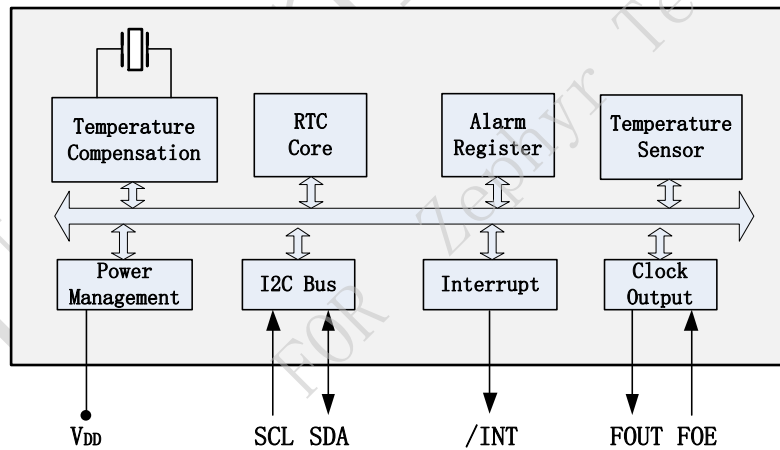
## Key Features

- Low current consumption: 1.0uA (Typ.)
- High stability:  
±3.4ppm @ -40°C ~ +85°C
- Build-in TCXO: 32.768KHz
- Build-in temperature sensor
- Communication Interface: I<sup>2</sup>C bus
- Power Supply Voltage: 1.6V~5.5V
- Operation Temperature Range: -40°C ~ +85°C
- Leap years autocorrection
- Timer output function with adjustable period
- Package: 10.1mm × 7.4mm × 3.2mm (SOP14)
- RoHS2.0 & REACH compliant

## Ordering Information

Part Name	Manufacture Part Number (MPN)	Description
INS5T8025	INS5T8025	±3.4ppm@-40°C~+85°C

## Block Diagram



## Overview

INS5T8025 is a high-accuracy I<sup>2</sup>C bus interface real-time clock with low power consumption. It embeds a 32.768KHz TCXO. The high precise temperature sensor and temperature compensated circuit ensure the high clock accuracy. It supports calendar (year, month, day, hour, minute, second), clock and timer functions etc. These features make it very suitable for energy, power devices and high-speed railway system application.



### Revision History

Version	Change Contents	Prepared by	Revised Date
V1.0	First Issued		2022.08.02
V1.1	<ol style="list-style-type: none"> <li>1. Update pin definition and description. (P6)</li> <li>2. Update temperature calculation formula: Temp [°C] = (TEMP[7:0] * 2 -147.5) / 3.0448. (P15)</li> <li>3. Add Frequency Offset register and related description. (P15)</li> <li>4. Update Packing information. (P21)</li> </ol>		2023.02.26
V1.2	<ol style="list-style-type: none"> <li>1. Key features Add “RoSH2.0 &amp; REACH compliant”</li> <li>2. Chapter 5.5 <ul style="list-style-type: none"> <li>- Change VDD voltage from “2.5V~4.5V” to “2.5V~5.5V”</li> <li>- Add tHD;DAT max value 0.9us</li> <li>- Change tr/td from 0.4us to 0.3us</li> </ul> </li> <li>3. Chapter 6.1 <ul style="list-style-type: none"> <li>- Change 0x0E/0x1E bit0 “Reserved” to “VDET”</li> <li>- Table9: Change 0x22~0x24 description “Ensure to be 0x00” to “Not use”</li> <li>- Add VDET description to Notes “Initial 1.....” &amp; “Only 0 can be written to.....”</li> </ul> </li> <li>4. Chapter 6.2.5 <ul style="list-style-type: none"> <li>- Change VLF voltage from “1.6V” to “1.4V”</li> <li>- Change bit0 description from “Reserved” to “VDET”</li> <li>- Add VDET description</li> </ul> </li> <li>5. Chapter 6.2.9 Change 0x22~0x24 description from “Ensure to be 0x00” to “Not use”</li> </ol>	LIN Jianhua	2023.04.11



	6. Chapter 9 Change marking “ST8025” to “5T8025”		
V1.3	1. Chapter 10, Packing Information SPQ value change from “1500pcs” to “1300pcs”		2023.11.30

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# 1 Overview

INS5T8025 is a high-accuracy I<sup>2</sup>C bus interface real-time clock with low power consumption. It embeds a 32.768KHz TCXO. The high precise temperature sensor and temperature compensated circuit ensure the high clock accuracy. It supports calendar (year, month, day, hour, minute, second), clock and timer functions etc. These features make it very suitable for energy, power devices and high-speed railway system application.

# 2 Block Diagram

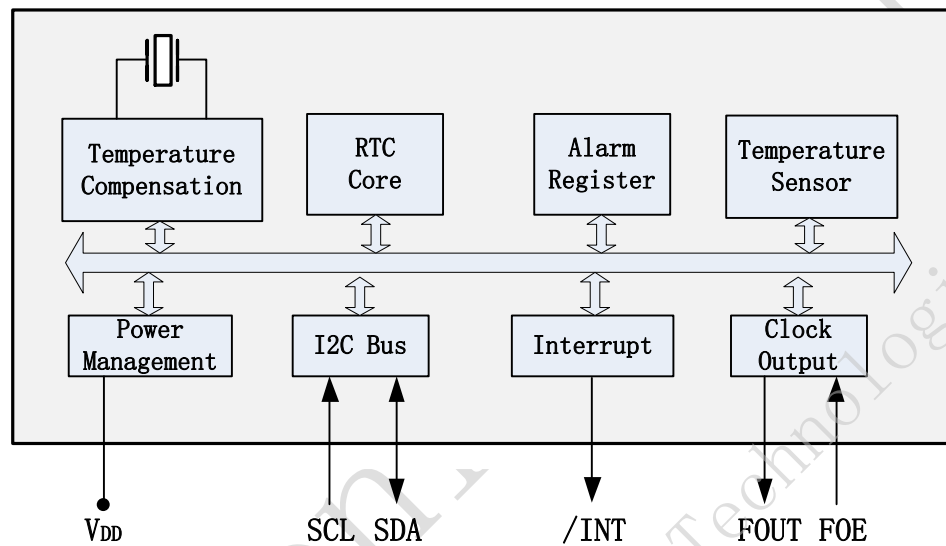


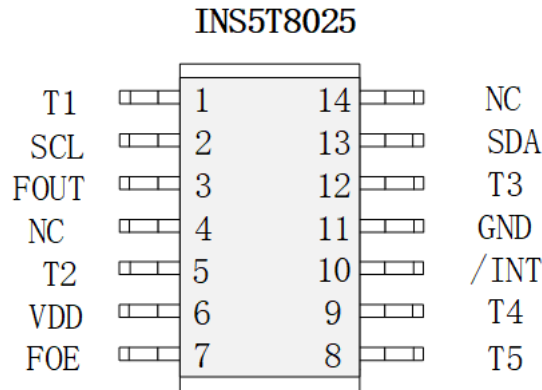
Figure 1. Block Diagram

# 3 Features

- Low current consumption: 1.0uA (Typ.)
- High stability:  
±3.4ppm @ -40°C ~ +85°C
- Communication Interface: I2C bus
- Build-in TCXO: 32.768KHz
- Build-in temperature sensor
- Power Supply Voltage: 1.6V ~ 5.5V
- Operation Temperature Range: -40°C ~ +85°C
- Leap years autocorrection
- Timer output function with adjustable period
- Package: 10.1mm × 7.4mm × 3.2mm (SOP14)
- RoHS2.0 & REACH compliant



## 4 Pin definition



**Table1. Pin Definition**

Pin Number	Pin Name	I/O	Description
1	T1	-	Manufacturer test only. Ensure to be floating.
2	SCL	In	I <sup>2</sup> C clock signal
3	FOUT	Out	Frequency output. Controlled by FOE. Frequency can be set by FSEL bits.
5	T2	-	Manufacturer test only. Ensure to be floating.
6	V <sub>DD</sub>	-	Power supply
7	FOE	In	FOUT output control pin. "1" - enable FOUT, "0"- FOUT Hi-Z
8	T5	-	Manufacturer test only. Ensure to be floating.
9	T4	-	Manufacturer test only. Ensure to be floating.
10	/INT	Out	Interrupt Output, Open-Drain
11	GND	-	Ground
12	T3	-	Manufacturer test only. Ensure to be floating.
13	SDA	In/Out	I <sup>2</sup> C data signal
4, 14	NC	-	Leave to be floated or connected to VDD or GND



## 5 Electrical Characteristics

### 5.1 Absolute Maximum Ratings

**Table2. Absolute Maximum Ratings**

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage	V <sub>DD</sub>	-0.3		6.5	V	
Input Voltage	V <sub>IN</sub>	GND-0.3		6.5	V	FOE, SCL, SDA input
Clock Output Voltage	V <sub>OUT1</sub>	GND-0.3		V <sub>DD</sub> +0.3	V	FOUT output
Output Voltage	V <sub>OUT2</sub>	GND-0.3		6.5	V	SDA, /INT output
Storage temperature	T <sub>STG</sub>	-55		125	°C	

### 5.2 Recommended Operating Conditions

**Table3. Recommended Operating Conditions**

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage	V <sub>DD</sub>	1.6	3.0	5.5	V	
Operation temperature	T <sub>OPR</sub>	-40	25	85	°C	

Note 1: V<sub>DD</sub> need to be supplied with more than 2.5V at least for the oscillation to stabilize (oscillation start time t<sub>STA</sub>).

Note2: After powered off, ensure that V<sub>DD</sub>=GND for more than 10 seconds before next power on

Note3: If there is no special indication, the test conditions are GND = 0V, V<sub>DD</sub> = 2.5V ~ 5.5V, T<sub>a</sub> = - 40 °C ~ + 85 °C

### 5.3 Frequency Characteristics

**Table4. Frequency Characteristics**

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Frequency stability	Δf/f	-3.4		+3.4	ppm	-40°C ~ +85°C
Oscillation start time	t <sub>STA</sub>			1	s	@25°C
Year Aging	f <sub>a</sub>			±3	ppm	@25°C, First year
Temperature Sensor Accuracy	T <sub>emp</sub>			±5	°C	V <sub>DD</sub> =3.0V
FOUT duty cycle	t <sub>w</sub> /t	40	50	60	%	

Note: If there is no special indication, the test conditions are GND = 0V, V<sub>DD</sub> = 2.5V ~ 5.5V, T<sub>a</sub> = - 40 °C ~ + 85 °C





## 5.4 DC Characteristics

**Table5. DC Characteristics**

Parameter	Symbol	Value			Unit	Notes	
		Min.	Typ.	Max.			
Average Current consumption1	I <sub>DD1</sub>		1.25	5.1	uA	V <sub>DD</sub> =5.0V	f <sub>SCL</sub> =0Hz, FOE=GND, /INT = V <sub>DD</sub> ; FOUT off (High-Z); Compensation interval 2s;
Average Current consumption2	I <sub>DD2</sub>		1.0	4.9		V <sub>DD</sub> =3.0V	
Average Current consumption3	I <sub>DD3</sub>		5.8	20	uA	V <sub>DD</sub> =5.0V	f <sub>SCL</sub> =0Hz, FOE=V <sub>DD</sub> , /INT = V <sub>DD</sub> ; FOUT:32.768kHz, CL=0pF; Compensation interval 2s;
Average Current consumption4	I <sub>DD4</sub>		3.8	19		V <sub>DD</sub> =3.0V	
High-level input voltage	V <sub>IH</sub>	0.8*V <sub>DD</sub>		5.5V	V	SCL, SDA, FOE pin	
Low-level input voltage	V <sub>IL</sub>	GND-0.3		0.2*V <sub>DD</sub>	V		
High-level output voltage	V <sub>OH1</sub>	4.0		5.0	V	V <sub>DD</sub> =5.0V, I <sub>OH</sub> = -1mA	FOUT pin
	V <sub>OH2</sub>	2.2		3.0		V <sub>DD</sub> =3.0V, I <sub>OH</sub> = -1mA	
	V <sub>OH3</sub>	2.9		3.0		V <sub>DD</sub> =3.0V, I <sub>OH</sub> = -100uA	
Low-level output voltage	V <sub>OL1</sub>	GND		GND+0.5	V	V <sub>DD</sub> =5.0V, I <sub>OL</sub> = 1mA	FOUT pin
	V <sub>OL2</sub>	GND		GND+0.8		V <sub>DD</sub> =3.0V, I <sub>OL</sub> = 1mA	
	V <sub>OL3</sub>	GND		GND+0.1		V <sub>DD</sub> =3.0V, I <sub>OL</sub> = 100uA	
	V <sub>OL4</sub>	GND		GND+0.25	V	V <sub>DD</sub> =5.0V, I <sub>OL</sub> = 1mA	/INT pin
	V <sub>OL5</sub>	GND		GND+0.4		V <sub>DD</sub> =3.0V, I <sub>OL</sub> = 1mA	
	V <sub>OL6</sub>	GND		GND+0.4	V	V <sub>DD</sub> ≥3.0V, I <sub>OL</sub> = 3mA	SDA pin
Input leakage current	I <sub>LK</sub>	-0.5		0.5	uA	FOE, SDA, SCL pin, V <sub>IN</sub> = V <sub>DD</sub> or GND	
Output leakage current	I <sub>OZ</sub>	-0.5		0.5	uA	FOUT, SDA, /INT pin, V <sub>IN</sub> = V <sub>DD</sub> or GND	

Note: If there is no special indication, the test conditions are GND = 0V, VDD = 2.5V ~ 5.5V, Ta = -40 °C ~ + 85 °C



### 5.5 AC Characteristics

**Table6. AC Characteristics**

V<sub>DD</sub>=2.5V ~ 5.5V; Ta=-40°C ~ +85°C

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
SCL clock frequency	f <sub>SCL</sub>			400	kHz
SCL low level time	t <sub>LOW</sub>	1.3			us
SCL high level time	t <sub>HIGH</sub>	0.6			us
Start condition setup time	t <sub>HD;STA</sub>	0.6			us
Start condition hold time	t <sub>SU;STA</sub>	0.6			us
Stop condition setup time	t <sub>SU;STO</sub>	0.6			us
Bus idle time between start condition and stop condition	t <sub>RCV</sub>	1.3			us
Data setup time	t <sub>SU;DAT</sub>	100			ns
Data hold time	t <sub>HD;DAT</sub>	0		0.9	us
SCL, SDA rising time	t <sub>r</sub>			0.3	us
SCL, SDA falling time	t <sub>f</sub>			0.3	us

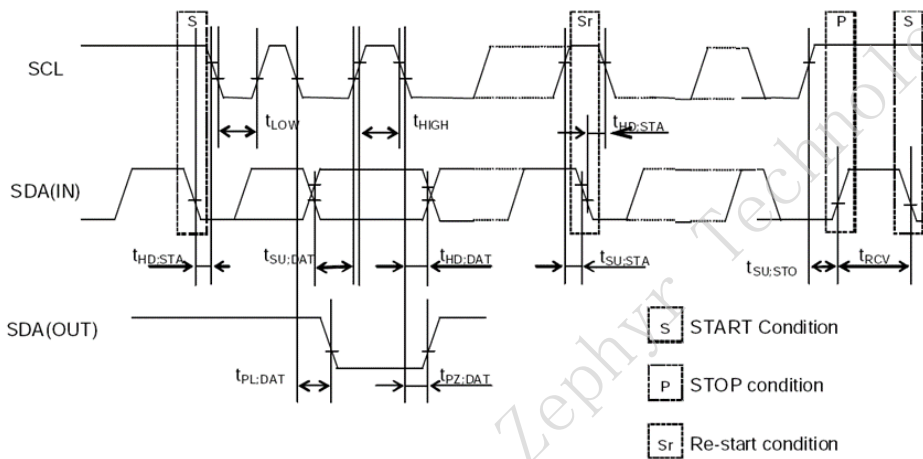


Figure 2. I<sup>2</sup>C bus Timing Chart

Note: when the master equipment accesses the equipment through I2C bus, all communication from sending start condition to sending stop shall be completed within 1 second. If it exceeds 1 second, the I2C bus interface will be reset through the internal bus timeout function.



## 6 Registers

### 6.1 Register Lists

Address 0x00~0x0F: Basic Time and Calendar Registers

Address 0x10~0x1F: Extended Register Group 1

Address 0x20~30: Extended Register Group 2

Note: 0x10~16 and 0x00~06 with the same function, 0x1B~1F and 0x0B~0F with the same function

**Table7. Basic Time and Calendar Registers**

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x00	SEC	○	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				R/W
0x01	MIN	○	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R/W
0x02	HOUR	○	○	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0x03	WEEK	○	6	5	4	3	2	1	0	R/W
0x04	DAY	○	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x05	MONTH	○	○	○	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				R/W
0x06	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				R/W
0x07	RAM	●	●	●	●	●	●	●	●	R/W
0x08	MIN Alarm	AE	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R/W
0x09	HOUR Alarm	AE	●	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0x0A	WEEK Alarm	AE	6	5	4	3	2	1	0	R/W
	DAY Alarm		●	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x0B	Timer Counter 0	128	64	32	16	8	4	2	1	R/W
0x0C	Timer Counter 1	●	●	●	●	2048	1024	512	256	R/W
0x0D	Extension Register	TEST	WADA	USEL	TE	FSEL [1]	FSEL [0]	TSEL [1]	TSEL [0]	R/W
0x0E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET	R/W
0x0F	Control Register	CSEL [1]	CSEL [0]	UIE	TIE	AIE	○	○	RESET	R/W

**Table8. Extended Register Group 1**

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x10	SEC	○	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				R/W
0x11	MIN	○	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R/W
0x12	HOUR	○	○	BCD code, Hour tens		BCD code, Hour ones place, 0-9				R/W



Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
				place, 0-2						
0x13	WEEK	○	6	5	4	3	2	1	0	R/W
0x14	DAY	○	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x15	MONTH	○	○	○	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				R/W
0x16	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				R/W
0x17	TEMP	128	64	32	16	8	4	2	1	R
0x18	RSV	Reserved								R/W
0x19	Not use	○	○	○	○	○	○	○	○	R
0x1A	Not use	○	○	○	○	○	○	○	○	R
0x1B	Timer Counter 0	128	64	32	16	8	4	2	1	R/W
0x1C	Timer Counter 1	●	●	●	●	2048	1024	512	256	R/W
0x1D	Extension Register	TEST	WADA	USEL	TE	FSEL [1]	FSEL [0]	TSEL [1]	TSEL [0]	R/W
0x1E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET	R/W
0x1F	Control Register	CSEL [1]	CSEL [0]	UIE	TIE	AIE	○	○	RESET	R/W

**Table9. Extended Register Group2**

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x20	Device ID	Vendor ID[3:0]				Ver[3:0]				R
0x21	RSV	Reserved: Ensure to be 0x80								R/W
0x22-24	RSV	Reserved: Not use								R/W
0x25	Offset0	○	○	○	○	○	S[4:2]			R/W
0x26	Offset1	S[1:0]		D[5:0]						R/W
0x27	SubSEC	Reserved				SubSEC[3:0]				R
0x28-30	RSV	Reserved: Ensure to be 0x00								R/W

Note:

1, After power-up reset or in case VLF bit returns “1”, make sure to initialize all registers to default state before using the RTC. Ensure all inputs are in the required range and the defined values are set for the reserved bits in case the clock cannot work normally.

- ✓ During the initial power-up, below bits will be in the state as below:  
Initial 0: TEST, WADA, USEL, TE, FSEL[1:0], TSEL[0], UF, TF, AF, CSEL[1], UIE, TIE, RESET,  
Initial 1: VLF, VDET, CSEL[0].
- ✓ All other register values are undefined, so make sure to reset the module before using it.
- ✓ The bits marked with “○” can be read out “0” only after initializing.
- ✓ The bits marked with “●” are RAM bits which can be used to write or read any data.
- ✓ Only 0 can be written to UF, TF, AF, VLF, VDET bits.
- ✓ Make sure “0” to be written for TEST bits which are used for testing only.
- ✓ Reserved bits must be set to the defined values accordingly.



## 6.2 Details of Registers

### 6.2.1 Clock counter registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x00/10	SEC	○	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				0x00
0x01/11	MIN	○	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x00
0x02/12	HOUR	○	○	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				0x00

SEC: BCD format, Value: 0~59

MIN: BCD format, Value: 0~59

HOUR: BCD format, Value: 0~23

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x03/13	WEEK	○	6	5	4	3	2	1	0	0x40

WEEK: Value 01h, 02h, 04h, 08h, 10h, 20h, 40h. Only one bit can be set to 1 each time, all others must be set to 0.

**Table10. WEEK Register**

WEEK	Data	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sunday	01h	0	0	0	0	0	0	0	1
Monday	02h	0	0	0	0	0	0	1	0
Tuesday	04h	0	0	0	0	0	1	0	0
Wednesday	08h	0	0	0	0	1	0	0	0
Thursday	10h	0	0	0	1	0	0	0	0
Friday	20h	0	0	1	0	0	0	0	0
Saturday	40h	0	1	0	0	0	0	0	0

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x04/14	DAY	○	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				0x01

DAY: BCD format, the value range will be adjusted automatically according to the month setting and if a leap year or not .

**Table11. DAY Register Value**

Month	Day Value Range
1, 3, 5, 7, 8, 10, 12	1~31
4, 6, 9, 11	1~30
February in normal year	1~28
February in leap year	1~29

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x05/15	MONTH	○	○	○	BCD code, Month	BCD code, Month ones place, 0-9				0x01



Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
					tens place, 0-1					
0x06/16	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				0x00

MONTH: BCD format, Value1~12

YEAR: BCD format, Value0~99(2000~2099)

Example: 2020/01/01 Wednesday 21:18:36

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x00/10	SEC	○	0	1	1	0	1	1	0
0x01/11	MIN	○	0	0	1	1	0	0	0
0x02/12	HOUR	○	○	1	0	0	0	0	1
0x03/13	WEEK	○	0	0	0	1	0	0	0
0x04/14	DAY	○	○	0	0	0	0	0	1
0x05/15	MONTH	○	○	○	0	0	0	0	1
0x06/16	YEAR	0	0	1	0	0	0	0	0

### 6.2.2 Alarm registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x08	MIN Alarm	AE	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x00
0x09	HOUR Alarm	AE	●	BCD code, Hour tens place, 0-2		BCD code, Minute ones place, 0-9				0x00
0x0A	WEEK Alarm	AE	6	5	4	3	2	1	0	0x00
	DAY Alarm		●	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				

According to AIE, AF, WADA bits setting, the alarm interrupt will be generated once the current time match the settings in the above registers, the /INT pin goes to low level and AF bit is set to '1' to record an alarm interrupt event has occurred.

WEEK Alarm/DAY Alarm: Controlled by WADA bit in 0x0D register

AE: Alarm Enable bit, 0-enable; 1-disable

AF: Defined in 0x0E register bit3

AIE: Defined in 0x0F register bit3

### 6.2.3 Timer control registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0B/1B	Timer Counter 0	128	64	32	16	8	4	2	1	0x00
0x0C/1C	Timer Counter 1	●	●	●	●	2048	1024	512	256	0x00

According to TE, TF, TIE, TSEL[1:0] bits setting, a timer interrupt will be generated once the value counts down to 0 from the one set in the above registers.

TE: Defined in 0x0D register bit4

TF: Defined in 0x0E register bit4

TIE: Defined in 0x0F register bit4



TSEL[1:0]: Defined in 0x0D register bit1 and bit0

### 6.2.4 Extension registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0D/1D	Extension Register	TEST	WADA	USEL	TE	FSEL[1]	FSEL[0]	TSEL[1]	TSEL[0]	0x02

TEST: Test bit, must be set to “0”

WADA: Week Alarm/Day Alarm control bit, decide 0x0A register as DAY Alarm or WEEK Alarm. 0-WEEK alarm, 1-DAY alarm

USEL: Update Interrupt Select bit, 0-output interrupt once a second, 1-output interrupt once a minute

TE: Timer Enable bit, 0-disable, 1-enable

FSEL[1], FSEL[0]: FOUT frequency setting:

FSEL[1]	FSEL[0]	FOUT Frequency
0	0	32.768KHz (Default)
0	1	1024Hz
1	0	1Hz
1	1	32.768KHz

TSEL[1], TSEL[0]: Timer countdown period(source clock) setting:

TSEL[1]	TSEL[0]	Source clock
0	0	4096Hz
0	1	64Hz
1	0	1Hz
1	1	1/60Hz

### 6.2.5 Flag registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0E/1E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET	0x03

UF: Update flag bit. When time update interrupt event occurs, it will be set to “1” and keeps “1” until a “0” is written to it.

TF: Timer Flag bit. When a fixed-cycle timer interrupt event occurs, it will be set to “1” and keeps “1” until a “0” is written to it.

AF: Alarm Flag bit. When an alarm interrupt event occurs, it will be set to “1” and keeps “1” until a “0” is written to it.

VLF: Voltage Low Flag bit. When supply voltage is lower than 1.4V, it will be set to “1” and keeps “1” until a “0” is written to it.

VDET: Voltage Detection Flag bit. When supply voltage is lower than 2.1V, it will be set to “1” and keeps “1” until a “0” is written to it.



## 6.2.6 Control registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0F/1F	Control Register	CSEL [1]	CSEL [0]	UIE	TIE	AIE	○	○	RESET	0x40

CSEL[1], CSEL[0]: Compensation interval Select 1, 0 bits, used to set temperature compensation interval.

CSEL[1]	CSEL[0]	Compensation interval
0	0	0.5s
0	1	2s(default)
1	0	10s
1	1	30s

UIE: Update Interrupt Enable bit. When UF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).

TIE: Timer Interrupt Enable bit: When TF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).

AIE: Alarm Interrupt Enable bit: When AF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).

RESET: Reset IC, prepared for the synchronized starting of time or timer.

## 6.2.7 Temperature register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x17	TEMP	128	64	32	16	8	4	2	1	0x00

Read digital temperature data, Temp [°C] = (TEMP[7:0] \* 2 - 147.5) / 3.0448.

## 6.2.8 Device ID register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x20	Device ID	VendorID[3:0]				Ver[3:0]				0xD2

VendorID[3:0]: The fixed value is defined as VendorID[3:0]=1101b=Dh to represent DAPU.

Ver[3:0]: version of the IC

## 6.2.9 RSV register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x21	RSV	Reserved: must be 0x80								0x80
0x22~ 0x24	RSV	Reserved: Not use								0x00

## 6.2.10 Frequency Offset register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x25	Frequency Offset0	Reserved	Reserved	Reserved	Reserved	Reserved	S [4]	S [3]	S [2]	0x00
0x26	Frequency Offset1	S [1]	S [0]	D [5]	D [4]	D [3]	D [2]	D [1]	D [0]	0x00





S [4:0]: Sign bits. Only 2b' 0 0000 and 2b' 1 1111 is legitimate.

D [5:0]: Data bits

S [4:0]	D [5:0]	Frequency Adjustment (ppm)
2b' 0 0000	2b'00 0000	0 (Default)
	2b'00 0001	-0.1
	2b'00 0010	-0.2
	...	...
	2b'11 1110	-6.2
	2b'11 1111	-6.3
2b' 1 1111	2b'11 1111	+0.1
	2b'11 1110	+0.2
	...	...
	2b'00 0010	+6.2
	2b'00 0001	+6.3
Other's	Other's	Invalid value, must be avoided.

Note: \*The Frequency offset register affects the frequency stability. Please be careful if you adjust it.

The offset function is effective for frequency adjustment at the normal temperature.

The single adjustment amount of 0.1ppm is approximate value.

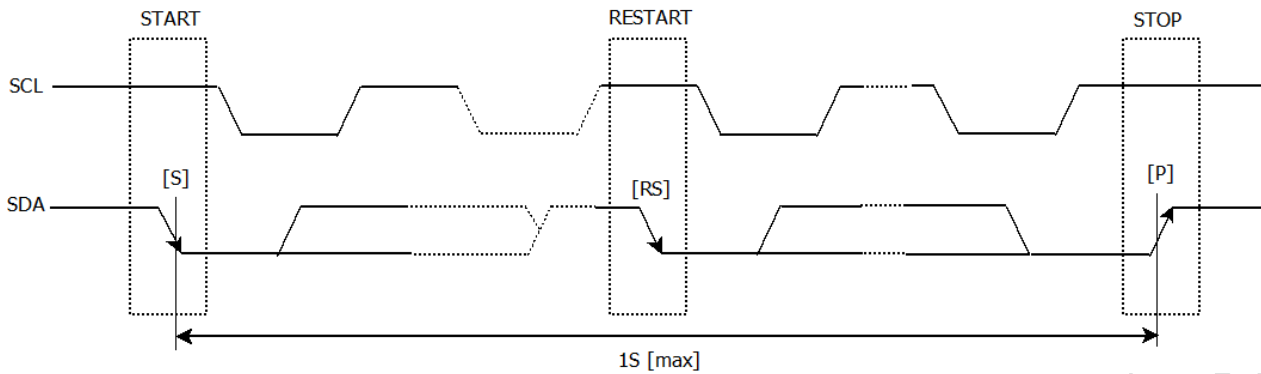
### 6.2.11 Sub-second timer register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x27	SubSEC	Reserved				SubSEC[3:0]				0x00

SubSEC[3:0]: sub second bit, and unit is 1/16s.



## 7 I<sup>2</sup>C Bus Interface



I<sup>2</sup>C bus supports bi-directional communications through a serial clock line SCL and a serial data line SDA. I<sup>2</sup>C bus device can be defined as “Master” and “Slave”. INS5T8025 can only be used as Slave.

### 7.1 Cautions

I<sup>2</sup>C bus includes START, RESTART, STOP conditions, the duration between START and STOP must be less than 1 second just in case the bus to be set to standby mode automatically. A new START condition must be transferred before restarting of any communications.

INS5T8025 I<sup>2</sup>C bus interface supports single byte read/write operations as well as multiple bytes incremental access. After 0xFF address, the next one will be 0x00.

### 7.2 Slave Address

Table12. I<sup>2</sup>C Bus Slave Address

Transfer data	Slave address							R/W
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
65h (Read)	0	1	1	0	0	1	0	1 (Read)
64h (Write)	0	1	1	0	0	1	0	0 (Write)

INS5T8025 I<sup>2</sup>C bus Slave Address is [0110 010\*].

### 7.3 I<sup>2</sup>C bus protocol

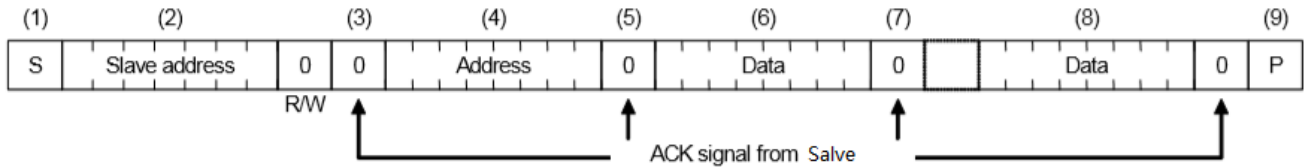
It is assumed CPU is master and INS5T8025 is slave in this section.

#### 7.3.1 Write process

I<sup>2</sup>C bus includes an address auto-increment function, once the initial address has been specified, the INS5T8025 increments (+1) the address automatically after each data is sent, then to write next data.



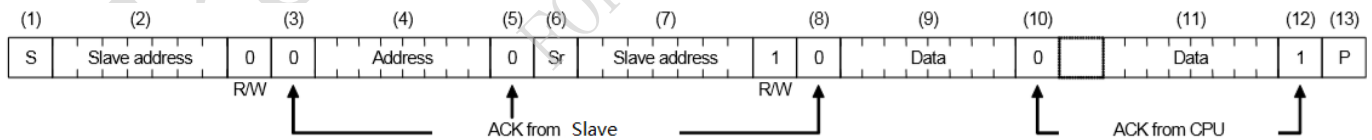
- (1) CPU sends start condition[S]
- (2) CPU sends INS5T8025's slave address with R/W bit to set to write mode
- (3) CPU verifies ACK signal from INS5T8025
- (4) CPU sends write address to INS5T8025
- (5) CPU verifies ACK signal from INS5T8025
- (6) CPU sends write data to the address specified at step (4)
- (7) CPU verifies ACK signal from INS5T8025
- (8) Repeat (6) (7) if multiple bytes need to be written, address will be incremented automatically
- (9) CPU ends stop condition[P]



### 7.3.2 Read process

Writing the address to be read with write mode firstly, then reading the data with read mode.

- (1) CPU sends start condition[S]
- (2) CPU sends INS5T8025's slave address with R/W bit to set to write mode
- (3) CPU verifies ACK signal from INS5T8025
- (4) CPU sends address for reading from INS5T8025
- (5) CPU verifies ACK signal from INS5T8025
- (6) CPU sends RESTART condition [Sr]
- (7) CPU sends INS5T8025's slave address with R/W bit to set to read mode
- (8) CPU verifies ACK signal from INS5T8025
- (9) CPU reads data from the specified address in step (4)
- (10) CPU sends ACK signal for "0"
- (11) Repeat (9) (10) if multiple bytes need to be read, address will be incremented automatically
- (12) CPU sends ACK signal for "1"
- (13) CPU sends stop condition[P]





## 8 Reflow Soldering Curve

Standard: IPC/JEDEC J-STD-020

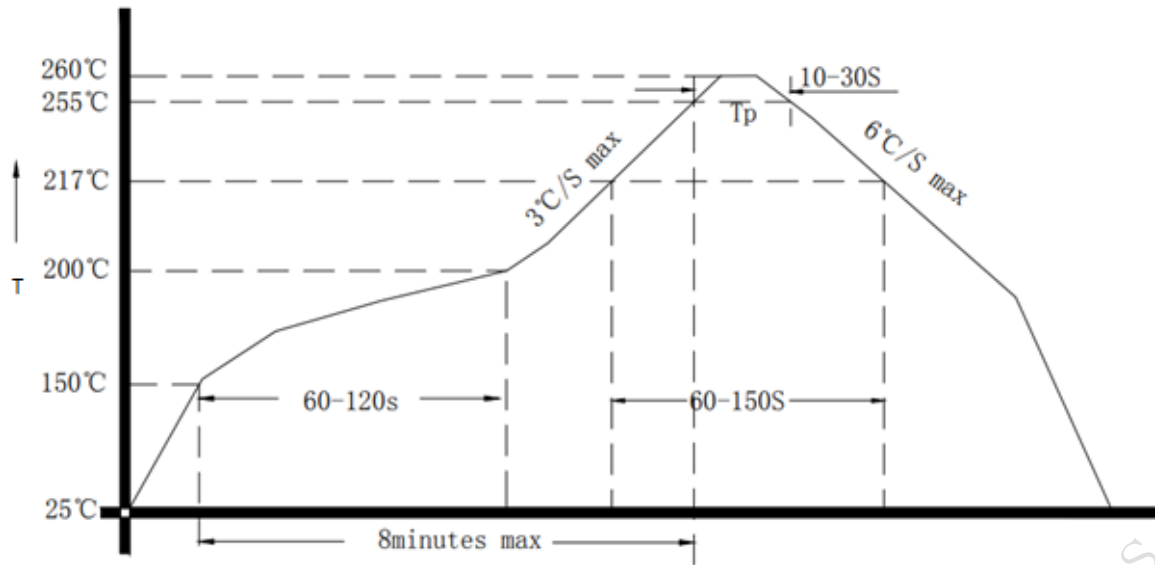
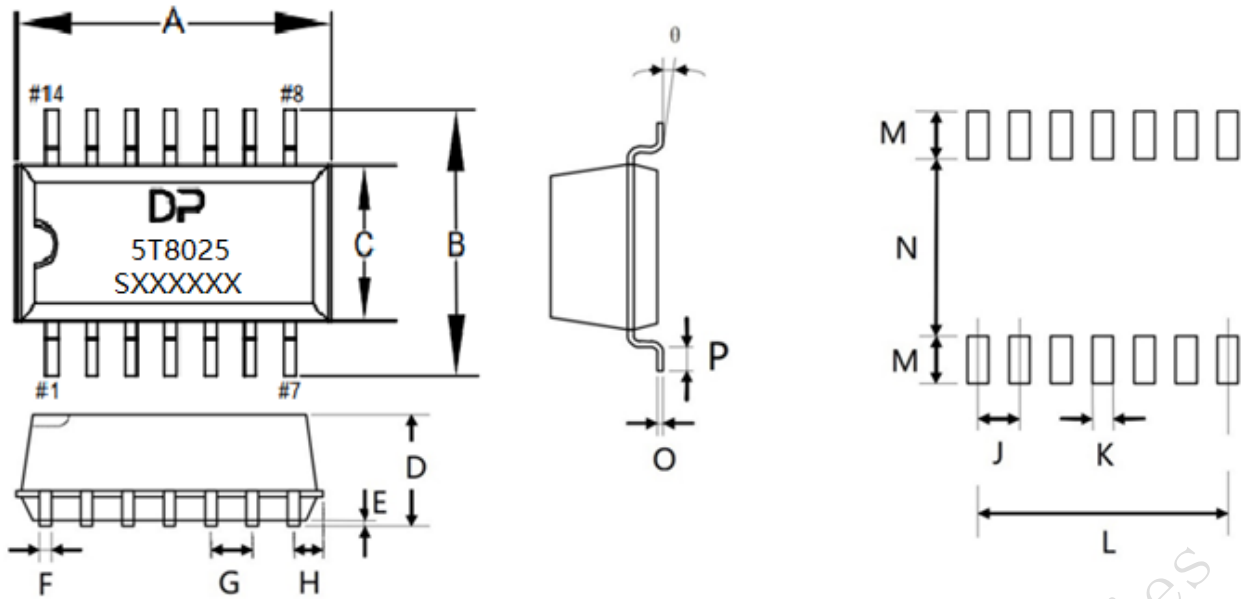


Figure 3. Reflow Soldering Curve

Note: It is suggested to solder IC under the condition shown in the curve above. Must pay attention to the temperature and time when manual soldering, if the temperature over +260°C, or you will make the xo performance bad, even damage it.



## 9 Package Dimensions



Dimension	Min.	Typ.	Max.
A	10.0	10.1	10.2
B	7.2	7.4	7.6
C	4.9	5.0	5.1
D	3.1	3.2	3.3
E	0.055	--	0.205
F	--	0.406	--
G	--	1.27	--
H	--	1.2	--
P	0.5	0.6	0.7
O	--	0.13	--
$\theta$	1°		8°

Unit: mm

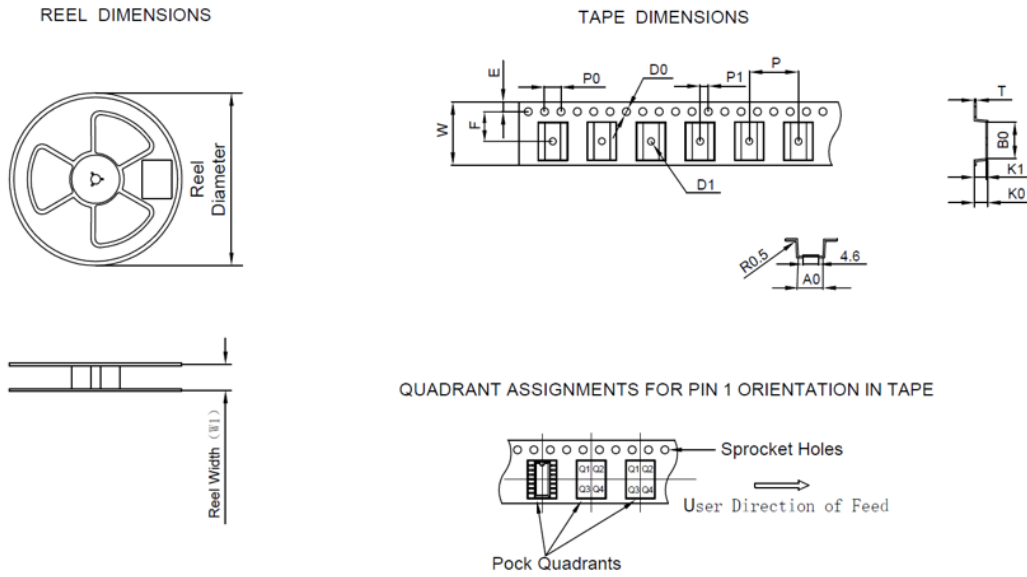
Dimension	Typ.
J	1.27
K	0.7
L	7.62
M	1.4
N	5.4

Unit: mm

Figure 4. Recommended Soldering Pattern and Dimension



# 10 Packing Information



Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	D0 (mm)	D1 (mm)	E (mm)	F (mm)	T (mm)	K0 (mm)	K1 (mm)	W (mm)	P (mm)	P0 (mm)	P1 (mm)	PIN1 Quadrant
INS5T8025	SOP14	14	1300pcs	330	16	8.0 ± 0.1	10.4 ± 0.1	1.5 ± 0.1	1.5 ± 0.1	1.75 ± 0.1	7.5 ± 0.1	0.3 ± 0.05	3.8 ± 0.1	3.5 ± 0.1	16 ± 0.3	12 ± 0.1	4 ± 0.1	2 ± 0.1	Q1

Figure 5. Packing Information