To Customer：_____

Realtime Clock Module

XPJ5711

Datasheet

Document Version 1.0

Released on May 24th, 2024

Ordering Information

Manufacture Part Number	Product Name	Description
XPJ5711-1AFY000N00MA	XPJ5711	±23ppm @ 25℃ -120ppm~10ppm @-20℃~70℃, SOP8

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1 Overview

XPJ5711 is a low-power RTC chip. It embeds a 32.768kHz TCXO. It supports calendar (year, month, day, hour, minute, second) function. The SOP8 package makes it suitable to be used in portable electronic devices.

2 Block Diagram

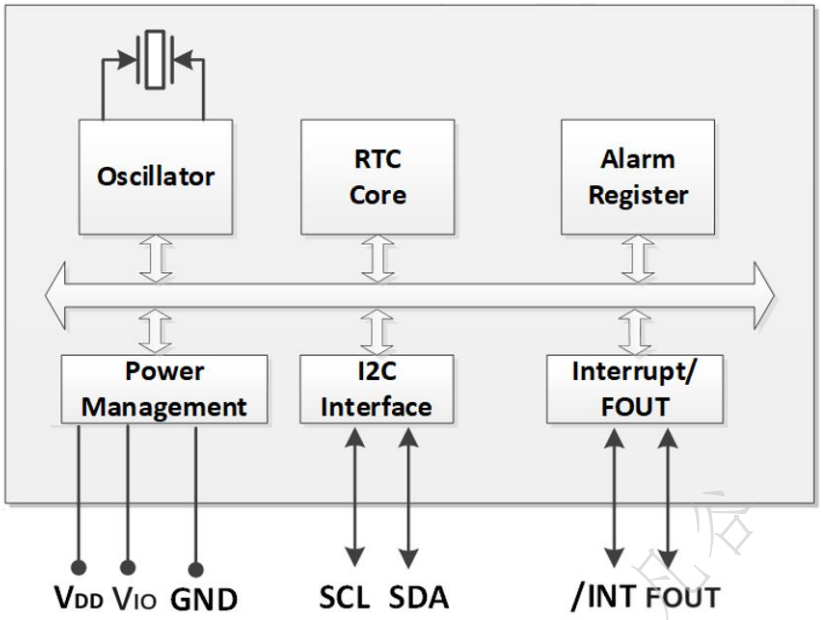


Figure 1. Block Diagram

3 Features

- Low Current Consumption: 0.25uA (Typ.)
- High Stability:
  ±23ppm @ 25℃
  -120ppm~10ppm @ -20℃ ~ +70℃
- Build-in XO: 32.768kHz
- RoHS2.0, REACH & Halogen-free compliant
- Communication Interface: I^2C bus
- Power Supply Voltage: 1.6V~5.5V
- Operation Temperature Range: -40℃ ~ +85℃
- Leap Years Autocorrection
- Package: 4.9mm × 6.0mm × 1.6mm (SOP8)

4 Pin Definition

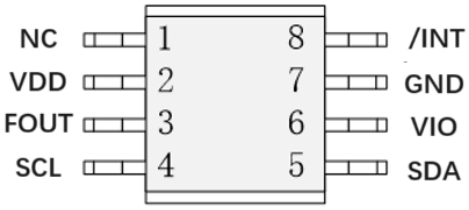


Figure 2. XPJ5711 PIN

Table1. Pin Definition

Pin Number	Pin Name	I/O	Description
1	NC	-	NC
2	VDD	-	Power in
3	FOUT	Out	Frequency output Pin, configurable, CMOS.
4	SCL	In	I2C clock signal
5	SDA	In/Out	I2C data signal
6	VIO	-	IO power in
7	GND	-	Ground
8	/INT	Out	Interrupt output (Open Drain)

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table2. Absolute Maximum Ratings

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage	V_{DD}	-0.3		6.5	V	
IO Power Supply Voltage	V_{IO}	-0.3		6.5	V	
I/O Input Voltage	V_{IN}	GND-0.3		6.5	V	SCL, SDA Input
Output Voltage1	V_{OUT1}	GND-0.3		6.5	V	SDA / INT Output
Output Voltage2	V_{OUT2}	GND-0.3		VDD+0.3	V	FOUT
Storage temperature	T_{STG}	-55		125	℃	

5.2 Recommended Operating Conditions

Table3. Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage (Startup)	V_{DD}	2.5	3.0	5.5	V	*
Power Supply Voltage (Normal mode)	V_{DD}	1.6	3.0	5.5	V	
Power Supply Voltage (Time keeping)	V_{DD}	1.2	3.0	5.5	V	
Operation temperature	T_{OPR}	-40	25	85	℃	

*Note 1: During the power on and vibration starting time, a voltage of more than 2.5V must be provided to ensure the stable vibration starting of the oscillation circuit.

Note2：After the power supply is powered off, ensure that VDD = GND for more than 10 seconds, and then power on.

Note3: If there is no special indication, the test conditions are GND = 0V, VDD = 1.6V ~ 5.5V, Ta = - 40 ℃ ~ + 85 ℃

5.3 Frequency Characteristics

Table4. Frequency Characteristics

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Frequency Tolerance	Δf/f	-23		+23	ppm	@25℃, V_{DD}=3.0V;
Frequency stability	f-t	-120		+10	ppm	VDD=3.0V; @-20℃～+70℃,refer to 25℃
Oscillation start time	t_{STA}			1	s	@25℃
Year Aging	f_a			±5	ppm	First year@25℃， VDD=3V

Note: If there is no special indication, the test conditions are GND = 0V, VDD = 1.6V ~ 5.5V, Ta = - 40 ℃ ~ + 85 ℃

5.4 DC Characteristics

Table5. DC Characteristics

Parameter	Symbol	Value			Unit	Notes	
		Min.	Typ.	Max.			
Average Current1	I_{DD1}		0.30	3	nA	V_{DD}=5.0V	fSCL=0Hz，SCL and SDA are low. V_{DD} pin.
Average Current2	I_{DD2}		0.25	2.5		V_{DD}=3.0V	
IO Average Current1	I_{IO1}		4.2	16	uA	V_{IO}=5.0V	fSCL=0Hz，SCL and SDA are high. V_{IO} pin. FOUT=32.768kHz, load=0pf
IO Average Current2	I_{IO2}		1.8	7		V_{IO}=3.0V	
Input High Voltage	V_{IH}	0.8*V_{IO}		5.5	V	SCL， SDA	
Input Low Voltage	V_{IL}	GND-0.3		0.2* V_{IO}	V		
Output Low Voltage	V_{OL1}	GND		GND+0.5	V	V_{IO} =5.0V, I_{OL} = 1mA	FOUT
	V_{OL2}	GND		GND+0.8		V_{IO} =3.0V, I_{OL} = 1mA	
	V_{OL3}	GND		GND+0.1		V_{IO} =3.0V, I_{OL} = 100uA	
	V_{OL4}	GND		GND+0.4		VDD=3.0V, I_{OL} = 1mA	/INT
	V_{OL5}	GND		GND+0.4	V	V_{IO}≥3.0V, I_{OL} = 3mA	SDA
Output High Voltage	V_{OH1}	4.0		5.0	V	V_{IO} =5.0V, I_{OH} = -1mA	FOUT
	V_{OH2}	2.2		3.0		V_{IO} =3.0V, I_{OH} = -1mA	
	V_{OH3}	2.9		3.0		V_{IO} =3.0V, I_{OH} = -100uA	
Input Leak Current	I_{LK}	-0.1		0.1	uA	SDA, SCL, V_{IN} = V_{IO} or GND	
Output Leak Current 1	I_{OZ1}	-0.1		0.1	uA	SDA, V_{IN} = V_{IO} or GND	
Output Leak Current 2	I_{OZ2}	-0.1		0.1	uA	/INT, V_{IN} = V_{DD} or GND	

Note3: If there is no special indication, the test conditions are GND = 0V, VDD = 1.6V ~ 5.5V, Ta = - 40 ℃ ~ + 85 ℃

5.5 AC Characteristics

Table6. AC Characteristics

V_{DD}=1.6V ~ 5.5V; V_{IO}=1.6~5.5V; Ta=-40℃ ~ +85℃

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}			400	kHz
SCL Low Voltage Time	t_{LOW}	1.3			us
SCL How Voltage Time	t_{HIGH}	0.6			us
Start condition hold time	$t_{HD;\ STA}$	0.6			us
Start condition setup time	$t_{SU;\ STA}$	0.6			us
Stop condition setup time	$t_{SU;\ STO}$	0.6			us
Bus idle time between start condition and stop condition	t_{RCV}	1.3			us
Data setup time	$t_{SU;\ DAT}$	100			ns
Data hold time	$t_{HD;\ DAT}$	0			ns
SCL, SDA rising time	t_r			0.3	us
SCL, SDA falling time	t_f			0.3	us

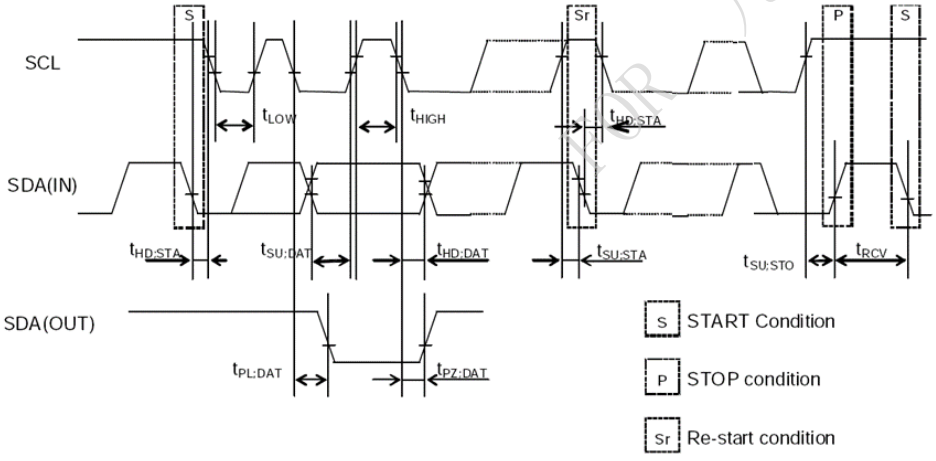


Figure 3. I2C bus Timing Chart

Note：When the master device gets access to this slave device through I2C, the whole operation duration should be less than 1s, otherwise it will be reset by the I2C bus through the internal bus overtime function.

6 Register

6.1 Register list

Table7. Registers List

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W	Default Value
0x10	SEC	○	40	20	10	8	4	2	1	R/W	0x00
0x11	MIN	○	40	20	10	8	4	2	1	R/W	0x00
0x12	HOUR	○	○	20	10	8	4	2	1	R/W	0x00
0x13	WEEK	○	6	5	4	3	2	1	0	R/W	0x40
0x14	DAY	○	○	20	10	8	4	2	1	R/W	0x01
0x15	MONTH	○	○	○	10	8	4	2	1	R/W	0x01
0x16	YEAR	80	40	20	10	8	4	2	1	R/W	0x00
0x17	MIN Alarm	AE	40	20	10	8	4	2	1	R/W	0x00
0x18	HOUR Alarm	AE	○	20	10	8	4	2	1	R/W	0x00
0x19	WEEK Alarm	AE	6	5	4	3	2	1	0	R/W	0x00
	DAY Alarm	AE	○	20	10	8	4	2	1	R/W	0x00
0x1A	Timer Counter 0	128	64	32	16	8	4	2	1	R/W	0x00
0x1B	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256	R/W	0x00
0x1C	Timer Counter 2	8388608	4194304	2097152	1048576	524288	262144	131072	65536	R/W	0x00

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W	Default Value
0x1D	Extension Register	FSEL 1	FSEL 0	USEL	TE	WA DA	○	TSEL [1]	TSEL [0]	R/W	0x02
0x1E	Flag Register	POR	○	UF	TF	AF	○	VLF	XST	R/W	0x80
0x1F	Control Register	○	○	UIE	TIE	AIE	○	○	STOP	R/W	0x00
0x2C	sec alarm	AE	40	20	10	8	4	2	1	R/W	0x00
0x2D	timer control	○	○	○	○	○	○	TMPIN	TSTP	R/W	0x00

Note: The bits marked with "○" can be read out "0" only after initializing.

6.2 Details of Registers

6.2.1 Clock counter registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x10	**SEC**	○	40	20	10	8	4	2	1	R/W
0x11	**MIN**	○	40	20	10	8	4	2	1	R/W
0x12	**HOUR**	○	○	20	10	8	4	2	1	R/W
0x13	**WEEK**	○	6	5	4	3	2	1	0	R/W
0x14	**DAY**	○	○	20	10	8	4	2	1	R/W
0x15	**MONTH**	○	○	○	10	8	4	2	1	R/W
0x16	**YEAR**	80	40	20	10	8	4	2	1	R/W
0x1F	Control Register	○	○	UIE	TIE	AIE	○	○	**STOP**	R/W

SEC: BCD format, Value: 0~59

MIN: BCD format, Value: 0~59

HOUR: BCD format, Value: 0~23

WEEK: Value 01h, 02h, 04h, 08h, 10h, 20h, 40h. Only one bit can be set to 1 each time, all others must be set to 0.

Table8. WEEK Register

WEEK	Data	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sunday	01h	0	0	0	0	0	0	0	1
Monday	02h	0	0	0	0	0	0	1	0
Tuesday	04h	0	0	0	0	0	1	0	0
Wednesday	08h	0	0	0	0	1	0	0	0
Thursday	10h	0	0	0	1	0	0	0	0
Friday	20h	0	0	1	0	0	0	0	0
Saturday	40h	0	1	0	0	0	0	0	0

DAY: BCD format, the value range will be adjusted automatically according to the month setting and if a leap year or not.

Table9. DAY Register Value

Month	Day Value Range
1, 3, 5, 7, 8, 10, 12	1~31
4, 6, 9, 11	1~30
February in normal year	1~28
February in leap year	1~29

MONTH: BCD format, Value1~12

YEAR: BCD format, Value0~99(2000~2099)

STOP: Stop calendar from 1/256s to year, and stop timer source clock of “64Hz / 1Hz / 1/60Hz”. When

STOP="1", 32768Hz and 1024Hz output is possible, but 1Hz output is disabled.

Example: 2020/01/01 Wednesday 21:18:36

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x10	SEC	○	0	1	1	0	1	1	0
0x11	MIN	○	0	0	1	1	0	0	0
0x12	HOUR	○	○	1	0	0	0	0	1
0x13	WEEK	○	0	0	0	1	0	0	0
0x14	DAY	○	○	0	0	0	0	0	1
0x15	MONTH	○	○	○	0	0	0	0	1
0x16	YEAR	0	0	1	0	0	0	0	0

6.2.2 Alarm Interrupt Function

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x17	MIN Alarm	**AE**	**40**	**20**	**10**	**8**	**4**	**2**	**1**	R/W
0x18	HOUR Alarm	**AE**	●	**20**	**10**	**8**	**4**	**2**	**1**	R/W
0x19	WEEK Alarm	**AE**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	R/W
	DAY Alarm	**AE**	●	**20**	**10**	**8**	**4**	**2**	**1**	R/W
0x1D	Extension Register	FSEL1	FSEL0	USEL	TE	**WADA**	○	TSEL[1]	TSEL[0]	R/W
0x1E	Flag Register	POR	○	UF	TF	**AF**	○	VLF	XST	R/W
0x1F	Control Register	○	○	UIE	TIE	**AIE**	○	○	STOP	R/W
0x2C	SEC Alarm	**AE**	**40**	**20**	**10**	**8**	**4**	**2**	**1**	R/W

1) WADA bit (Week Alarm / Day Alarm Select)

The alarm interrupt function uses either "Day" or "Week" as its target. The WADA bit is used to specify either WEEK or DAY as the target for alarm interrupt events.

Table10. WADA bit (Week Alarm / Day Alarm Select)

WADA	Value	Description
Write	0	Set WEEK as target of alarm function
	1	Set DAY as target of alarm function

2) AF (Alarm Flag)

Alarm Flag bit. When an alarm interrupt event occurs, it will be set to “1” and keeps “1” until a “0” is written to it.

Table11. AF Bit (Alarm Flag)

AF	Value	Description
Write	0	Clearing this bit to 0 enables /INTS low output to be canceled when an alarm interrupt event has occurred.
	1	Invalid
Read	0	-
	1	Alarm interrupt events are detected. (Result is retained until this bit is cleared to zero)

3) AIE Bit (Alarm Interrupt Enable)

Alarm Interrupt Enable bit: When AF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disenable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).

Table12. AIE Bit (Alarm Interrupt Enable)

AIE	Value	Description
Write	0	1) When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status remains Hi-Z). 2) When an alarm interrupt event occurs, the interrupt signal is canceled (/INT status changes from low to Hi-Z).
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low).

4) Example of alarm settings

✧ Example of alarm settings when “WEEK” has been specified (WADA=0)

	BIT7 AE	BIT6 Saturday	BIT5 Friday	BIT4 Thursday	BIT3 Wednesday	BIT2 Tuesday	BIT1 Monday	BIT0 Sunday	HOUR Alarm	MIN Alarm	SEC Alarm
Monday to Friday, at 6:00 AM 1 minute alarm	0	0	1	1	1	1	1	0	0x06	0x00	0x80
Every Monday, for 30 minutes each hour, Hour value is ignored	0	0	0	0	0	0	1	0	0x80	0x30	0x00
Every day, at 7:20:15 PM	0	1	1	1	1	1	1	1	0x19	0x20	0x15

✧ Example of alarm settings when “DAY” has been specified (WADA=1)

	BIT7 AE	BIT6	BIT5 20	BIT4 10	BIT3 08	BIT2 04	BIT1 02	BIT0 01	HOUR Alarm	MIN Alarm	SEC Alarm
5th of each month, at 8:00 AM 1 minute alarm. Second value is ignored	1	0	0	0	0	1	0	1	0x08	0x00	0x80
15th of each month, for 30 minute each month. Hour value is ignored.	1	0	0	1	0	1	0	1	0x80	0x30	0x00
Every day, at 7:20:15 PM	1	X	X	X	X	X	X	X	0x19	0x20	0x15

6.2.3 Wake-up Timer Interrupt Function

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x1A	Timer Counter 0	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**	R/W
0x1B	Timer Counter 1	**32768**	**16384**	**8192**	**4096**	**2048**	**1024**	**512**	**256**	R/W
0x1C	Timer Counter 2	**8388608**	**4194304**	**2097152**	**1048576**	**524288**	**262144**	**131072**	**65536**	R/W
0x1D	Extension Register	FSEL1	FSEL0	USEL	**TE**	WADA	○	**TSEL [1]**	**TSEL [0]**	R/W

0x1E	Flag Register	POR	○	UF	**TF**	AF	○	VLF	XST	R/W
0x1F	Control Register	○	○	UIE	**TIE**	AIE	○	○	STOP	R/W
0x2D	timer control	○	○	○	○	○	○	TMPIN	**TSTP**	R/W

The wake-up timer interrupt function generates an interrupt event periodically at any fixed cycle set between 244.14 μs and 31.9 years. This function can stop at one time and is available as an accumulative timer. After the interrupt occurs, the /INT status is automatically cleared.

Before entering operation settings, we recommend first clearing the TE bit to "0". When the fixed-cycle timer function is not being used, the fixed-cycle Timer Counter0,1 register can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.

1) Timer counter 2, 1, 0

Preset values of timer counter. Any value from 1(0x000001h) to 16777216 (0xFFFFFFh) can be set. Please ensure TE & TIE write “0” before writing timer counter

2) TE

This bit is use to control timer start / stop.

Table13. TE Bit (Timer Enable)

TE	Data	Description
Write	0	Stops wake-up interrupt timer interrupt function. Clearing this bit to zero does not enable the /INT low output status to be cleared (to Hi-Z).
	1	Starts wake-up interrupt timer interrupt function. The countdown that starts when the TE bit value changes from "0" to "1" always begins from the preset value.

3) TSEL[1], TSEL[0]

This bits be used to set the source clock of timer count down period.

Table14. TSEL[1:0] Selection of source clock

TESL[1]	TSEL[0]	Source Clock	Auto Reset Time(tRTN)
0	0	4096 Hz, once per 244.14us	122us
0	1	64 Hz, once per 15.625ms	7.813ms
1	0	1 Hz, once per 1 second	7.813ms
1	1	1/60 Hz, once per minute	7.813ms

Below shows an error of first countdown: Timer counter value is 3h

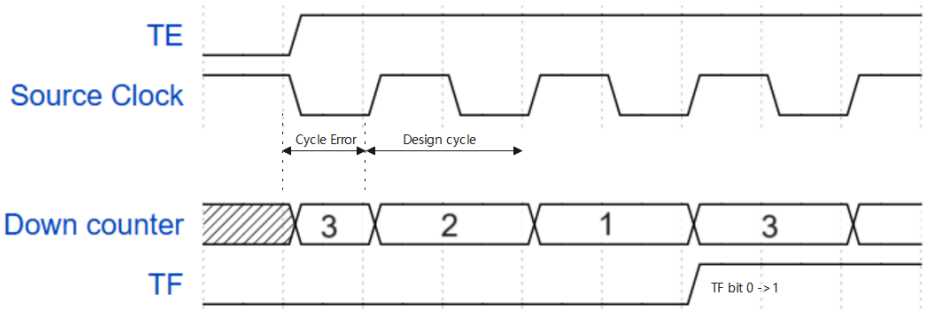


Figure 4. Cycle Error of Timer Initial Sequence

4) TF

Timer Flag bit. When a fixed-cycle timer interrupt event occurs, it will be set to "1" and keeps "1" until a "0" is written to it.

Table15. TF Bit

TF	Data	Description
Write	0	The TF bit is cleared to 0 to prepare for the next status detection. Clearing this bit to 0 is not enable the /INT low output status to Hi-Z.
	1	Invalid
Read	0	
	1	Wake-up timer interrupt events are detected. This bit will keep "1" until software to write "0".

5) TIE

Timer Interrupt Enable bit: When TF changes from "0" to "1", this bit controls if an interrupt signal is generated. 0-disenable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).

Table16. TIE Bit

TIE	Value	Description
Write	0	1.When a wake-up timer interrupt event occurs, an interrupt signal is not generated. When a wake-up timer interrupt event occurs, the interrupt signal is canceled. (/INT status change from low to Hi-Z).
	1	When a wake-up timer interrupt event occurs, an interrupt signal is generated. (/INT status changes from Hi-Z to low)

6) TBKON, TBKE (Timer Backup ON, Timer Backup/normal Enable)

This bit set operation timer with the main power supply or the backup power supply.

Table17. TBKON, TBKE Bit

	TBKE	TBKON	Description
Write	0	X	This setting counts at normal mode and backup mode.

	1	0	This setting counts at normal mode (VDD Operation).
	1	1	This setting counts at backup mode (VBAT Operation).

7) TMPIN

This timer interrupt output can be assigned to FOUT pin.

To output only the interrupt on FOUT pin, set the FOUT output setting to FSEL[1:0] = 11b, FOUT is stopped.

Table18. TMPIN Bit

TMPIN	Value	Description
Write	0	Timer interruption is output from /INT pin. (Open Drain)
	1	Timer interruption is output from FOUT pin. (CMOS)

8) TSTP (Timer Stop)

This bit is used to stop wake-up timer count down.

Table19. TSTP Bit

TE	STOP	TBKE	TSTP	Description
1	0	0	0	Write a "0", it will cancels stop status (restart timer counts down).
			1	Write a "1", it will stop timer counts down.
		1	X	Write a "1" is invalid. Timer count does not stop even if set TSTP="1"
	1	X	X	The count stops at the timer of the setting of 64Hz, 1Hz, 1/60Hz.
0	X	X	X	It doesn't start counting.

6.2.4 Time Update Interrupt Function

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x1D	Extension Register	FSEL1	FSEL0	**USEL**	TE	WADA	○	TSEL [1]	TSEL [0]	R/W
0x1E	Flag Register	POR	○	**UF**	TF	AF	○	VLF	XST	R/W

0x1F	Control Register	○	○	**UIE**	TIE	AIE	○	○	STOP	R/W

1) USEL (Update Selection)
This bit is used to select "second" update or "minute" update as the timing for generation of time update interrupt events.

Table20. USEL Bit

USEL	Value	Description
Write / Read	0	Selects “Second update” (once per second) as the timing for generation of interrupt events.
	1	Selects “Minute update” (once per minute) as the timing for generation of interrupt events.

2) UF (Update Flag)
This flag bit value changes from "0" to "1" when a time update interrupt event occurs.

Table21. UF Bit

UF	Value	Description
Write	0	Clearing this bit to zero enables /INT low output to be canceled (/INT remains Hi-Z) when a time update interrupt event has occurred.
	1	Invalid
Read	0	-
	1	Time update interrupt events are detection. Keeping “1” until software to write “0”.

3) UIE (Update Interrupt Enable)
This bit selects whether to generate an interrupt signal or not generate it.

Table22. UIE Bit

UIE	Description
0	Does not output an interrupt signal when a time update interrupt event occurs.
1	Time update interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low).

6.2.5 Clock Output Function

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x1D	Extension Register	**FSEL1**	**FSEL0**	USEL	TE	WADA	○	TSEL [1]	TSEL [0]	R/W

This function is use to configure the FOUT frequency.

1) FSEL1, FSEL0

Table23. FSEL1, FSEL0

TMPIN	FSEL1	FSEL0	Description
0	0	0	FOUT output 32.768kHz (Default)
	0	1	FOUT output 1024Hz
	1	0	FOUT output 1Hz
	1	1	FOUT output off
1	X	X	FOUT output off

6.2.6 Self-Monitor Detection

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x1E	Flag Register	**POR**	○	UF	TF	AF	○	**VLF**	**XST**	R/W

Self-Monitor is a function of detecting RTC status and holding the result.

1) POR bit (Power on Reset)

This bit detect power on reset operation.

Table24. POR Bit

POR	Value	Description
Write	0	Clear flag and waiting for the next power on reset detection.
	1	Invalid.
Read	0	No power on reset detection.
	1	Power on reset is detected. Keeping the result until software write “0”. All registers are set into default when power on reset.

2) VLF (Voltage Low Flag)

This bit is use to detect the status of VDD low voltage (1.2V Typ.).

Table25. VLF Bit

VLF	Value	Description
Write	0	Clear flag and waiting for the next low voltage detection.
	1	Invalid.
Read	0	No low voltage detection.
	1	VDD low voltage is detected. Keeping the result until software write “0”. The RTC is working abnormally. Unser can check the RTC status and initialize by software.

3) XST (X’tal Oscillation Stop)

This bit is use to detect the status of internal X’tal stopping.

Table26. XST Bit

XST	Value	Description
Write	0	Clear flag and waiting for the next internal X’tal stopping detection.
	1	Invalid.
Read	0	No internal X’tal stopping detection.
	1	Internal X’tal stopping is detected. Keeping the result until software write “0”.

7 I2C Bus Interface

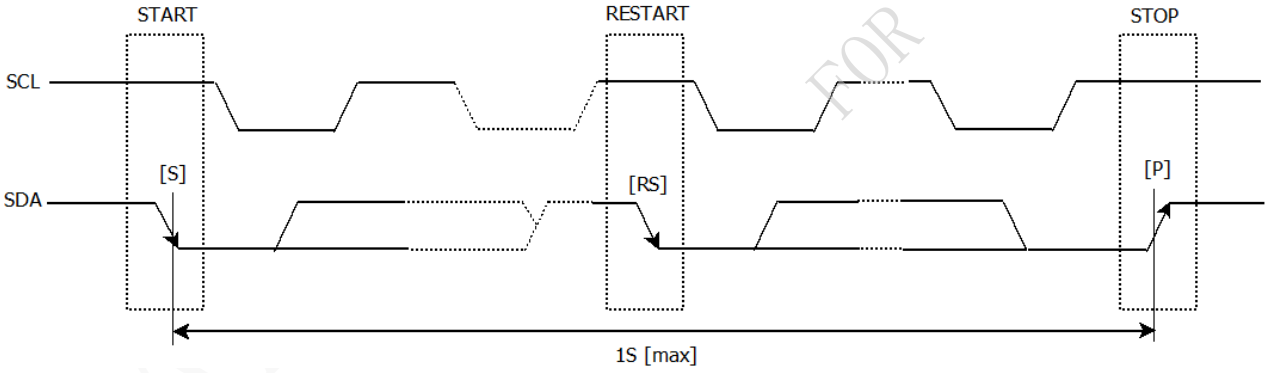


Figure 5. I2C Timing

I²C bus supports bi-directional communications through a serial clock line SCL and a serial data line SDA. I²C bus device can be defined as “Master” and “Slave”. XPJ5711 can only be used as Slave.

7.1 Cautions

I²C bus includes START, RESTART, STOP conditions, the duration between START and STOP must be

less than 1 second just in case the bus to be set to standby mode automatically. If the time is more than 1S, XPJ5711 will reset I²C Interface.

XPJ5711 I²C bus interface supports single byte read/write operations as well as multiple bytes incremental access. After 0xFF address, the next one will be 0x00.

7.2 Slave Address

Table27. I2C Bus Slave Address

Transfer data	Slave address							R/W
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
65h (Read)	0	1	1	0	0	1	0	1 (Read)
64h (Write)								0 (Write)

XPJ5711 I²C bus Slave Address is [0110 010*].

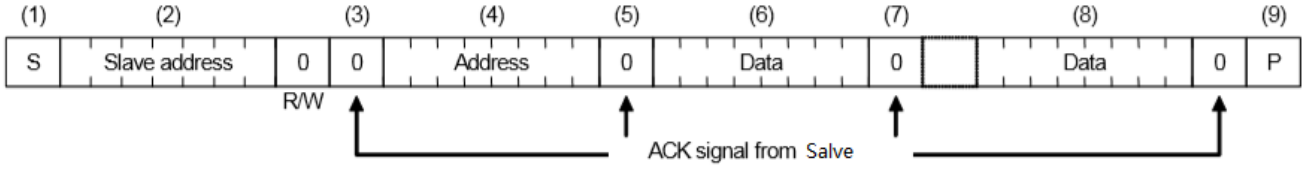
7.3 I2C bus protocol

It is assumed CPU is master and XPJ5711 is slave in this section.

7.3.1 Write process

I²C bus includes an address auto-increment function, once the initial address has been specified, the XPJ5711 increments (+1) the address automatically after each data is sent, then to write next data.

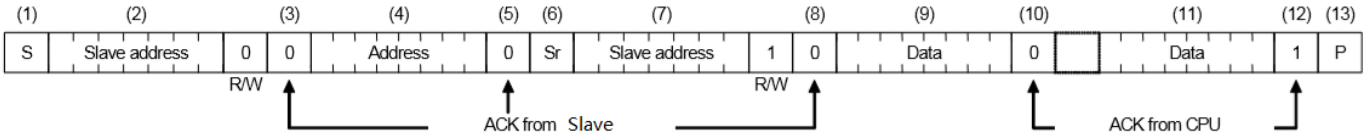
(1) CPU sends start condition[S]
(2) CPU sends XPJ5711's slave address with R/W bit to set to write mode
(3) CPU verifies ACK signal from XPJ5711
(4) CPU sends write address to XPJ5711
(5) CPU verifies ACK signal from XPJ5711
(6) CPU sends write data to the address specified at step (4)
(7) CPU verifies ACK signal from XPJ5711
(8) Repeat (6) (7) if multiple bytes need to be written, address will be incremented automatically
(9) CPU ends stop condition[P]



7.3.2 Read process

Writing the address to be read with write mode firstly, then reading the data with read mode.

(1) CPU sends start condition[S]
(2) CPU sends XPJ5711's slave address with R/W bit to set to write mode
(3) CPU verifies ACK signal from XPJ5711
(4) CPU sends address for reading from XPJ5711
(5) CPU verifies ACK signal from XPJ5711
(6) CPU sends RESTART condition [Sr]
(7) CPU sends XPJ5711's slave address with R/W bit to set to read mode
(8) CPU verifies ACK signal from XPJ5711
(9) CPU reads data from the specified address in step (4)
(10) CPU sends ACK signal for "0"
(11) Repeat (9) (10) if multiple bytes need to be read, address will be incremented automatically
(12) CPU sends ACK signal for "1"
(13) CPU sends stop condition[P]



8 Reflow Soldering Curve

Standard: IPC/JEDEC J-STD-020

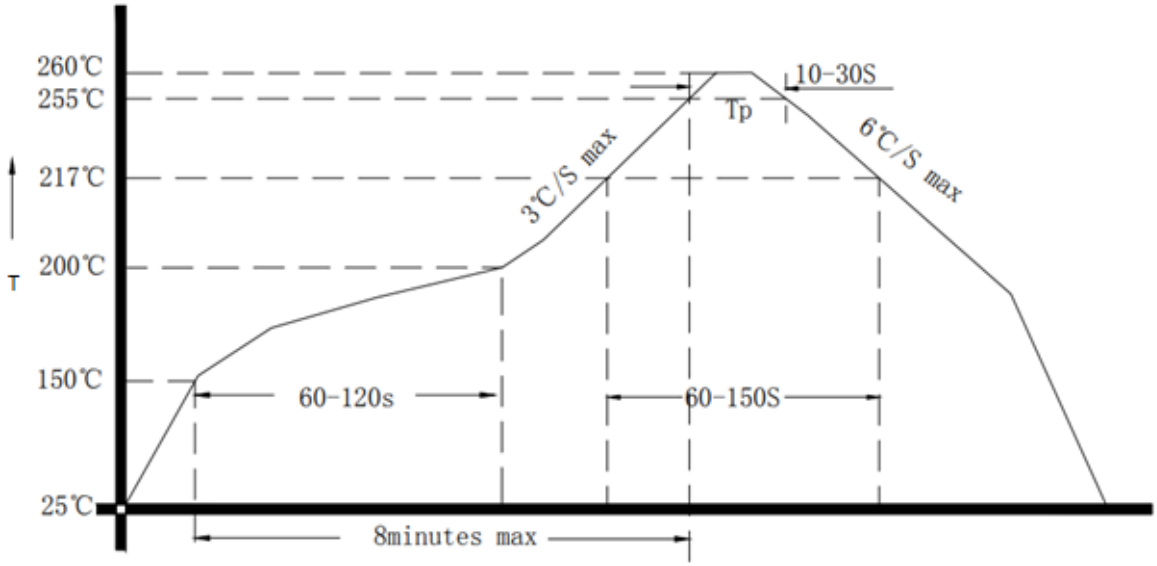


Figure 6. Reflow Soldering Curve

Note: It is suggested to solder IC under the condition shown in the curve above. Must pay attention to the temperature and time when manual soldering, if the temperature over +260℃, or you will make the xo performance bad, even damage it.

9 Dimensions

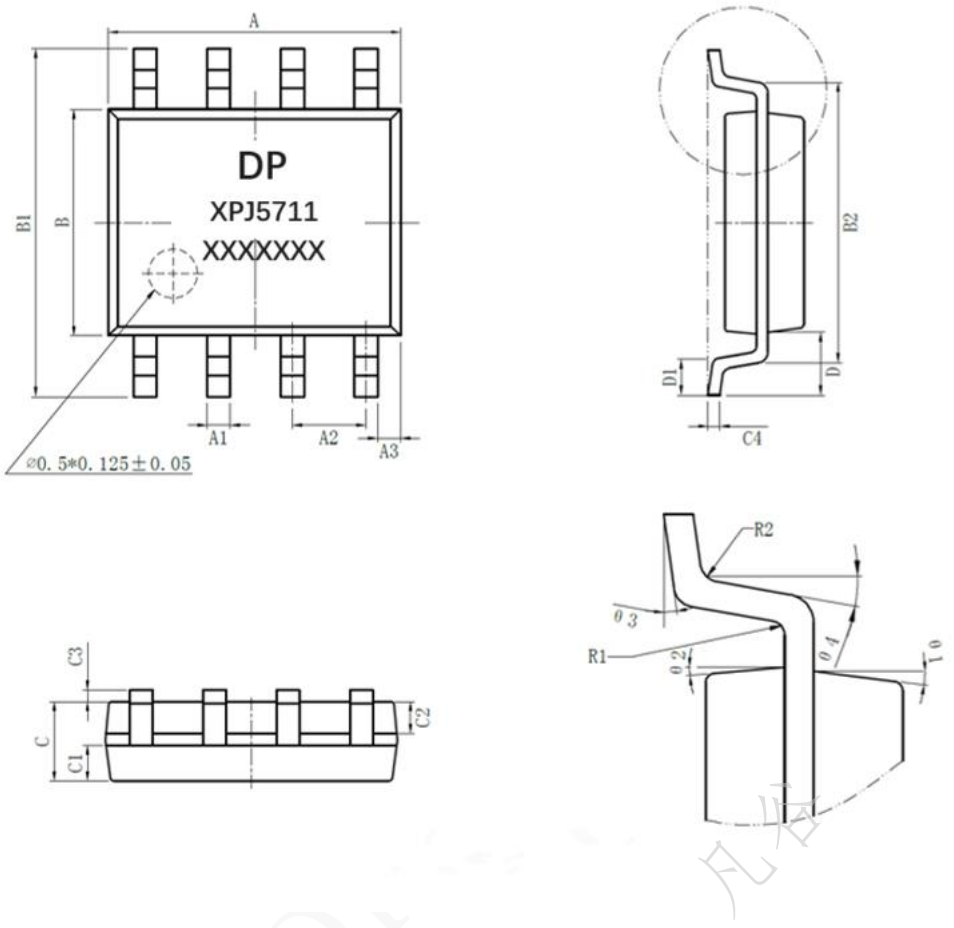


Figure 7. Dimension

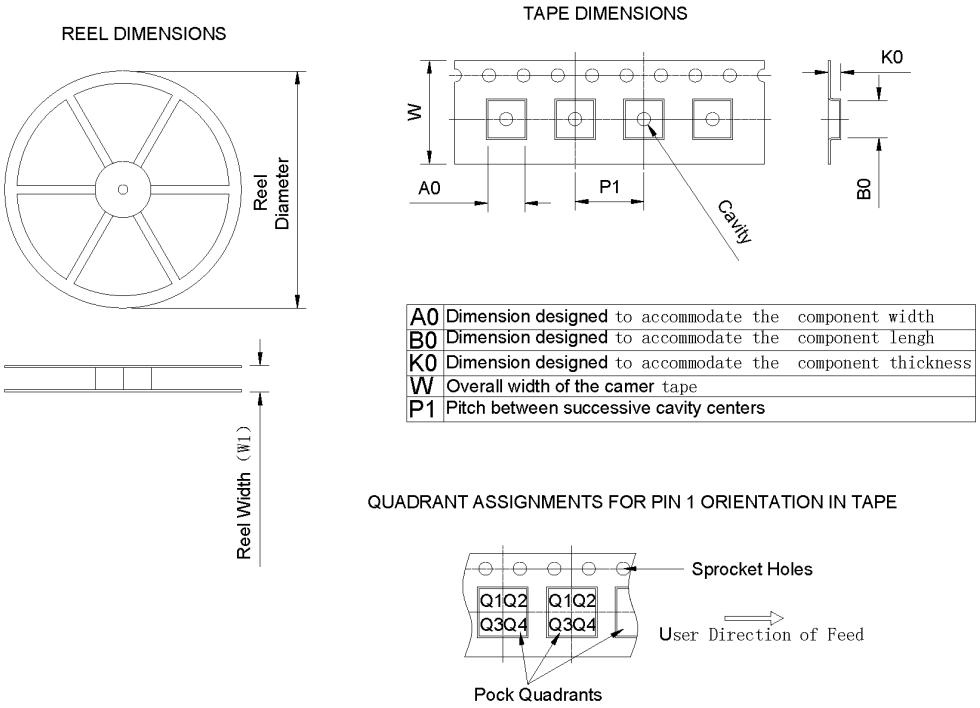
Dimension	Min.	Typ.	Max.
A	4.8	4.9	5.0
A1	0.356	--	0.456
A2	--	1.27	--
A3	--	0.345	--
B	3.8	3.9	4.0
B1	5.8	6.0	6.2
B2	--	5.00	--
C	1.3	--	1.6
C1	0.55	--	0.65
C2	0.55	--	0.65

(Unit: mm)

Dimension	Min.	Typ.	Max.
C3	0.05	--	0.20
C4	0.203	--	0.233
D	--	1.05	--
D1	0.4	--	0.8
R1	--	0.2	--
R2	--	0.2	--
θ1	17°		
θ2	13°		
θ3	0°~8°		
θ4	4°~12°		

(Unit: mm)

10 Package Information



Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	PIN1 Quadrant
XPJ5711-1AFY000N00MA	SOP	8	3000	330±1	12.4±0.2	6.40	5.30	2.10	8.00±0.1	12.00±0.1	Q1

Figure 8. Package information

11 Revision History

Version	Change Contents	Prepared by	Revised Date
V1.0	Released Version		2024.05.24