



To Customer: \_\_\_\_\_

# Realtime Clock Module

**INS5S8563**

## Datasheet

Document Version 1.0

Released on November 16th, 2023

### Ordering Information

Manufacture Part Number	Product Name	Description
INS5S8563-8BSX000N00MA	INS5S8563	SOP8, $\pm 100\text{ppm}$ @-40°C~85°C, $\pm 200\text{ppm}$ @-55°C~125°C
INS5S8563-8BSX000N00AA	INS5S8563	DFN6L, $\pm 100\text{ppm}$ @-40°C~85°C, $\pm 200\text{ppm}$ @-55°C~125°C
INS5S8563-8BSX000N00BA	INS5S8563	FCDFN6L, $\pm 100\text{ppm}$ @-40°C~85°C, $\pm 200\text{ppm}$ @-55°C~125°C
INS5S8563-8BSX000N00DA	INS5S8563	WLCSP, $\pm 100\text{ppm}$ @-40°C~85°C, $\pm 200\text{ppm}$ @-55°C~125°C

## Guangdong Dapu Telecom Technology Co., Ltd

Bldg 5, SSL Modern Enterprise Accelerator Zone, Dongguan City, Guangdong Province, PRC China

TEL:0086-0769-88010888

FAX:0086-0769-81800098



# Index

<b>1</b>	<b>OVERVIEW</b> .....	<b>3</b>
<b>2</b>	<b>BLOCK DIAGRAM</b> .....	<b>3</b>
<b>3</b>	<b>FEATURES</b> .....	<b>3</b>
<b>4</b>	<b>PIN DEFINITION</b> .....	<b>4</b>
<b>5</b>	<b>ELECTRICAL CHARACTERISTICS</b> .....	<b>5</b>
5.1	ABSOLUTE MAXIMUM RATINGS .....	5
5.2	RECOMMENDED OPERATING CONDITIONS.....	5
5.3	FREQUENCY CHARACTERISTICS .....	5
5.4	DC CHARACTERISTICS .....	5
5.5	AC CHARACTERISTICS.....	6
<b>6</b>	<b>REGISTERS</b> .....	<b>7</b>
6.1	REGISTER LISTS .....	7
6.2	DETAILS OF REGISTERS.....	8
6.2.1	<i>Clock counter registers</i> .....	8
6.2.2	<i>Alarm registers</i> .....	9
6.2.3	<i>Timer registers</i> .....	10
6.2.4	<i>CLKOUT control registers</i> .....	10
6.2.5	<i>Timer control registers</i> .....	11
6.2.6	<i>Control register</i> .....	11
<b>7</b>	<b>I<sup>2</sup>C BUS INTERFACE</b> .....	<b>12</b>
7.1	CAUTIONS.....	12
7.2	SLAVE ADDRESS .....	12
7.3	I <sup>2</sup> C BUS PROTOCOL .....	12
7.3.1	<i>Write process</i> .....	12
7.3.2	<i>Read process</i> .....	13
<b>8</b>	<b>REFLOW SOLDERING CURVE</b> .....	<b>14</b>
<b>9</b>	<b>DIMENSIONS AND MARKING</b> .....	<b>15</b>
<b>10</b>	<b>PACKAGE INFORMATION</b> .....	<b>18</b>
	<b>REVISION HISTORY</b> .....	<b>19</b>



# 1 Overview

INS5S8563 is an I<sup>2</sup>C bus interface real-time clock with low power consumption. It supports calendar (year, month, day, hour, minute, second), timer and alarm function. The most important features of this device are ultra-fast start-up and higher resistant to shock and vibration, and it integrates silicon oscillator without fragile crystal. The ultra-small and ultra-thin package makes it suitable to be used in portable electronic devices.

# 2 Block Diagram

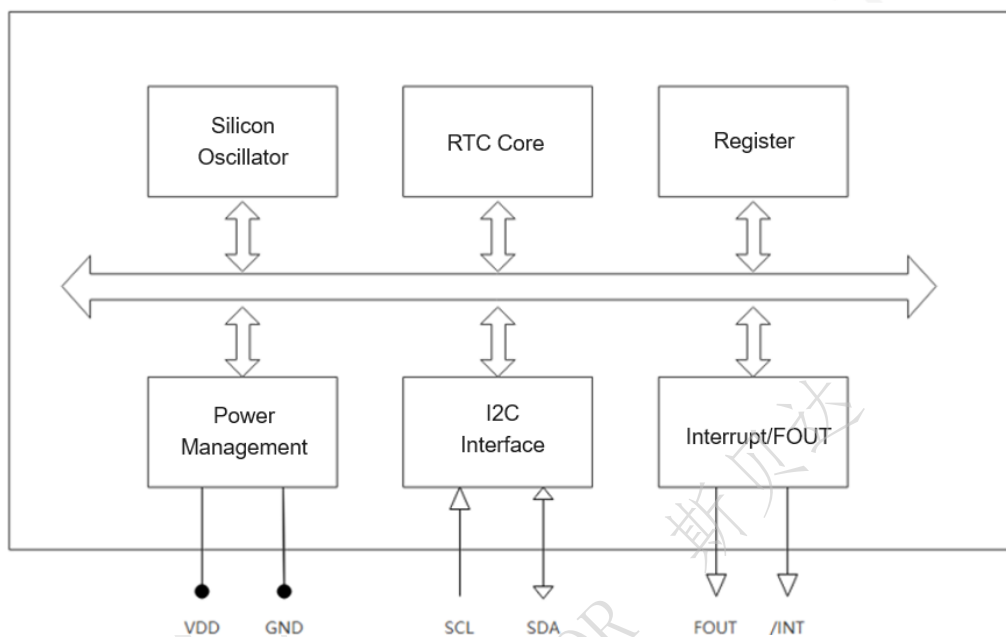


Figure 1. Block Diagram

# 3 Features

- Low Current Consumption: 1.45uA (Typ.)
- Communication Interface: I<sup>2</sup>C bus
- Alarm / Timer Interruption
- Frequency Output
- Ultra-fast start-up (1ms@25°C)
- High resistant to shock and vibration
- Power Supply Voltage: 1.2V ~ 5.5V
- Leap Years Autocorrection
- Operation Temperature Range: -55°C ~ +125°C
- RoHS2.0 & REACH compliant
- Package: 4.9 \* 6.0 \* 1.6mm (SOP8)
- Package: 2.0 \* 2.0 \* 0.75mm (DFN6L)
- Package: 1.2 \* 1.2 \* 0.55mm (FCDFN6L)
- Package: 1.0 \* 0.9mm (WLCSP)



## 4 Pin Definition

SOP8 Pin config	Pin Number	Pin Name	I/O	Description
	1	NC		
	2	NC		
	3	/INT	Out	Alarm、Timer Output. (Open-Drain).
	4	GND	-	Ground
	5	SDA	In/Out	I2C data signal
	6	SCL	In	I2C clock signal
	7	CLKOUT	Out	Frequency Output. (Open-Drain).
	8	VDD	-	Power in
DFN6L Pin config	Pin Number	Pin Name	I/O	Description
	1	/INT2	Out	Alarm、Timer Output. (Open-Drain).
	2	VDD	-	Power in
	3	/INT	Out	Alarm、Timer Output. (Open-Drain).
	4	SDA	In/Out	I2C data signal
	5	SCL	In	I2C clock signal
	6	CLKOUT	Out	Frequency Output. (Open-Drain).
	7	GND	-	Ground
FCDFN6L Pin config	Pin Number	Pin Name	I/O	Description
	1	GND	-	Ground
	2	/INT	Out	Alarm、Timer Output. (Open-Drain).
	3	VDD	-	Power in
	4	CLKOUT	Out	Frequency Output. (Open-Drain).
	5	SCL	In	I2C clock signal
	6	SDA	In/Out	I2C data signal
WLCSP Pin config	Pin Number	Pin Name	I/O	Description
TBD	TBD	TBD	TBD	TBD



## 5 Electrical Characteristics

### 5.1 Absolute Maximum Ratings

**Table1. Absolute Maximum Ratings**

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage	V <sub>DD</sub>	-0.3		6.5	V	
I/O Input Voltage	V <sub>IN</sub>	GND-0.3		6.5	V	SCL, SDA Input
Clock Output Voltage	V <sub>OUT</sub>	GND-0.3		6.5	V	SDA, /INT, /INT2, CLKOUT
Storage Temperature	T <sub>STG</sub>	-55		125	°C	

### 5.2 Recommended Operating Conditions

**Table2. Recommended Operating Conditions**

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage	V <sub>DD</sub>	1.2	3.0	5.5	V	Ensure that the time of supply from 0 to VDD is less than 100ms
Operation Temperature	T <sub>OPR</sub>	-55	25	125	°C	

### 5.3 Frequency Characteristics

**Table3. Oscillator Characteristics**

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Frequency stability	$\Delta f/f$	-200		+200	ppm	-55°C ~ +125°C
		-100		+100	ppm	-40°C ~ +85°C
Oscillation start time	t <sub>STA</sub>		1	5	ms	
Duty cycle	t <sub>w</sub> /t	40	50	60	%	CLKOUT

### 5.4 DC Characteristics

**Table4. DC Characteristics**

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Average Current1	I <sub>DD1</sub>	0.5	1.8	45	uA	V <sub>DD</sub> =5.0V CLKOUT = OFF OR 32KHz, SDA="L", SCL="L"
Average Current2	I <sub>DD2</sub>	0.4	1.45	43		
Low Voltage Detection	VL	1.1	1.3	1.5	V	



Parameter	Symbol	Value			Unit	Notes	
		Min.	Typ.	Max.			
Input High Voltage	V <sub>IH</sub>	0.8*V <sub>DD</sub>		5.5	V	SCL, SDA	
Input Low Voltage	V <sub>IL</sub>	GND		0.2*V <sub>DD</sub>	V		
Output Low Voltage	V <sub>OL1</sub>	GND		GND+0.25	V	VDD =5V, IOL=1mA	/INT
	V <sub>OL2</sub>	GND		GND+0.4		VDD =3V, IOL=1mA	
	V <sub>OL3</sub>	GND		GND+0.5	V	VDD =5V, IOL=1mA	CLKOUT
	V <sub>OL4</sub>	GND		GND+0.3		VDD =3V, IOL=0.5mA	
Input Leak Current	I <sub>LK</sub>	-0.1		0.1	uA	SDA, SCL, V <sub>IN</sub> = V <sub>DD</sub> or GND	
Output Leak Current	I <sub>OZ</sub>	-0.1		0.1	uA	SDA, V <sub>IN</sub> = V <sub>DD</sub> or GND	

## 5.5 AC Characteristics

**Table5. AC Characteristics**

V<sub>DD</sub>=2V ~ 5.5V; Ta=-55°C ~ +125°C

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
SCL clock frequency	f <sub>SCL</sub>			400	kHz
SCL Low Voltage Time	t <sub>LOW</sub>	1.3			us
SCL How Voltage Time	t <sub>HIGH</sub>	0.6			us
Start condition hold time	t <sub>HD; STA</sub>	0.6			us
Start condition setup time	t <sub>SU; STA</sub>	0.6			us
Stop condition setup time	t <sub>SU; STO</sub>	0.6			us
Bus idle time between start condition and stop condition	t <sub>RCV</sub>	1.3			us
Data setup time	t <sub>SU; DAT</sub>	100			ns
Data hold time	t <sub>HD; DAT</sub>	0		0.9	us
SCL, SDA rising time	t <sub>r</sub>			0.3	us
SCL, SDA falling time	t <sub>f</sub>			0.3	us

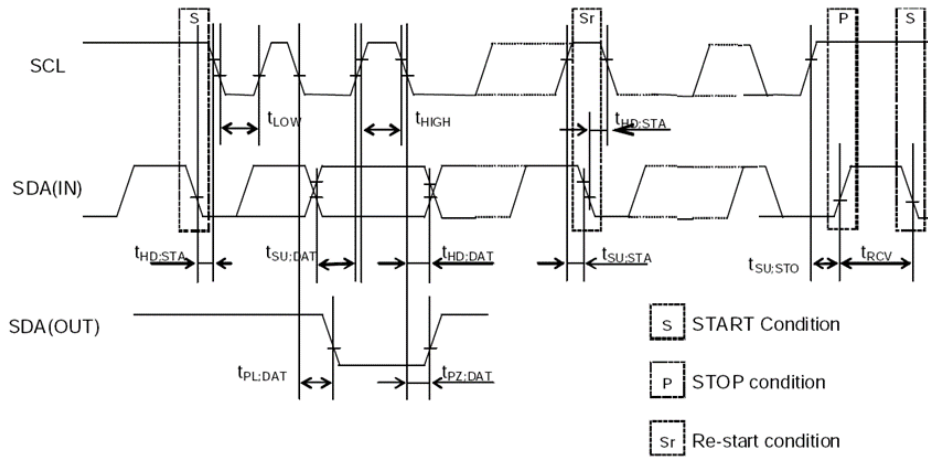


Figure 2. I<sup>2</sup>C bus Timing Chart

Note: When the master device gets access to this slave device through I2C, the whole operation duration should be less than 1s, otherwise it will be reset by the I2C bus through the internal bus overtime function.

## 6 Registers

### 6.1 Register Lists

Address 0x00~0x01: Control and Flag Registers Group

Address 0x02~0x08: Time Register Group

Address 0x09~0x0C: Alarm Register Group

Address 0x0D: CLKOUT Control Register

Address 0x0E~0x0F, 0x12~0x13: Timer Register Group

**Table6. Basic Time and Calendar Registers**

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default Value	R/W
0x00	Control Register_1	EXT_TEST	○	STOP	○	○	○	○	○	0x00	R/W
0x01	Control Register_2	○	○	○	TI_TP	AF	TF	AIE	TIE	0x00	R/W
0x02	SEC	VLF	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				0x80	R/W
0x03	MIN	○	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x00	R/W
0x04	HOUR	○	○	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				0x00	R/W
0x05	DAY	○	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				0x01	R/W
0x06	WEEK	○	○	○	○	○	BCD code, Week ones place, 0-6			0x00	R/W
0x07	MONTH	○	○	○	BCD code, Month tens place, 0-1		BCD code, Month ones place, 0-9			0x00	R/W
0x08	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				0x00	R/W
0x09	MIN Alarm	AE	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x80	R/W
0x0a	HOUR Alarm	AE	○	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				0x80	R/W
0x0b	DAY Alarm	AE	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				0x80	R/W
0x0c	WEEK Alarm	AE	○	○	○	○	BCD code, Week ones place, 0-6			0x80	R/W



0x0d	CLKOUT_Control Register	FE	○	○	○	○	○	FD[1:0]		0x80	R/W
0x0e	Timer_Control Register	TE	○	○	○	○	○	TD[1:0]		0x00	R/W
0x0f	Timer Counter[7:0]	128	64	32	16	8	4	2	1	0x00	R/W
0x12	Timer Counter[23:16]	8388608	4194304	2097152	1048576	524288	262144	131072	65536	0x00	R/W
0x13	Timer Counter[15:8]	32768	16384	8192	4096	2048	1024	512	256	0x00	R/W

Note:

- 1, After power-up reset or in case VLF bit returns “1”, make sure to initialize all registers before using the RTC.
2. The default value of register after power on:  
Initial 0: EXIT\_TEST、STOP、TI\_TP、AF、TF、AIE、TIE、FD[1:0]、TD[1:0]、TE.  
Initial 1: VLF、AE、FE.
3. The bits marked with “○” can be read out “0” after initializing.
4. Only 0 can be written to TF、AF and VLF bits.

## 6.2 Details of Registers

### 6.2.1 Clock counter registers

**Table7. Second、Minute and Hour Registers**

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x02	SEC	VLF	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9			
0x03	MIN	○	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9			
0x04	HOUR	○	○	BCD code, Hour tens place, 0-2		0x00			

SEC: BCD format, Value: 0~59

MIN: BCD format, Value: 0~59

HOUR: BCD format, Value: 0~23

VLF (Voltage Low Flag): Voltage Low Flag, when voltage is lower than VL, this bit will be set to “1”, and keep this value until written to “0” by software.

**Table8. Day Register**

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x05	DAY	○	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9			

DAY: BCD format, the value range will be adjusted automatically according to the month setting and if a leap year or not.

**Table9. DAY Register Value Range**

Month	Day Value Range
1, 3, 5, 7, 8, 10, 12	1~31
4, 6, 9, 11	1~30
February in normal year	1~28
February in leap year	1~29





**Table10. Week Registers**

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x06	WEEK	○	○	○	○	○	BCD code, Week ones place, 0-6		

**Table11. WEEK Register Value table**

	Bit2	Bit1	Bit0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

**Table12. Month and Year Register**

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x07	MONTH	○	○	○	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9			
0x08	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9			

MONTH: BCD format, Value1~12

YEAR: BCD format, Value01~99(2001~2099)

Example: 2023/01/01 Wednesday 21:18:36

**Table13. Example of time setting**

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x02	SEC	○	0	1	1	0	1	1	0
0x03	MIN	○	0	0	1	1	0	0	0
0x04	HOUR	○	○	1	0	0	0	0	1
0x05	WEEK	○	0	0	0	0	0	1	1
0x06	DAY	○	○	0	0	0	0	0	1
0x07	MONTH	○	○	○	0	0	0	0	1
0x08	YEAR	0	0	1	0	0	0	1	1

6.2.2 Alarm registers

**Table14. Alarm Register**

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x01	Control Register_2	○	○	○	TI_TP	AF	TF	AIE	TIE
0x09	MIN Alarm	AE	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9			
0x0a	HOUR Alarm	AE	○	BCD code, Hour tens		BCD code, Hour ones place, 0-9			



Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
				place, 0-2					
0x0b	DAY Alarm	AE	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9			
0x0c	WEEK Alarm	AE	○	○	○	○	BCD code, Week ones place, 0-6		

Alarm interruption can be generated with the setting of these registers and the cooperation of AIE and AF.

AE (Alarm Enable): Alarm Enable bit, 0-Enable; 1-Disable.

AF function refer to 0x01 register bit3.

AIE function refer to 0x01 register bit1.

### 6.2.3 Timer registers

**Table15. Timer Register**

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x01	Control Register_2	○	○	○	TI_TP	AF	TF	AIE	TIE
0x0e	Timer_Control Register	TE	○	○	○	○	○	TD[1]	TD[0]
0x0f	Timer Counter[7:0]	128	64	32	16	8	4	2	1
0x12	Timer Counter[23:16]	8388608	4194304	2097152	1048576	524288	262144	131072	65536
0x13	Timer Counter[15:8]	32768	16384	8192	4096	2048	1024	512	256

Timer interruption can be generated with the setting of these registers and the cooperation of TE、TF 、TIE and TD[1:0].

TE function refer to 0x0e register bit7.

TF function refer to 0x01 register bit2.

TIE function refer to 0x01 register bit0.

TD[1:0] function refer to 0x0e register bit1 and bit0.

### 6.2.4 CLKOUT control registers

**Table16. CLKOUT Control Register**

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x0D	CLKOUT_Control Register	FE	○	○	○	○	○	FD[1]	FD[0]

Used for the CLKOUT Frequency function.

FE (CLKOUT Enable): 0- Disable CLKOUT Frequency function, 1-Enable CLKOUT Frequency function。

FD[1], FD[0] to config the output frequency. Shown as below table:

**Table17. FD Table**

FD [1]	FD [0]	CLKOUT Frequency
0	0	32768Hz Output
0	1	1024Hz output
1	0	32Hz output
1	1	1Hz Output



6.2.5 Timer control registers

**Table18. Timer Control Register**

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x0E	Timer_Control Register	TE	○	○	○	○	○	TD[1]	TD[0]

Used for the specified functions, including Time Update Interruption.

TE (Timer Enable): 0- Disable Timer Interrupt function, 1-Enable Timer Interrupt function。

TD[1], TD[0]: Timer/Counter Clock configuration bits, just as below table:

**Table19. TD Table**

TD [1]	TD [0]	Timer/Counter Clock	Interruption duration
0	0	4096Hz (244.14us)	122uS
0	1	64Hz (15.625ms)	7.813mS
1	0	1Hz (Second)	7.813mS
1	1	1/60Hz (Min)	7.813mS

6.2.6 Control register

**Table20. Control Register**

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x00	Control Register_1	EXT_TEST	○	STOP	○	○	○	○	○
0x01	Control Register_2	○	○	○	TI_TP	AF	TF	AIE	TIE

EXT\_TEST: 1: Test Mode, 0: Normal Mode.

STOP: 1: RTC Clock is Stop, 0: RTC Clock is normal.

AF(Alarm Flag): Alarm Flag, when Alarm Interruption generation, this bit will change from “0”to “1”,and keep this value until written to “0” by software;

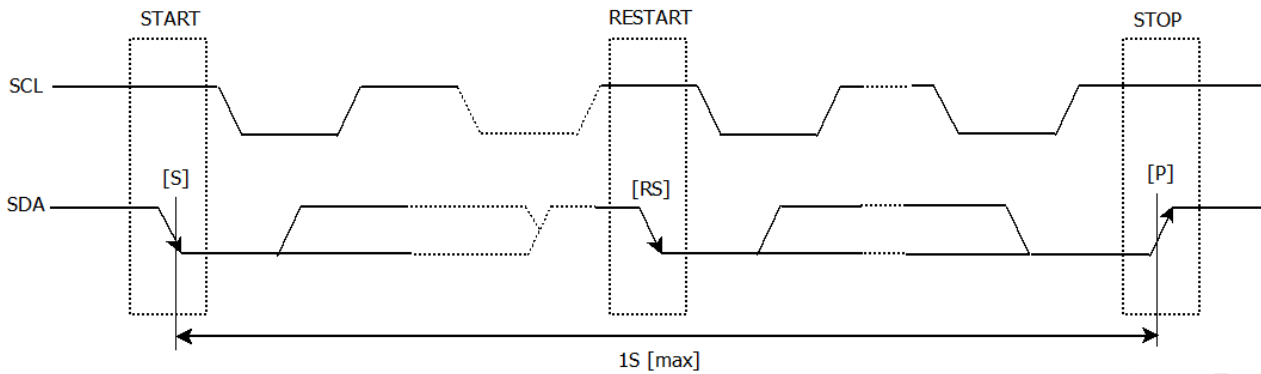
TF (Timer Flag): Timer Flag, when timer interruption generates, this bit will change from “0”to “1”,and keep this value until written to “0” by software;

AIE(Alarm Interrupt Enable): When AF changes from“0”to“1”, this bit can control if the interruption generates or not. 0-Did not generate(/INT maintain high resistance), 1-generate the interruption(/INT changes from high resistance to low voltage)。

TIE(Timer Interrupt Enable): When TF changes from“0”to“1”, this bit can control if the interruption generates or not. 0-Did not generate(/INT maintain high resistance), 1-generate the interruption(/INT changes from high resistance to low voltage)。



## 7 I<sup>2</sup>C Bus Interface



I2C bus supports bi-directional communications through a serial clock line SCL and a serial data line SDA. I2C bus device can be defined as “Master” and “Slave”. INS5S8563 can only be used as Slave.

### 7.1 Cautions

I2C bus includes START, RESTART, STOP conditions, the duration between START and STOP must be less than 1 second just in case the bus to be set to standby mode automatically. If the time is more than 1s, INS5S8563 will reset I2C Interface.

INS5S8563 I2C bus interface supports single byte read/write operations as well as multiple bytes incremental access. After 0xFF address, the next one will be 0x00.

### 7.2 Slave Address

**Table21. I<sup>2</sup>C Bus Slave Address**

Transfer data	Slave address							R/W
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A3h (Read)	1	0	1	0	0	0	1	1 (Read)
A2h (Write)								0 (Write)

INS5S8563 I2C bus Slave Address is [1010 001\*].

### 7.3 I<sup>2</sup>C bus protocol

It is assumed CPU is master and INS5S8563 is slave in this section.

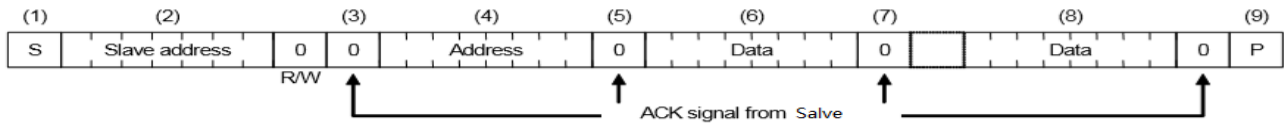
#### 7.3.1 Write process

I2C bus includes an address auto-increment function, once the initial address has been specified, the INS5S8563 increments (+1) the address automatically after each data is sent, then to write next data.

- (1) CPU sends start condition[S]
- (2) CPU sends INS5S8563's slave address with R/W bit to set to write mode
- (3) CPU verifies ACK signal from INS5S8563
- (4) CPU sends write address to INS5S8563
- (5) CPU verifies ACK signal from INS5S8563
- (6) CPU sends write data to the address specified at step (4)
- (7) CPU verifies ACK signal from INS5S8563



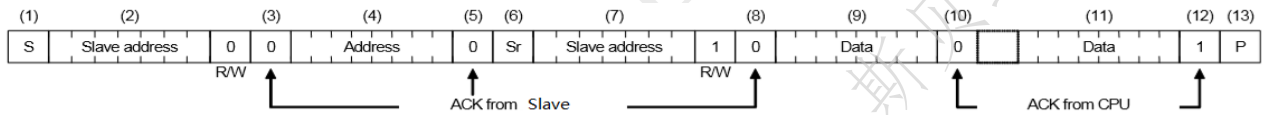
- (8) Repeat (6) (7) if multiple bytes need to be written, address will be incremented automatically
- (9) CPU ends stop condition[P]



### 7.3.2 Read process

Writing the address to be read with write mode firstly, then reading the data with read mode.

- (1) CPU sends start condition[S]
- (2) CPU sends INS5S8563's slave address with R/W bit to set to write mode
- (3) CPU verifies ACK signal from INS5S8563
- (4) CPU sends address for reading from INS5S8563
- (5) CPU verifies ACK signal from INS5S8563
- (6) CPU sends RESTART condition [Sr]
- (7) CPU sends INS5S8563's slave address with R/W bit to set to read mode
- (8) CPU verifies ACK signal from INS5S8563
- (9) CPU reads data from the specified address in step (4)
- (10) CPU sends ACK signal for "0"
- (11) Repeat (9) (10) if multiple bytes need to be read, address will be incremented automatically
- (12) CPU sends ACK signal for "1"
- (13) CPU sends stop condition[P]





## 8 Reflow Soldering Curve

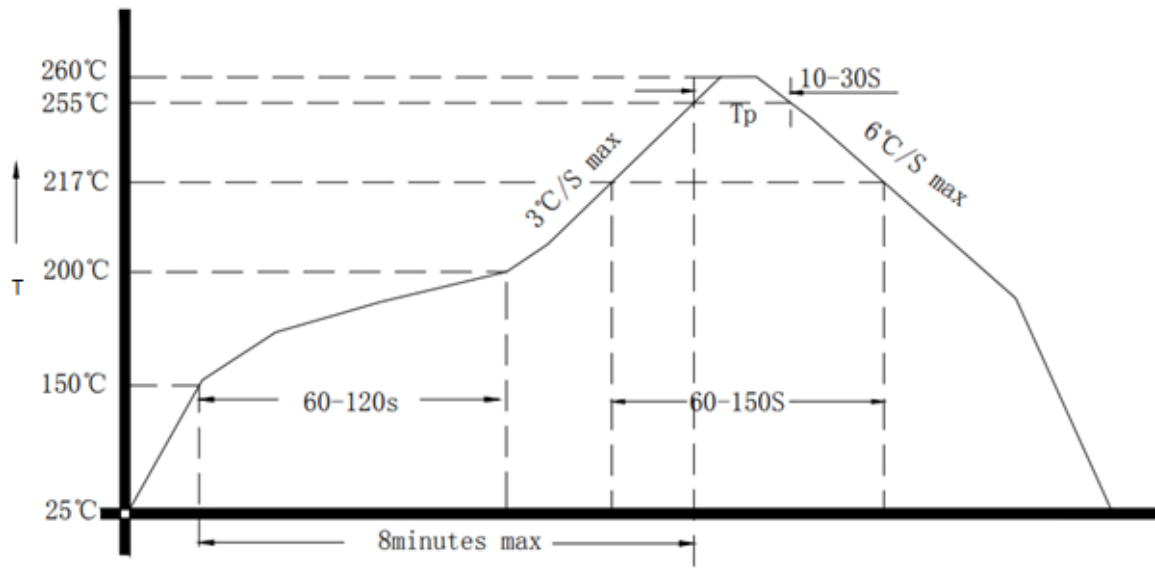


Figure 3. Reflow Soldering Curve

Note:

1. Standard: IPC/JEDEC J-STD-020
2. It is suggested to solder IC under the condition shown in the curve above. Must pay attention to the temperature and time when manual soldering.



## 9 Dimensions and Marking

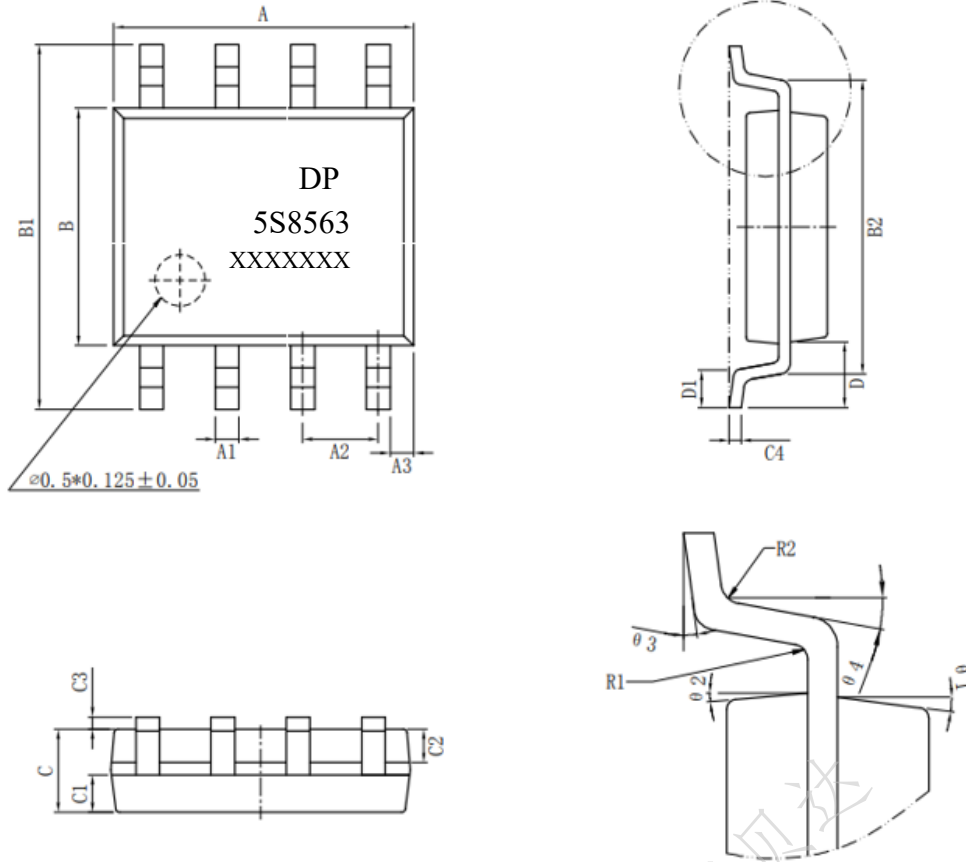


Figure 4. SOP8 Dimension

Dimension/mm	Min.	Typ.	Max.
A	4.8	4.9	5.0
A1	0.356	--	0.456
A2	--	1.27	--
A3	--	0.345	--
B	3.8	3.9	4.0
B1	5.8	6.0	6.2
B2	--	5.00	--
C	1.3	--	1.6
C1	0.55	--	0.65
C2	0.55	--	0.65

Dimension/mm	Min.	Typ.	Max.
C3	0.05	--	0.20
C4	0.203	--	0.233
D	--	1.05	--
D1	0.4	--	0.8
R1	--	0.2	--
R2	--	0.2	--
theta 1	17°		
theta 2	13°		
theta 3	0°~8°		
theta 4	4°~12°		

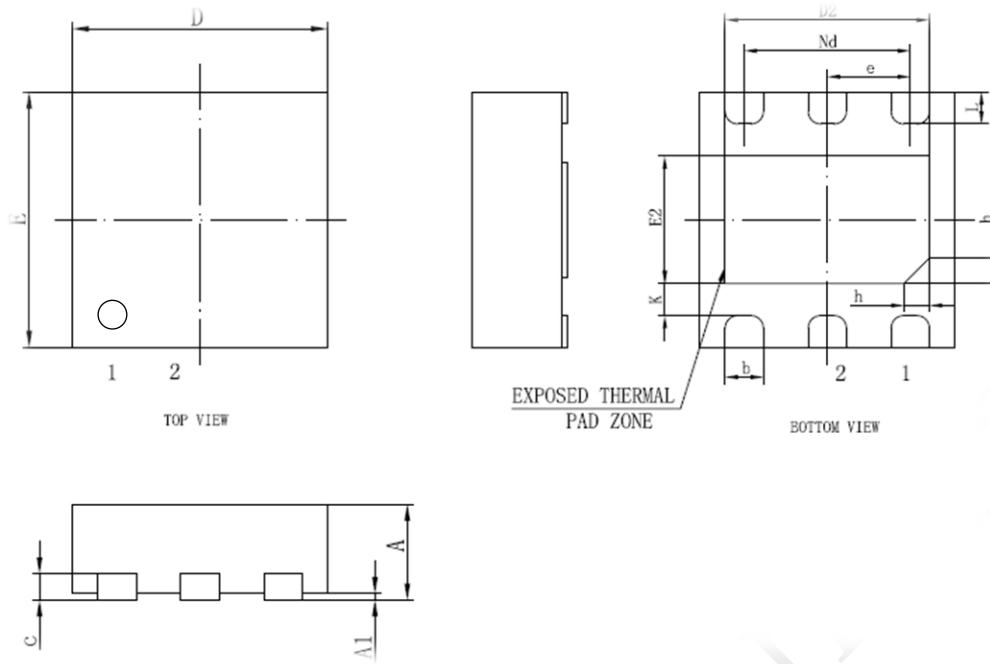


Figure 5. DFN6L Dimension

Dimension/mm	Min.	Typ.	Max.
A	0.7	0.75	0.8
A1	0	0.02	0.05
b	0.25	0.3	0.35
c	0.18	0.2	0.25
D	1.9	2.0	2.1
D2	1.5	1.6	1.7
e	0.65BSC		

Dimension/mm	Min.	Typ.	Max.
Nd	1.3BSC		
E	1.9	2.0	2.1
E2	0.9	1.0	1.1
K	0.2	-	-
L	0.2	0.25	0.3
h	0.15	0.2	0.25
L/F 载体尺寸 (MIL)	69*47		



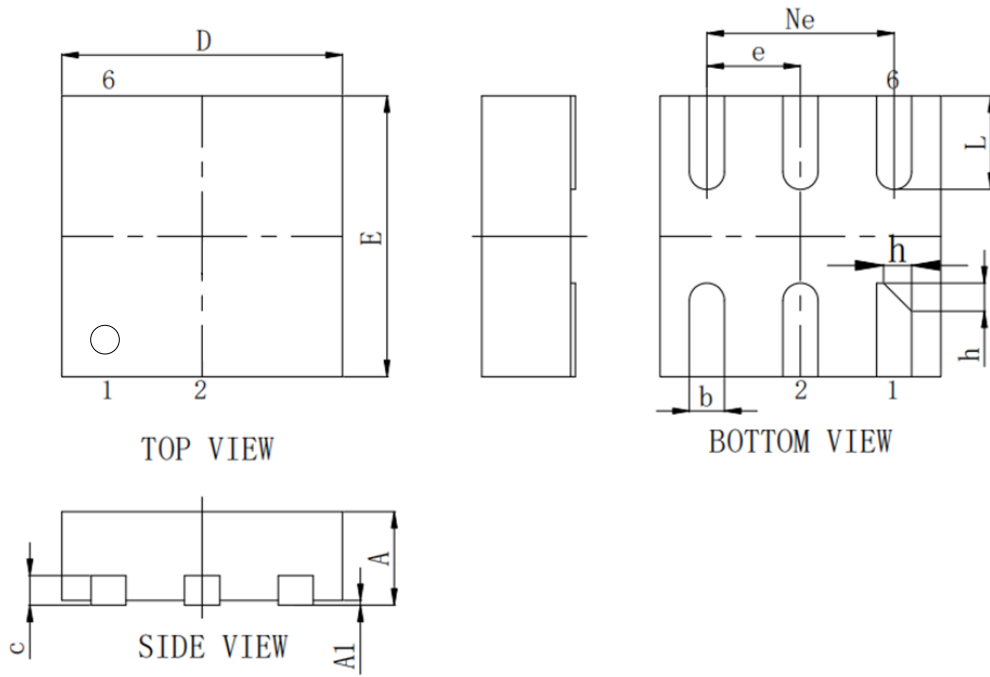


Figure 6. FCDFN6L Dimension

Dimension/mm	Min.	Typ.	Max.
A	0.5	0.55	0.6
A1	0	0.02	0.05
b	0.15	0.2	0.25
c	0.152REF		
D	1.1	1.2	1.3

Dimension/mm	Min.	Typ.	Max.
e	0.40BSC		
Ne	0.80BSC		
E	1.1	1.2	1.3
L	0.3	0.4	0.5
h	0.1	0.15	0.2



# 10 Package Information

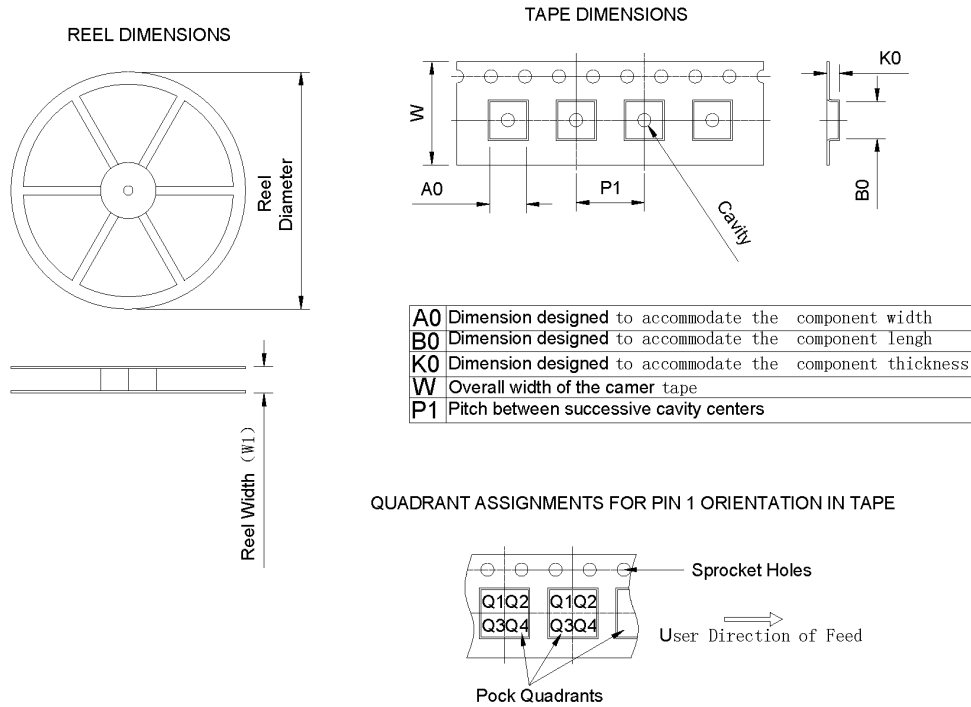


Figure 7. SOP8 Package information

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	PIN1 Quad rant
INS5S8563-8BSX000N00MA	SOP8	8	3000	330±1	12.4±0.2	6.40	5.30	2.10	8.00±0.1	12.00±0.1	Q1



### Revision History

Version	Change Contents	Prepared by	Revised Date
V1.0	First Issued	LIN Jianhua	2023.11.16

DAPU Confidential FOR 斯贝达