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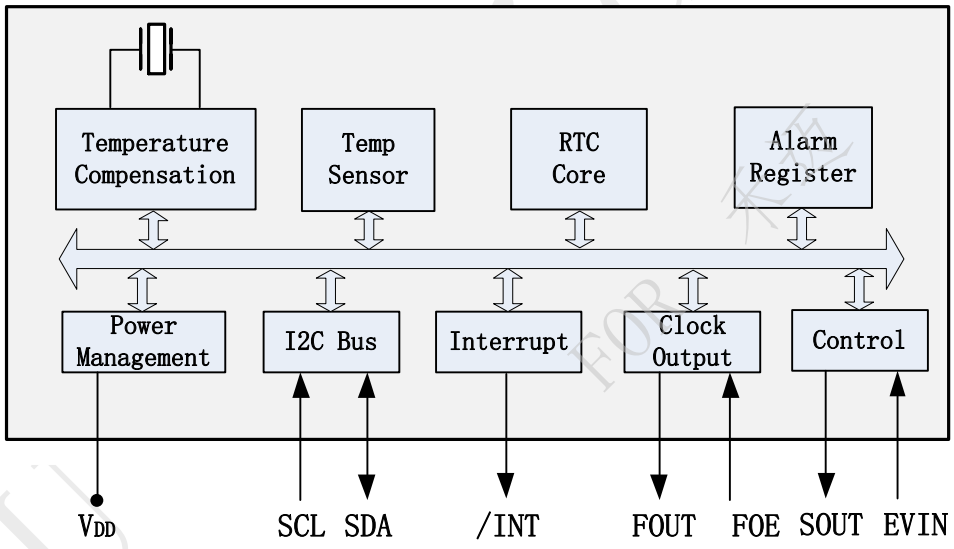
INS5A8804—Automotive High Accuracy I²C RTC

Key Features

- Low current consumption: 1.8uA (Typ.)
- High stability:
  - ±5ppm @ -40℃~+90℃
  - ±20ppm@ +90℃~+105℃
- Build-in TCXO: 32.768KHz
- Build-in temperature sensor
- Communication Interface: I²C bus
- Power Supply Voltage:1.6V~5.5V
- Operation Temperature Range: -40℃~+105℃
- Leap years autocorrection
- Time stamp trigger function
- Timer output function with adjustable period
- Package: 3.2mm × 2.5mm × 0.9mm
- AEC-Q100 Compliant
- RoHS2.0 & REACH compliant

Block Diagram



Overview

INS5A8804 is a high-accuracy I²C bus interface real-time clock with low power consumption. It embeds a 32.768KHz TCXO. The high precise temperature sensor and temperature compensated circuit ensure the high clock accuracy. It supports calendar (year, month, day, hour, minute, second), clock and timer functions etc. The SMD3225 package with only 0.9mm thickness and AEC-Q100 compliant makes it suitable for automotive applications.

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1 Overview

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2 Block Diagram

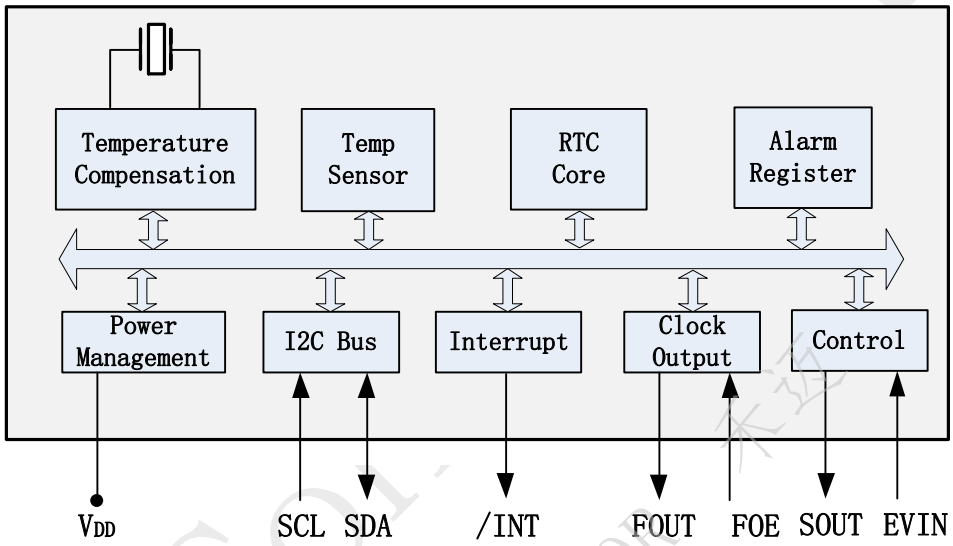

Figure 1. Block Diagram

3 Features

- Low current consumption: 1.8uA (Typ.)
- High stability:
  ±5ppm @ -40℃~ +90℃
  ±20ppm@ +90℃~ +105℃
- Communication Interface: I2C bus
- Build-in TCXO: 32.768KHz
- Build-in temperature sensor
- Power Supply Voltage:1.6V~5.5V
- Operation Temperature Range: -40℃~+105℃
- Leap years autocorrection
- Time stamp trigger function
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- Package: 3.2mm × 2.5mm × 0.9mm
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4 Pin definition

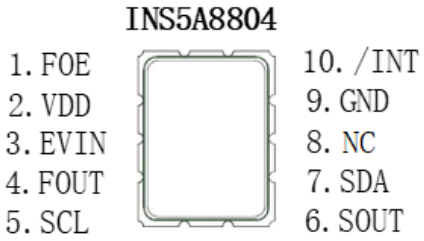

Table1. Pin Definition

Pin Number	Pin Name	I/O	Description
1	FOE	In	FOUT output control pin. “1”- enable FOUT, “0”-FOUT Hi-Z, build-in pull down resistor(Typ:500KΩ).
2	V_{DD}	-	Power supply
3	EVIN	In	Trigger input terminal for time stamps.
4	FOUT	Out	Frequency output. Controlled by FOE. Frequency can be set by FSEL bits.
5	SCL	In	I^2C clock signal
6	SOUT	Out	SOUT is the inside state output (CMOS output). SOUT outputs state of a specified flag bit or programmed logical 1 or 0
7	SDA	In/Out	I^2C data signal
8	NC	-	
9	GND	-	Ground
10	/INT	Out	Interrupt Output, Open-Drain

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5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table2. Absolute Maximum Ratings

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage	V_{DD}	-0.3		6.5	V	
Input Voltage	V_{IN}	GND-0.3		6.5	V	FOE, SCL, SDA, EVIN
Output Voltage	V_{OUT1}	GND-0.3		V_{DD}+0.3	V	FOUT, SOUT
	V_{OUT2}	GND-0.3		6.5	V	SDA, /INT
Storage temperature	T_{STG}	-55		125	℃	

5.2 Recommended Operating Conditions

Table3. Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage	V_{DD}	1.6	3.0	5.5	V	
Current consumption	I_{DD}		1.8		uA	@25℃, VDD=3V
Operation temperature	T_{OPR}	-40	25	105	℃	

Note 1: During the power on and oscillation starting time, a voltage of more than 2.5V must be provided to ensure the oscillation circuit to a stable state.

Note2：After the power supply is removed or power off, ensure that VDD=GND for more than 10 seconds before next power on cycle.

Note3: If there is no special indication, the test conditions are GND =0V, VDD=1.6V~5.5V, Ta=-40℃~+105℃

5.3 Frequency Characteristics

Table4. Frequency Characteristics

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Frequency stability	Δf/f	-5		+5	ppm	-40℃~+90℃
Frequency stability	Δf/f	-20		+20	ppm	+90℃~+105℃
Oscillation start time	t_{STA}			1	s	@25℃, VDD=3V
Year Aging	f_a	-5		+5	ppm	@25℃, First year
FOUT duty cycle	$t_{w/t}$	40	50	60	%	

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5.4 DC Characteristics

Table5. DC Characteristics

Parameter	Symbol	Value			Unit	Notes	
		Min.	Typ.	Max.			
Average Current consumption1	I_{DD1}		1.9	26	uA	V_{DD}=5.0V	f_{SCL}=0Hz, FOE=GND, /INT = V_{DD}; FOUT off (High-Z); Compensation interval 2s;
Average Current consumption2	I_{DD2}		1.8	25		V_{DD}=3.0V	
Average Current consumption3	I_{DD3}		4.8	30	uA	V_{DD}=5.0V	f_{SCL}=0Hz, FOE=V_{DD}, /INT = V_{DD}; FOUT:32.768kHz, CL=0pF; Compensation interval 2s;
Average Current consumption4	I_{DD4}		2.8	28		V_{DD}=3.0V	
Average Current consumption5	I_{DD5}		10	35	uA	V_{DD}=5.0V	f_{SCL}=0Hz, / INT = Hi-Z, FOUT outputs 32 kHz, CL = 30 pF, Temp compensation interval 2.0 s
Average Current consumption6	I_{DD6}		6	28		V_{DD}=3.0V	
Average Current consumption7	I_{DD7}		1.85	24	uA	V_{DD}=5.0V	f_{SCL}=0Hz, / INT = Hi-Z, FOUT is stopped, Temp compensation is stopped.
Average Current consumption8	I_{DD8}		1.75	23		V_{DD}=3.0V	
Peak Current consumption (1)	I_{DD9}		55	95	uA	V_{DD}=5.0V	f_{SCL}=0Hz, / INT = VDD, FOUT is stopped, Temp compensation ON (peak)
Peak Current consumption (2)	I_{DD10}		50	90		V_{DD}=3.0V	
Low Voltage Detection	VLF	1	1.3	1.5	V		
High-level input voltage	V_{IH}	0.8*V_{DD}		V_{DD}	V	SCL, SDA, FOE, EVIN	
Low-level input voltage	V_{IL}	GND-0.3		0.2*V_{DD}	V		
High-level output voltage	V_{OH1}	4.0		5.0	V	V_{DD}=5.0V, I_{OH} = -1mA	FOUT, SOUT
	V_{OH2}	2.2		3.0		V_{DD}=3.0V, I_{OH} = -1mA	
	V_{OH3}	2.9		3.0		V_{DD}=3.0V, I_{OH} = -100uA	
Low-level output voltage	V_{OL1}	GND		GND+0.5	V	V_{DD}=5.0V, I_{OL} = 1mA	FOUT, SOUT
	V_{OL2}	GND		GND+0.8		V_{DD}=3.0V, I_{OL} = 1mA	
	V_{OL3}	GND		GND+0.1		V_{DD}=3.0V, I_{OL} = 100uA	
	V_{OL4}	GND		GND+0.25		V_{DD}=5.0V, I_{OL} = 1mA	

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Parameter	Symbol	Value			Unit	Notes	
		Min.	Typ.	Max.			
	V_{OL5}	GND		GND+0.4	V	V_{DD}=3.0V, I_{OL} = 1mA	/INT
	V_{OL6}	GND		GND+0.4	V	V_{DD}≥3.0V, I_{OL} = 3mA	SDA
Input leakage current	I_{LK}	-0.5		0.5	uA	FOE, SDA, SCL, EVIN, V_{IN} = V_{DD} or GND	
Output leakage current	I_{OZ}	-0.5		0.5	uA	FOUT, SDA, /INT, SOUT, V_{IN} = V_{DD} or GND	

Note: If there is no special indication, the test conditions are GND=0V, VDD=1.6V~5.5V, Ta=-40°C~+105°C.

5.5 AC Characteristics

Table6. AC Characteristics

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}			400	kHz
SCL low level time	t_{LOW}	1.3			us
SCL high level time	t_{HIGH}	0.6			us
Start condition setup time	$t_{HD;STA}$	0.6			us
Start condition hold time	$t_{SU;STA}$	0.6			us
Stop condition setup time	$t_{SU;STO}$	0.6			us
Bus idle time between start condition and stop condition	t_{RCV}	1.3			us
Data setup time	$t_{SU;DAT}$	100			ns
Data hold time	$t_{HD;DAT}$	0			us
SCL, SDA rising time	t_r			0.3	us
SCL, SDA falling time	t_f			0.3	us

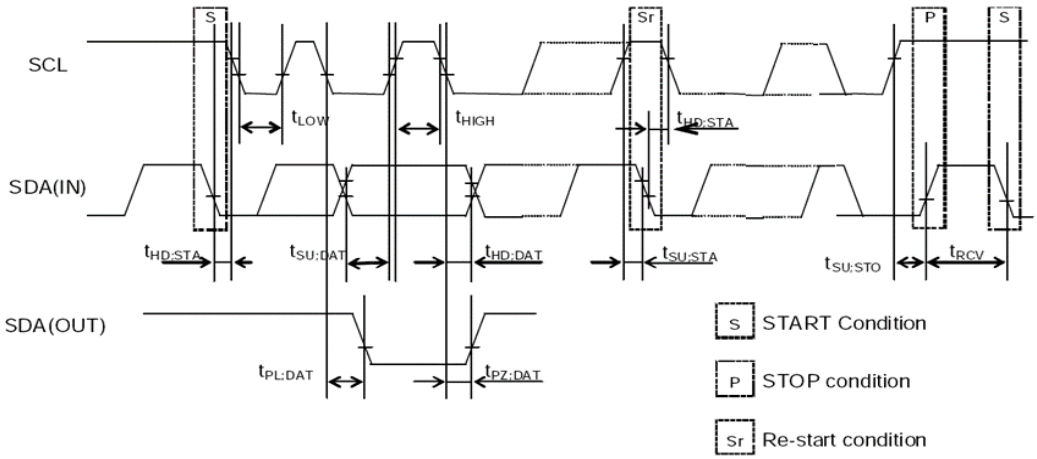

Figure 2. I^2C bus Timing Chart

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Note: when the master equipment accesses the equipment through I2C bus, all communication from sending start condition to sending stop shall be completed within 1 second. If it exceeds 1 second, the I2C bus interface will be reset through the internal bus timeout function.

6 Registers

6.1 Register Lists

Address 0x00~0x0F: Basic Time and Calendar Registers

Address 0x10~0x1F: Extended Registers

Address 0x20: ID Registers

Table7. Basic Time and Calendar Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x00	SEC	○	Second ten's place, 0-5			Second unit's place, 0-9				R/W
0x01	MIN	○	Minute ten's place, 0-5			Minute unit's place, 0-9				R/W
0x02	HOUR	○	○	Hour ten's place, 0-2		Hour unit's place, 0-9				R/W
0x03	WEEK	○	6	5	4	3	2	1	0	R/W
0x04	DAY	○	○	Day ten's place, 0-3		Day unit's place, 0-9				R/W
0x05	MONTH	○	○	○	Month ten's place, 0-1	Month unit's place, 0-9				R/W
0x06	YEAR	Year ten's place, 0-9				Year unit's place, 0-9				R/W
0x07	RAM	●	●	●	●	●	●	●	●	R/W
0x08	MIN Alarm	AE	Minute ten's place, 0-5			Minute unit's place, 0-9				R/W
0x09	HOUR Alarm	AE	●	Hour ten's place, 0-2		Hour unit's place, 0-9				R/W
0x0A	WEEK Alarm	AE	6	5	4	3	2	1	0	R/W
	DAY Alarm		●	Day ten's place, 0-3		Day unit's place, 0-9				R/W
0x0B	Timer Counter 0	128	64	32	16	8	4	2	1	R/W
0x0C	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256	R/W
0x0D	Control 1	TEST	WADA	USEL	TE	FSEL [1]	FSEL [0]	TSEL [1]	TSEL [0]	R/W
0x0E	Flag Register	○	○	UF	TF	AF	○	VLF	RSV	R/W
0x0F	Control 2	CSEL [1]	CSEL [0]	UIE	TIE	AIE	○	○	RESET	R/W

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Table8. Extended Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x10	Time Stamp SEC	○	Second ten's place, 0-5			Second unit's place, 0-9				R
0x11	Time Stamp MIN	○	Minute ten's place, 0-5			Minute unit's place, 0-9				R
0x12	Time Stamp HOUR	○	○	Hour ten's place, 0-2		Hour unit's place, 0-9				R
0x13	Time Stamp WEEK	○	6	5	4	3	2	1	0	R
0x14	Time Stamp DAY	○	○	Day ten's place, 0-3		Day unit's place, 0-9				R
0x15	Time Stamp MONTH	TSVLF	RSV	○	Month ten's place, 0-1	Month unit's place, 0-9				R
0x16	Time Stamp YEAR	Year ten's place, 0-9				Year unit's place, 0-9				R
0x17	EVIN set	ECP	EHL	EPU	RCE	EIE	○	ET[1]	ET[0]	R/W
0x18	EVIN det	EF	○	○	○	EVMON	○	○	○	R/W
0x19	SOUT config1	SOE[7]	SOE[6]	SOE[5]	SOE[4]	SOE[3]	SOE[2]	SOE[1]	SOE[0]	R/W
0x1A	SOUT config2	DCE	DC	○	○	SRV	FS[2]	FS[1]	FS[0]	R/W
0x1B	Timer set	TSTP	TRES	○	○	○	○	○	○	R/W
0x1C	Timer0	128	64	32	16	8	4	2	1	R
0x1D	Timer1	32768	16384	8192	4096	2048	1024	512	256	R
0x1E	Timer2	8388608	4194304	2097152	1048576	524288	262144	131072	65536	R
0x1F	Timer counter 2	8388608	4194304	2097152	1048576	524288	262144	131072	65536	R/W

Table9. ID Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x20	ID	Vendor ID[3:0]				Version[3:0]				R

Note:

1, After power-up reset or in case VLF bit returns "1", make sure to initialize all registers to default state before using the RTC. Ensure all inputs

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are in the required range and the defined values are set for the reserved bits in case the clock cannot work normally.

- ✓ During the initial power-up, below bits will be in the state as below:

  Initial 0: TEST, WADA, USEL, TE, FSEL[1:0], TSEL[0], UF, TF, AF, EF,CSEL[1], UIE, TIE, AIE, RESET, TSVLF, ECP, EHL, EPU, RCE, EIE, ET[1:0], EVMON, SOE[7:0], DCE, DC, SRV, FS[2:0], TRES, TSTP, All bits of address 1Fh.

  Initial 1: TSEL[1], VLF, CSEL[0], All bits of address 1Ch,1Dh,1Eh.
- ✓ All other register values are undefined, so make sure to reset the module before using it.
- ✓ The bits marked with "○"can be read out "0" only after initializing.
- ✓ The bits marked with "●" are RAM bits which can be used to write or read any data.
- ✓ Only 0 can be written to UF, TF, AF, VLF bits.
- ✓ Make sure "0" to be written for TEST bits which are used for testing only.
- ✓ Forbidden to modify the register except 6.1 register list and RSV register.

6.2Details of Registers

6.2.1 Clock counter registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x00	SEC	○	BCD code, Second ten's place, 0-5			BCD code, Second unit's place, 0-9				0x00
0x01	MIN	○	BCD code, Minute ten's place, 0-5			BCD code, Minute unit's place, 0-9				0x00
0x02	HOUR	○	○	BCD code, Hour ten's place, 0-2		BCD code, Hour unit's place, 0-9				0x00

SEC: BCD format, Value: 0~59

MIN: BCD format, Value: 0~59

HOUR: BCD format, Value: 0~23

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x03	WEEK	○	6	5	4	3	2	1	0	0x40

WEEK:Value01h, 02h, 04h, 08h, 10h, 20h, 40h. Only one bit can be set to 1 each time, all others must be set to 0.

Table10. WEEK Register

WEEK	Data	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sunday	01h	0	0	0	0	0	0	0	1
Monday	02h	0	0	0	0	0	0	1	0
Tuesday	04h	0	0	0	0	0	1	0	0

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WEEK	Data	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Wednesday	08h	0	0	0	0	1	0	0	0
Thursday	10h	0	0	0	1	0	0	0	0
Friday	20h	0	0	1	0	0	0	0	0
Saturday	40h	0	1	0	0	0	0	0	0

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x04	DAY	○	○	BCD code, Day ten's place, 0-3		BCD code, Day unit's place, 0-9				0x01

DAY: BCD format, the value range will be adjusted automatically according to the month setting and if a leap year or not .

Table11. DAY Register Value

Month	Day Value Range
1, 3, 5, 7, 8, 10, 12	1~31
4, 6, 9, 11	1~30
February in normal year	1~28
February in leap year	1~29

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x05	MONTH	○	○	○	BCD code, Month ten's place, 0-1	BCD code, Month unit's place, 0-9				0x01
0x06	YEAR	BCD code, Year ten's place, 0-9				BCD code, Year unit's place, 0-9				0x00

MONTH: BCD format, Value1~12

YEAR: BCD format, Value0~99(2000~2099)

Example: 2020/01/01 Wednesday 21:18:36

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x00	SEC	○	0	1	1	0	1	1	0
0x01	MIN	○	0	0	1	1	0	0	0
0x02	HOUR	○	○	1	0	0	0	0	1
0x03	WEEK	○	0	0	0	1	0	0	0
0x04	DAY	○	○	0	0	0	0	0	1
0x05	MONTH	○	○	○	0	0	0	0	1
0x06	YEAR	0	0	1	0	0	0	0	0

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6.2.2 Alarm registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x08	MIN Alarm	AE	BCD code, Minute ten's place, 0-5			BCD code, Minute unit's place, 0-9				0x00
0x09	HOUR Alarm	AE	●	BCD code, Hour ten's place, 0-2		BCD code, Minute unit's place, 0-9				0x00
0x0A	WEEK Alarm	AE	6	5	4	3	2	1	0	0x00
	DAY Alarm		●	BCD code, Day ten's place, 0-3		BCD code, Day unit's place, 0-9				

According to AIE, AF, WADA bits setting, the alarm interrupt will be generated once the current time match the settings in the above registers, the /INT pin goes to low level and AF bit is set to '1' to record an alarm interrupt event has occurred.

WEEK Alarm/DAY Alarm: Controlled by WADA bit in 0x0D register

AE: Alarm Enable bit, 0-enable; 1-disenable

AF: Defined in 0x0E register bit3

AIE: Defined in 0x0F register bit3

6.2.3 Timer control registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0B	Timer Counter 0	128	64	32	16	8	4	2	1	0x00
0x0C	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256	0x00
0x1B	Timer set	TSTP	TRES	○	○	○	○	○	○	0x00
0x1C	Timer0	128	64	32	16	8	4	2	1	0xFF
0x1D	Timer1	32768	16384	8192	4096	2048	1024	512	256	0xFF
0x1E	Timer2	8388608	4194304	2097152	1048576	524288	262144	131072	65536	0xFF
0x1F	Timer Counter 2	8388608	4194304	2097152	1048576	524288	262144	131072	65536	0x00

According to TE, TF, TIE, TSEL[1:0] bits setting, a timer interrupt will be generated once the value countdowns to 0 from the one set in the above Timer Counter registers.

TE: Defined in 0x0D register bit4

TF: Defined in 0x0E register bit4

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TIE: Defined in 0x0F register bit4

TSEL[1:0]:Defined in 0x0D register bit1 and bit0

TSTP： 0: Timer counter are continued

1: Stop the timer counter

TRES: Timer counter reset control

0: Timer counter do not reset

1: Timer counter reset to default value

6.2.4 Control registers 1

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0D	Control 1	TEST	WADA	USEL	TE	FSEL[1]	FSEL[0]	TSEL[1]	TSEL[0]	0x02

TEST: Test bit, must be set to “0”

WADA: WeekAlarm/ DayAlarm control bit, decide 0x0A register as DAY Alarm or WEEK Alarm. 0-WEEK alarm, 1-DAY alarm

USEL: Update Interrupt Select bit, 0-output interrupt once a second, 1-output interrupt once a minute

TE: Timer Enable bit, 0-disenable, 1-enable

FSEL[1], FSEL[0]:FOUT frequency setting:

FSEL[1]	FSEL[0]	FOUT Frequency
0	0	32.768KHz(Default)
0	1	1024Hz
1	0	1Hz
1	1	32.768KHz

TSEL[1], TSEL[0]:Timer countdown period(source clock) setting:

TSEL[1]	TSEL[0]	Source clock
0	0	4096Hz
0	1	64Hz
1	0	1Hz
1	1	1/60Hz

6.2.5 Flag registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0E	Flag Register	○	○	UF	TF	AF	○	VLF	RSV	0x03

UF: Update flag bit. When time update interrupt event occurs, it will be set to “1”and keeps“1” until a “0” is written to it.

TF: Timer Flag bit. When a fixed-cycle timer interrupt event occurs, it will be set to “1” and keeps“1” until a

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"0" is written to it.

AF: Alarm Flag bit. When an alarm interrupt event occurs, it will be set to "1" and keeps"1" until a "0" is written to it.

VLF: Voltage Low Flag bit. When supply voltage is lower than 1.3V(Typ), it will be set to "1" and keeps "1" until a "0" is written to it.

6.2.6 Control registers 2

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0F	Control 2	CSEL [1]	CSEL [0]	UIE	TIE	AIE	○	○	RESET	0x40

CSEL[1], CSEL[0]: Compensation interval Select 1, 0 bits, used to set temperature compensation interval.

CSEL[1]	CSEL[0]	Compensation interval
0	0	0.5s
0	1	2s(default)
1	0	10s
1	1	30s

UIE: Update Interrupt Enable bit. When UF changes from "0" to "1", this bit controls if an interrupt signal is generated. 0-disenable(/INT keeps Hi-Z), 1-enable(/INT status changes from Hi-Z to Low).

TIE: Timer Interrupt Enable bit: When TF changes from "0" to "1", this bit controls if an interrupt signal is generated. 0-disenable(/INT keeps Hi-Z), 1-enable(/INT status changes from Hi-Z to Low).

AIE: Alarm Interrupt Enable bit: When AF changes from "0" to "1", this bit controls if an interrupt signal is generated. 0-disenable(/INT keeps Hi-Z), 1-enable(/INT status changes from Hi-Z to Low).

RESET: Reset divider, prepared for the synchronized starting of time or timer.

Reset	Value	
Write	0	Write 0 is invalid
	1	Write 1 reset 16384Hz~1Hz of 32.768KHz counter
Read	0	The read value of RESET is 0, always writes0, it is invalid.
	1	RESET bit clears automatically after Write access.

The detailed function of RESET.

For example.

S is start condition. P is stop condition.

Write access to RESET bit.

S—lave address—ACK1—0Fh—ACK2—01h—ACK3—P.

After P, RESET bit clears automatically.

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6.2.7 SOUT Control register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x19	SOUT config1	SOE[7]	SOE[6]	SOE[5]	SOE[4]	SOE[3]	SOE[2]	SOE[1]	SOE[0]	0x00
0x1A	SOUT config2	DCE	DC	○	○	SRV	FS[2]	FS[1]	FS[0]	0x00

By setting 0x19h = 0x69, SOUT function becomes activated. Other data disable SOUT function, then SOUT becomes Hi-Z.

In case of DCE = 1, DC bit value is outputted at SOUT.

In case of DCE = 0, register value Flag Value is outputted at SOUT. If SRV = 1 then SOUT output reverse.

Flag Value is decided by SRV, FS[2:0].

DCE	DC	FS[2]	FS[1]	FS[0]	Flag Value	SOUT Output	
						SRV = 0	SRV = 1
0	X	0	0	0	TF	TF	Inversion of TF
0	X	0	0	1	AF	AF	Inversion of AF
0	X	0	1	0	UF	UF	Inversion of UF
0	X	0	1	1	EF	EF	Inversion of EF
0	X	1	0	0	X	X	
0	X	1	0	1	VLF	VLF	Inversion of VLF
0	X	1	1	0	-	Low	
0	X	1	1	1	-	Low	
1	0	X	X	X	X	Low	
1	1	X	X	X	X	High	

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6.2.8 Time Stamp Data Event Controller register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x10	Time Stamp SEC	○	40	20	10	8	4	2	1	0x00
0x11	Time Stamp MIN	○	40	20	10	8	4	2	1	0x00
0x12	Time Stamp HOUR	○	○	20	10	8	4	2	1	0x00
0x13	Time Stamp WEEK	○	6	5	4	3	2	1	0	0x00
0x14	Time Stamp DAY	○	○	20	10	8	4	2	1	0x00
0x15	Time Stamp MONTH	TSVLF	RSV	○	10	8	4	2	1	0x00
0x16	Time Stamp YEAR	80	40	20	10	8	4	2	1	0x00
0x17	EVIN set	ECP	EHL	EPU	RCE	EIE	○	ET[1]	ET[0]	0x00
0x18	EVIN det	EF	○	○	○	EVMON	○	○	○	0x00

1) Time stamp SEC ~ YEAR

In case of trigger input detection from EVIN terminal, Clock and calendar data are recorded in Time stamp SEC ~ YEAR.

2) Time stamp VLF, Time stamp VDET

In case of trigger input detection from EVIN terminal, VLF bit is recorded to TSVLF.

3) ECP bit (Event capture Enable)

ECP enables Time Stamp function. Time Stamp function is enabled in case of ECP = 1.

4) EHL bit (EVIN pin, High/Low detection select)

Selection bit of EVIN Voltage level. In case of EHL = 0, EVIN pin detects active Low level; In case of EHL = 1, EVIN pin detects active High level.

5) EPU bit (Enable Pull-up register)

EPU enables Pull-up-resistor of EVIN input terminal. 0 – disabled; 1-enabled.

6) RCE bit (Repeat Capture Enable)

RCE enables repeated times stamp capture. 0 – disabled; 1-enabled.

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7) EF bit (Event trigger Flag)

History bit of EVIN trigger. 0 – There is no EVIN detection history; 1- There is EVIN detection history.

8) ET[1:0] bits (Event input debounce Time set)

Selection of debounce filtering cycle time.

ET[1]	ET[0]	Filtering Cycle Time
0	0	No filtered(default)
0	1	3.9ms
1	0	15.6ms
1	1	125ms

9) EIE bit (EVIN Interrupt Enable)

/INT Interrupt Enable/Disable selection bit. 0-disable;1-enable.

10) EVMON bit (EVIN Monitor)

EVMON can read the EVIN input level. 0-LOW; 1-HIGH.

6.2.9 ID Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x20	ID	Vendor ID[3:0]				Version[3:0]				0xD4

Vendor ID: Vendor Code, Vendor ID[3:0]=1101b=Dh, Dh instead of DAPU.
Version: Chip Version.

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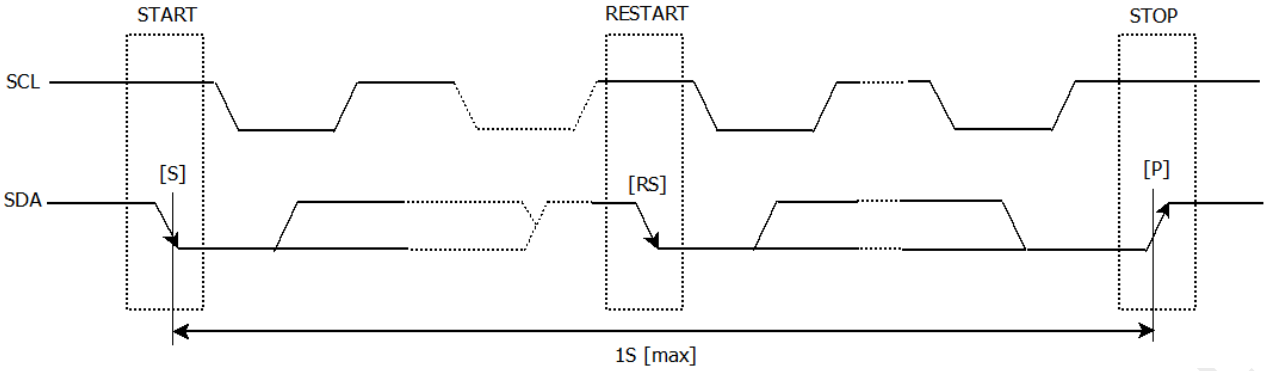
7 I²C Bus Interface



I²C bus supports bi-directional communications through a serial clock line SCL and a serial data line SDA. I²C bus device can be defined as “Master” and “Slave”. INS5A8804 can only be used as Slave.

7.1 Cautions

I²C bus includes START, RESTART, STOP conditions, the duration between START and STOP must be less than 1 second just in case the bus to be set to standby mode automatically. A new START condition must be transferred before restarting of any communications.

INS5A8804I²C bus interface supports single byte read/write operations as well as multiple bytes incremental access. After 0xFF address, the next one will be 0x00.

7.2 Slave Address

Table12. I²CBus Slave Address

Transfer data	Slave address							R/W
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
65h(Read)	0	1	1	0	0	1	0	1 (Read)
64h(Write)								0 (Write)

INS5A8804 I²C bus Slave Address is [0110 010*].

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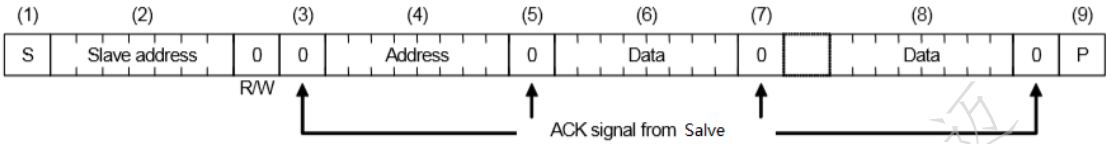
7.3 I²C bus protocol

It is assumed CPU is master and INS5A8804 is slave in this section.

7.3.1 Write process

I²C bus includes an address auto-increment function, once the initial address has been specified, the INS5A8804 increments (+1) the address automatically after each data is sent, then to write next data.

(1) CPU sends start condition[S]
(2) CPU sends INS5A8804's slave address with R/W bit to set to write mode
(3) CPU verifies ACK signal from INS5A8804
(4) CPU sends write address to INS5A8804
(5) CPU verifies ACK signal from INS5A8804
(6) CPU sends write data to the address specified at step (4)
(7) CPU verifies ACK signal from INS5A8804
(8) Repeat (6) (7) if multiple bytes need to be written, address will be incremented automatically
(9) CPU ends stop condition[P]



7.3.2 Read process

Writing the address to be read with write mode firstly, then reading the data with read mode.

(1) CPU sends start condition[S]
(2) CPU sends INS5A8804's slave address with R/W bit to set to write mode
(3) CPU verifies ACK signal from INS5A8804
(4) CPU sends address for reading from INS5A8804
(5) CPU verifies ACK signal from INS5A8804
(6) CPU sends RESTART condition [Sr]
(7) CPU sends INS5A8804's slave address with R/W bit to set to read mode
(8) CPU verifies ACK signal from INS5A8804
(9) CPU reads data from the specified address in step (4)
(10) CPU sends ACK signal for "0"
(11) Repeat (9) (10) if multiple bytes need to be read, address will be incremented automatically
(12) CPU sends ACK signal for "1"
(13) CPU sends stop condition[P]

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8 Reflow Soldering Curve

Standard: IPC/JEDEC J-STD-020

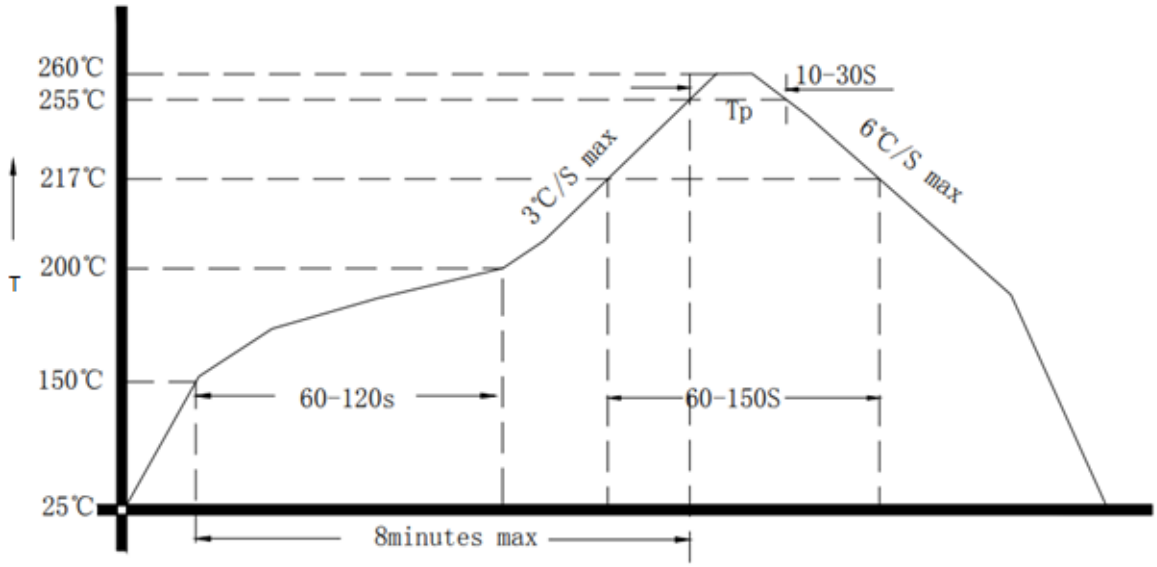

Figure 3. Reflow Soldering Curve

Note: It is suggested to solder IC under the condition shown in the curve above. Must pay attention to the temperature and time when manual soldering, if the temperature over +260℃, or you will make the xo performance bad, even damage it.

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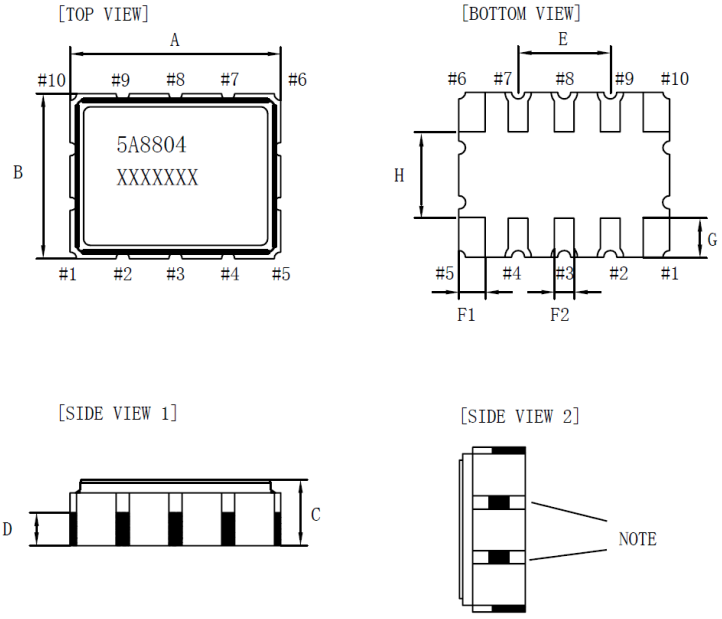
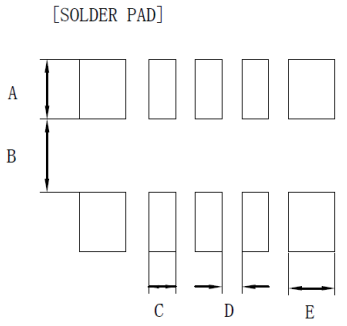
9 Dimensions



Dimension	Min.	Typ.	Max.
A	3.1	3.2	3.3
B	2.4	2.5	2.6
C	0.8	0.9	1.0
D	--	0.45	--
E	--	1.4	--
F1	--	0.4	--
F2	--	0.3	--
G	--	0.6	--
H	--	1.3	--

unit：mm



Dimension	Recommend
A	0.9
B	1.1
C	0.4
D	0.3
E	0.7

unit：mm

Note: The metal surface on the side shown in the figure is used for crystal test. Please avoid short circuit caused by contact between the metal surface and other electrical networks or other device surfaces during design and assembly.

Figure 4. Recommended Solder Pad and Dimensions

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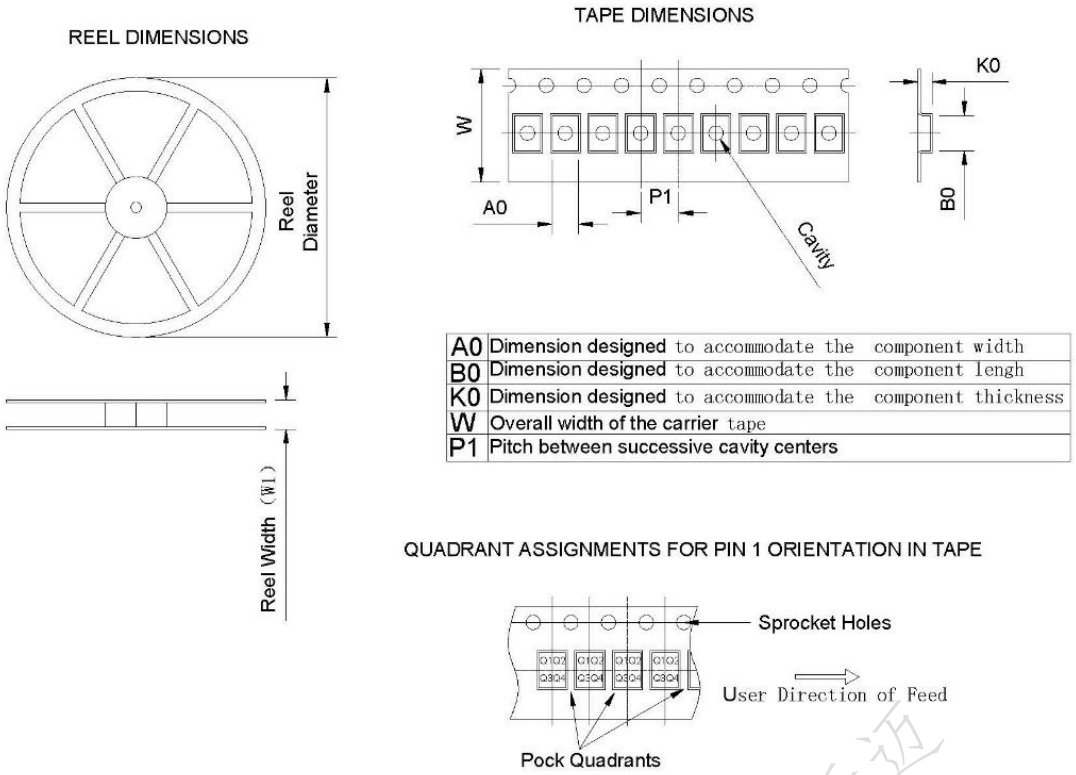
10 Package



Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	PIN1 Quadrant
INS5A8804	Ceramic	10	3000	180	11.6±2.0	3.00	3.70	1.50	4	8.00	Q1

Figure 5. Package

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11 Revision History

Version	Change Contents	Prepared by	RevisedDate
V1.0	First issued		2022.11.28
V2.0	1. Key Features： 1> Change Low current consumption from 1.5uA to 1.8uA. 2> Add “RoHS2.0 & REACH compliant”. 2. Chapter 4, Table1. Pin Definition: 1> FOE Description, add “build in pull down resistor(Typ:500KΩ)”. 2> SOUT Description, correct to “SOUT is the inside state output(CMOS output)”. 3> Delete T2 description, change to NC. 3. Chapter5.2 Table3 1> Change Current consumption typ value from 1.5uA to 1.8uA, add “VDD=3V” to Notes. 4. Chapter5.3 Table4 1> Add “VDD=3V” to oscillation start time notes. 2> Year aging: add min value -5ppm. 5. Chapter5.4 Table5 1> Correct IDD1/2/3/4 IDD1 typ value from 1.6 to 1.9uA. IDD1 max value from 50 to 26uA. IDD2 typ value from 1.5 to 1.8uA. IDD2 max value from 45 to 25uA. IDD3 typ value from 4.5 to 4.8uA. IDD3 max value from 50 to 30uA. IDD4 typ value from 2.5 to 2.8uA. IDD4 max value from 45 to 28uA.		2023.07.24

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	2> Add IDD5/6/7/8/9/10 description and value. 3> Add VLF description and value. 4> Modify High-level input voltage max value 5.5V to Vdd. 6. Chapter5.5 Table6: 1> Correct SCL/SDA tr/tf max value from 0.4us to 0.3us. 7. Chapter6 Registers 1> Delete 0x0E Bit0 "VDET" and description. 2> Delete 0x15 Bit6 "TSVDET" and description. 3> Table9 change to "ID Registers", delete RSV register and add 0x20 register description. 4> Note description Initial0: delete "TSVDET", "All bits of address 1Ch, 1Dh, 1Eh". 5> Note description Initial1: delete "VDET", add "All bits of address 1Ch, 1Dh, 1Eh". 6> Note description: delete "VDET" in "Only 0 can be written to UF, TF, AF, VLF, VDET bits". 7> Add description "Forbidden to modify the register except 6.1 register list and RSV register". 8> Correct an error in 6.2.3, modify the description from "REES" to "TRES". 9> Chapter 6.2.5, delete bit0 "VDET" and description, modify VLF value from "1.6V" to "1.3V(Typ)". 10> Chapter 6.2.6, modify RESET bit description from "RESET IC" to "RESET divider", and add more detail information for this bit. 11> Chapter 6.2.7, delete FS[2:0] config 100 SOUT Output VDET signal in the table. Modify FS[2:0] config 011 SOUT output from "LOW" to "EF". 12> Chapter 6.2.8, delete 0x15 bit6 "TSVDET" and item2 description "VDET bit to		

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	TSVDET". 13> ADD Chapter 6.2.9 ID Register description. 8. Chapter 7.1 1> Modify "0x7F address" to "0xFF address"		
V2.1	1. Chapter 6.2.7: Correct an error, modify "0x69 = 0x69" to "0x19 = 0x69"		2023.08.01

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