



To Customer: _____

Realtime Clock Module

INS5T8563

Datasheet

Document Version 1.0

Released on October 9th, 2023

Ordering Information

Manufacture Part Number	Product Name	Description
INS5T8563-7CEZ000N00MA	INS5T8563	-40°C~85°C, External 32K Crystal, SOP8
INS5T8563-7CEZ000N00LA	INS5T8563	-40°C~85°C, External 32K Crystal, TSSOP8

Guangdong Dapu Telecom Technology Co., Ltd

Bldg 5, SSL Modern Enterprise Accelerator Zone, Dongguan City, Guangdong Province, PRC China

[TEL:0086-0769-88010888](tel:0086-0769-88010888)

FAX:0086-0769-81800098



Revision History

Version	Change Contents	Prepared by	Revised Date
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1 Overview

INS5T8563 is an I²C bus interface real-time clock with low power consumption. It supports calendar (Century, year, month, day, hour, minute, second), timer and alarm function. The SOP8/TSSOP8 package makes it suitable to be used in portable electronic devices.

2 Block Diagram

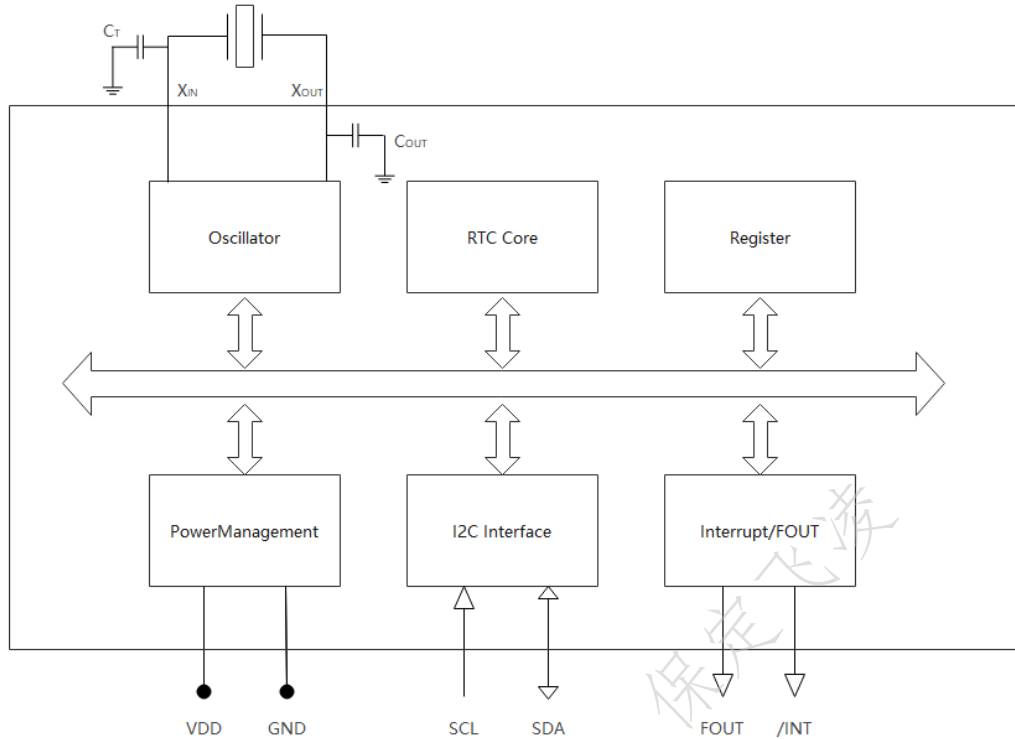


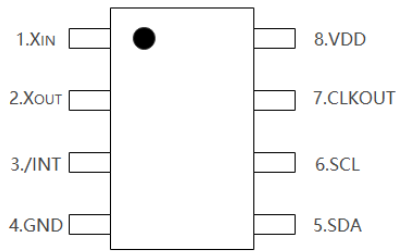
Figure 1. Block Diagram

3 Features

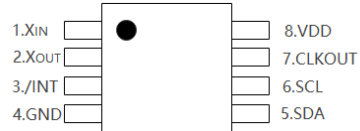
- Low Current Consumption: 0.9uA (Typ.)
- Communication Interface: I²C bus
- Alarm, Timer and Interruption
- Frequency Output
- External 32K crystal
- Integrated Oscillator Capacitors
- Power Supply Voltage: 1.2V ~ 5.5V
- Leap Years Autocorrection
- Operation Temperature Range: -40°C ~ +85°C
- Package: 4.9 * 6.0 * 1.6mm (SOP8)
- Package: 3.0 * 4.9 * 1.1mm (TSSOP8)



4 Pin Definition



SOP8 PIN CONFIG



TSSOP8 PIN CONFIG

Table1. Pin Definition

Pin Number	Pin Name	I/O	Description
1	X _{IN}		Oscillator Input, must connect an 8pf~25pf capacitor for trimming.
2	X _{OUT}		Oscillator Output.
3	/INT	Out	Alarm、 Timer Output. (Open-Drain).
4	GND	-	Ground
5	SDA	In/Out	I2C data signal
6	SCL	In	I2C clock signal
7	CLKOUT	Out	Frequency Output. (Open-Drain).
8	V _{DD}	-	Power in



5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table2. Absolute Maximum Ratings

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage	V _{DD}	-0.3		6.5	V	
I/O Input Voltage	V _{IN}	GND-0.3		6.5	V	SCL, SDA Input
Clock Output Voltage	V _{OUT}	GND-0.3		6.5	V	SDA, /INT Output, FOUT
Storage Temperature	T _{STG}	-55		125	°C	

5.2 Recommended Operating Conditions

Table3. Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage (normal mode)	V _{DD}	1.6	3.0	5.5	V	Note1,2,3
Power Supply Voltage (Time keeping)	V _{DD}	1.2	3.0	5.5	V	
Operation Temperature	T _{OPR}	-40	25	85	°C	

Note:

- 1: V_{DD} need to be supplied with more than 2.5V at least for the oscillator to work until stabilization.
- 2: A capacitor(8pf~25pf) need to be connected between X_{IN} and GND.
- 3: Ensure that the time of supply from 0 to V_{DD} is less than 100ms.

5.3 Oscillator Characteristics

Table4. Oscillator Characteristics

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Oscillator						
X _{out} Capacitor	C _{OUT}	15	25	35	pF	
External Crystal(32.768KHz)						
Series Resistance	R _S			100	kΩ	
Capacitor Trim	C _T	8		25	pF	
Load Capacitance	C _L	7		12.5	pF	$C_L = \frac{C_T * C_{OUT}}{C_T + C_{OUT}}$
FOUT Duty cycle	t _w /t	40	50	60	%	FOUT



5.4 DC Characteristics

Table5. DC Characteristics

Parameter	Symbol	Value			Unit	Notes	
		Min.	Typ.	Max.			
Average Current1	I _{DD1}		1.0	3.0	uA	V _{DD} =5.0V	f _{SCL} = 0 Hz, /INT = OFF, FOUT = OFF, SDA="L", SCL="L"
Average Current2	I _{DD2}		0.9	2.8		V _{DD} =3.0V	
Average Current3	I _{DD3}		1.9	3.8		V _{DD} =5.0V	FOUT = 32.768KHz (CL=15PF), /INT=OFF , SDA="L", SCL="L"
Average Current4	I _{DD4}		1.7	3.5		V _{DD} =3.0V	
Input High Voltage	V _{IH}	0.8*V _{DD}		5.5	V	SCL, SDA	
Input Low Voltage	V _{IL}	GND		0.2*V _{DD}	V		
Output Low Voltage	V _{OL1}	GND		GND+0.25	V	V _{DD} =5V, IOL=1mA	/INT
	V _{OL2}	GND		GND+0.4		V _{DD} =3V, IOL=1mA	
	V _{OL3}	GND		GND+0.5		V _{DD} =5V, IOL=1mA	FOUT
	V _{OL4}	GND		GND+0.3		V _{DD} =3V, IOL=0.5mA	
Input Leak Current	I _{LK}	-0.1		0.1	uA	SDA, SCL, V _{IN} = V _{DD} or GND	
Output Leak Current	I _{OZ}	-0.1		0.1	uA	SDA, V _{IN} = V _{DD} or GND	

5.5 AC Characteristics

Table6. AC Characteristics

V_{DD}=1.6V ~ 5.5V; Ta=-40°C ~ +85°C

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
SCL clock frequency	f _{SCL}			400	kHz
SCL Low Voltage Time	t _{LOW}	1.3			us
SCL How Voltage Time	t _{HIGH}	0.6			us
Start condition hold time	t _{HD} , STA	0.6			us
Start condition setup time	t _{SU} , STA	0.6			us
Stop condition setup time	t _{SU} , STO	0.6			us



Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Bus idle time between start condition and stop condition	t_{RCV}	1.3			us
Data setup time	$t_{SU, DAT}$	100			ns
Data hold time	$t_{HD, DAT}$	0			ns
SCL, SDA rising time	t_r			0.3	us
SCL, SDA falling time	t_f			0.3	us

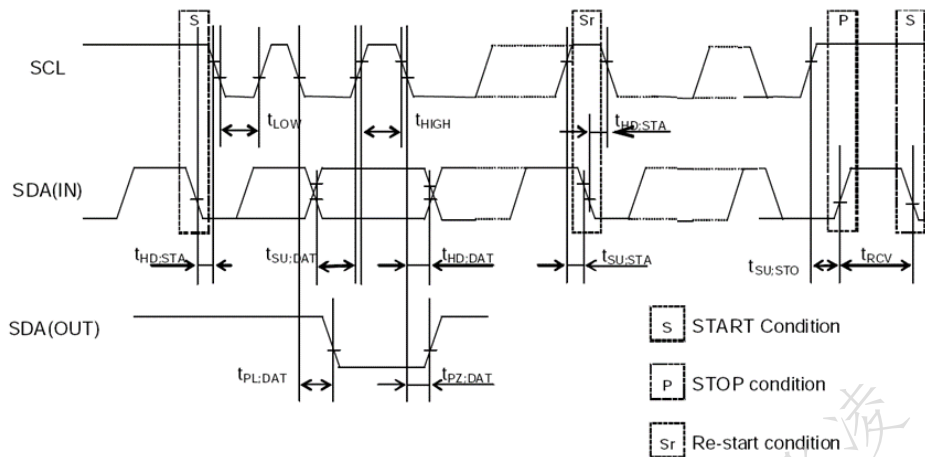


Figure 2. I²C bus Timing Chart

Note: When the master device gets access to this slave device through I2C, the whole operation duration should be less than 1s, otherwise it will be reset by the I2C bus through the internal bus overtime function.



6 Registers

6.1 Register Lists

Address 0x00~0x01: Control and Flag Registers Group

Address 0x02~0x08: Time Register Group

Address 0x09~0x0C: Alarm Register Group

Address 0x0D: CLKOUT Control Register

Address 0x0E~0x0F: Timer Register Group

Address 0x11: Offset Register

Table7. Basic Time and Calendar Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x00	Control Register_1	EXT_TEST	○	STOP	○	○	○	○	○	R/W
0x01	Control Register_2	○	○	○	TI_TP	AF	TF	AIE	TIE	R/W
0x02	SEC	VLF	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				R/W
0x03	MIN	○	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R/W
0x04	HOUR	○	○	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0x05	DAY	○	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x06	WEEK	○	○	○	○	○	BCD code, Week ones place, 0-6			R/W
0x07	MONTH	Century	○	○	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				R/W
0x08	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				R/W
0x09	MIN Alarm	AE	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R/W
0x0a	HOUR Alarm	AE	○	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0x0b	DAY Alarm	AE	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x0c	WEEK Alarm	AE	○	○	○	○	BCD code, Week ones place, 0-6			R/W
0x0d	CLKOUT_Control Register	FE	○	○	○	○	○	FD[1:0]		R/W
0x0e	Timer_Control Register	TE	○	○	○	○	○	TD[1:0]		R/W
0x0f	Timer Counter	128	64	32	16	8	4	2	1	R/W
0x11	Offset Control	MODE	OFFSET_CFG[6:0]							R/W



Note:

- 1, After power-up reset or in case VLF bit returns “1”, make sure to initialize all registers before using the RTC.
2. The default value of register after power on:
 - Initial 0: AF、TF、AIE、TIE、FD[1:0]、TD[1:0].
 - Initial 1: VLF、AE、FE、TE.
- 3.The bits marked with “○” can be read out “0” after initializing.
- 4.Only 0 can be written to TF、AF and VLF bits.

6.2 Details of Registers

6.2.1 Clock counter registers

Table8. Second、Minute and Hour Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x02	SEC	VLF	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				0x80
0x03	MIN	○	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x00
0x04	HOUR	○	○	BCD code, Hour tens place, 0-2		0x00			0x00	

SEC: BCD format, Value: 0~59

MIN: BCD format, Value: 0~59

HOUR: BCD format, Value: 0~23

VLF (Voltage Low Flag): Voltage Low Flag, when voltage is lower than 1.3V ,this bit will be set to”1”, and keep this value until written to “0” by software.

Table9. Day Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x05	DAY	○	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				0x01

DAY: BCD format, the value range will be adjusted automatically according to the month setting and if a leap year or not.

Table10. DAY Register Value Range

Month	Day Value Range
1, 3, 5, 7, 8, 10, 12	1~31
4, 6, 9, 11	1~30
February in normal year	1~28
February in leap year	1~29



Table11. Week Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x06	WEEK	○	○	○	○	○	BCD code, Week ones place, 0-6			0x00

Table12. WEEK Register Value table

	Bit2	Bit1	Bit0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

Table13. Month and Year Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x07	MONTH	Century	○	○	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				0x01
0x08	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				0x00

MONTH: BCD format, Value1~12

YEAR: BCD format, Value01~99(2001~2099)

Century: 0-Century is X, 1-Century is X+1

Example: 2023/01/01 Wednesday 21:18:36

Table14. Example of time setting

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x02	SEC	○	0	1	1	0	1	1	0
0x03	MIN	○	0	0	1	1	0	0	0
0x04	HOUR	○	○	1	0	0	0	0	1
0x05	WEEK	○	0	0	0	0	0	1	1
0x06	DAY	○	○	0	0	0	0	0	1
0x07	MONTH	○	○	○	0	0	0	0	1
0x08	YEAR	0	0	1	0	0	0	1	1

6.2.2 Alarm registers

Table15. Alarm Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x01	Control Register_2	○	○	○	TI_TP	AF	TF	AIE	TIE	0x00
0x09	MIN Alarm	AE	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x80
0x0a	HOUR Alarm	AE	○	BCD code, Hour tens		BCD code, Hour ones place, 0-9				0x80



Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
				place, 0-2						
0x0b	DAY Alarm	AE	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				0x80
0x0c	WEEK Alarm	AE	○	○	○	○	BCD code, Week ones place, 0-6			0x80

Alarm interruption can be generated with the setting of these registers and the cooperation of AIE and AF.

AE (Alarm Enable): Alarm Enable bit, 0-Enable; 1-Disable.

AF function refer to 0x01 register bit3.

AIE function refer to 0x01 register bit1.

6.2.3 Timer registers

Table16. Timer Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x01	Control Register_2	○	○	○	TI_TP	AF	TF	AIE	TIE	0x00
0x0e	Timer_Control Register	TE	○	○	○	○	○	TD[1]	TD[0]	0x80
0x0f	Timer Counter	128	64	32	16	8	4	2	1	0x00

Timer interruption can be generated with the setting of these registers and the cooperation of TE、TF 、TIE and TD[1:0].

TE function refer to 0x0e register bit7.

TF function refer to 0x01 register bit2.

TIE function refer to 0x01 register bit0.

TD[1:0] function refer to 0x0e register bit1 and bit0.

6.2.4 CLKOUT control registers

Table17. CLKOUT Control Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0D	CLKOUT_Control Register	FE	○	○	○	○	○	FD[1]	FD[0]	0x80

Used for the CLKOUT Frequency function.

FE (Fout Enable): 0- Disable CLKOUT Frequency function, 1-Enable CLKOUT Frequency function。

FD[1], FD[0] to config the output frequency. Shown as below table:

Table18. FD Table

FD [1]	FD [0]	CLKOUT Frequency
0	0	32768Hz Output
0	1	1024Hz output
1	0	32Hz output
1	1	1Hz Output



6.2.5 Timer control registers

Table19. Timer Control Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0E	Timer_Control Register	TE	○	○	○	○	○	TD[1]	TD[0]	0x80

Used for the specified functions, including Time Update Interruption.

TE (Timer Enable): 0- Disable Timer Interrupt function, 1-Enable Timer Interrupt function.

TD[1], TD[0]: Timer/Counter Clock configuration bits, just as below table:

Table20. TD Table

TD [1]	TD [0]	Timer/Counter Clock	Interruption duration
0	0	4096Hz (244.14us)	122uS
0	1	64Hz (15.625ms)	7.813mS
1	0	1Hz (Second)	7.813mS
1	1	1/60Hz (Min)	7.813mS

6.2.6 Control register

Table21. Control Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x00	Control Register_1	EXT_TEST	○	STOP	○	○	○	○	○	0x00
0x01	Control Register_2	○	○	○	TI_TP	AF	TF	AIE	TIE	0x00

EXT_TEST: 1:Test Mode, 0: Normal Mode.

STOP: 1: RTC Clock is Stop, 0: RTC Clock is normal.

AF (Alarm Flag): Alarm Flag, when Alarm Interruption generation, this bit will change from “0”to “1”,and keep this value until written to “0” by software;

TF (Timer Flag): Timer Flag, when timer interruption generates, this bit will change from “0”to “1”,and keep this value until written to “0” by software;

AIE (Alarm Interrupt Enable): When AF changes from“0”to“1”, this bit can control if the interruption generates or not. 0-Did not generate (/INT maintain high resistance), 1-generate the interruption (/INT changes from high resistance to low voltage)。

TIE (Timer Interrupt Enable): When TF changes from“0”to“1”, this bit can control if the interruption generates or not. 0-Did not generate (/INT maintain high resistance), 1-generate the interruption (/INT changes from high resistance to low voltage)。



6.2.7 Offset control register

Table22. Offset Control Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x11	Offset Control	MODE	OFFSET_CFG[6:0]							0x00

Mode: Offset mode bit. See below table

Offset_cfg [6:0]: For MODE = 0, each LSB introduces an offset of 4.069 ppm. For MODE = 1, each LSB introduces an offset of 4.34 ppm. The offset value is coded in two's complement giving a range of +63 LSB to -64 LSB. See below table.

Table23. Mode

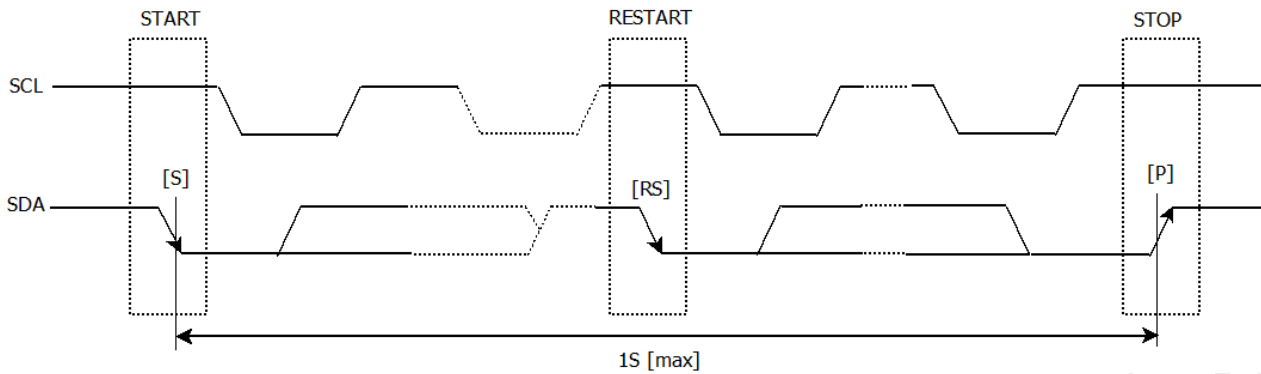
Symbol	Value	Description
Mode	0	Offset is made once every 4 minutes
	1	Offset is made once every 2 hours

Table24. Offset_Cfg

Offset_cfg[6:0]	Offset value in decimal	Offset value in ppm	
		Mode 0	Mode 1
011 1111	+63	+256.347	+273.42
011 1110	+62	+252.278	+269.080
.....
000 0010	+2	+8.138	+8.680
000 0001	+1	+4.069	+4.34
000 0000	0	0	0
111 1111	-1	-4.069	-4.34
111 1110	-2	-8.138	-8.680
.....
100 0001	-62	-252.278	-269.080
100 0000	-63	-256.347	-273.42



7 I²C Bus Interface



I²C bus supports bi-directional communications through a serial clock line SCL and a serial data line SDA. I²C bus device can be defined as “Master” and “Slave”. INS5T8563 can only be used as Slave.

7.1 Cautions

I²C bus includes START, RESTART, STOP conditions, the duration between START and STOP must be less than 1 second just in case the bus to be set to standby mode automatically. If the time is more than 1s, INS5T8563 will reset I²C Interface.

INS5T8563 I²C bus interface supports single byte read/write operations as well as multiple bytes incremental access. After 0xFF address, the next one will be 0x00.

7.2 Slave Address

Table25. I²C Bus Slave Address

Transfer data	Slave address							R/W
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A3h (Read)								1 (Read)
A2h (Write)	1	0	1	0	0	0	1	0 (Write)

INS5T8563 I²C bus Slave Address is [1010 001*].

7.3 I²C bus protocol

It is assumed CPU is master and INS5T8563 is slave in this section.

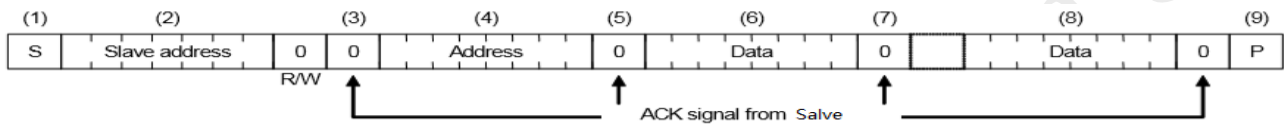
7.3.1 Write process

I²C bus includes an address auto-increment function, once the initial address has been specified, the INS5T8563 increments (+1) the address



automatically after each data is sent, then to write next data.

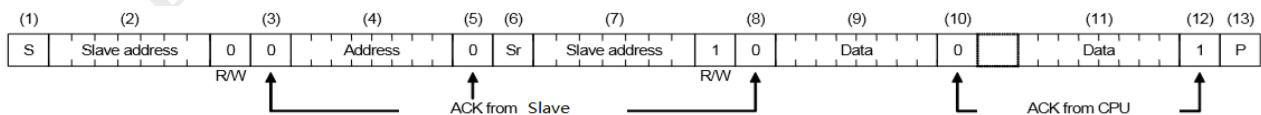
- (1) CPU sends start condition[S]
- (2) CPU sends INS5T8563's slave address with R/W bit to set to write mode
- (3) CPU verifies ACK signal from INS5T8563
- (4) CPU sends write address to INS5T8563
- (5) CPU verifies ACK signal from INS5T8563
- (6) CPU sends write data to the address specified at step (4)
- (7) CPU verifies ACK signal from INS5T8563
- (8) Repeat (6) (7) if multiple bytes need to be written, address will be incremented automatically
- (9) CPU ends stop condition[P]



7.3.2 Read process

Writing the address to be read with write mode firstly, then reading the data with read mode.

- (1) CPU sends start condition[S]
- (2) CPU sends INS5T8563's slave address with R/W bit to set to write mode
- (3) CPU verifies ACK signal from INS5T8563
- (4) CPU sends address for reading from INS5T8563
- (5) CPU verifies ACK signal from INS5T8563
- (6) CPU sends RESTART condition [Sr]
- (7) CPU sends INS5T8563's slave address with R/W bit to set to read mode
- (8) CPU verifies ACK signal from INS5T8563
- (9) CPU reads data from the specified address in step (4)
- (10) CPU sends ACK signal for "0"
- (11) Repeat (9) (10) if multiple bytes need to be read, address will be incremented automatically
- (12) CPU sends ACK signal for "1"
- (13) CPU sends stop condition[P]





8 Reflow Soldering Curve

Standard: IPC/JEDEC J-STD-020

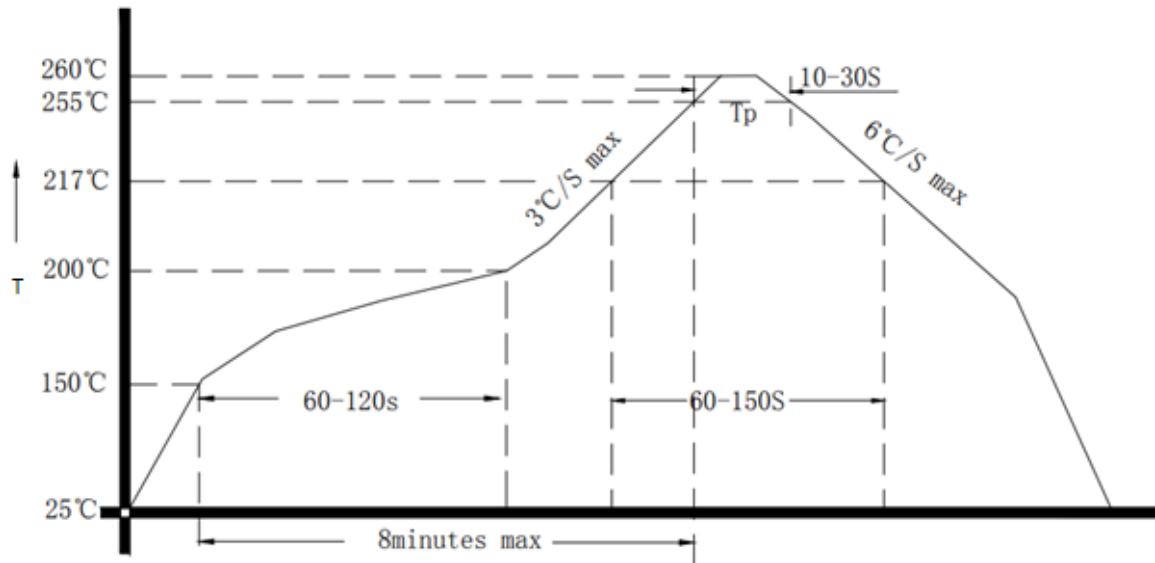
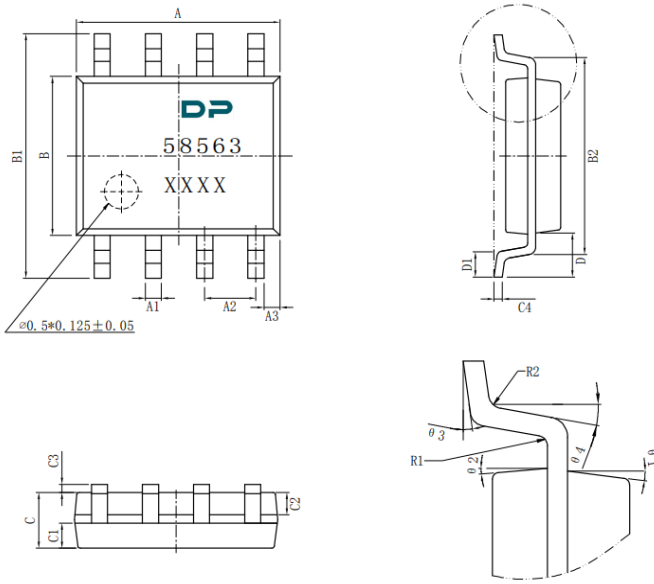


Figure 3. Reflow Soldering Curve

Note: It is suggested to solder IC under the condition shown in the curve above. Must pay attention to the temperature and time when manual soldering, if the temperature over +260°C, or you will make the xo performance bad, even damage it.

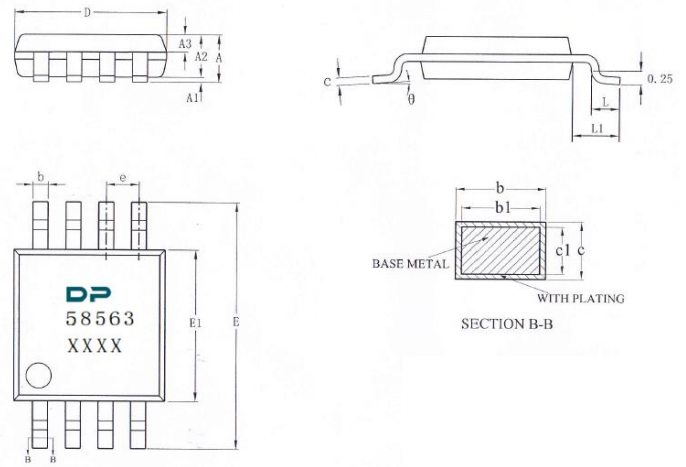


9 Dimensions and Marking



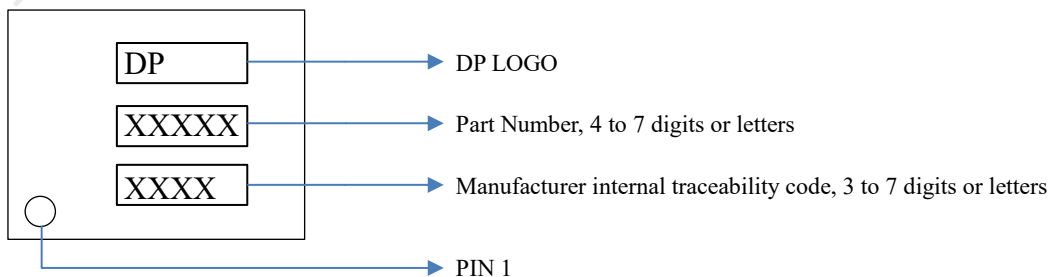
SOP8 Dimension and Mark

SOP8 Dimension/mm	Min.	Typ.	Max.
A	4.8	4.9	5.0
A1	0.356	--	0.456
A2	--	1.27	--
A3	--	0.345	--
B	3.8	3.9	4.0
B1	5.8	6.0	6.2
B2	--	5.00	--
C	1.3	--	1.6
C1	0.55	--	0.65
C2	0.55	--	0.65
C3	0.05	--	0.20
C4	0.203	--	0.233
D	--	1.05	--
D1	0.4	--	0.8
R1	--	0.2	--
R2	--	0.2	--
θ1		17°	
θ2		13°	
θ3		0°~8°	
θ4		4°~12°	



TSSOP8 Dimension and Mark

TSSOP8 Dimension/mm	Min.	Typ.	Max.
A	--	--	1.1
A1	0.05	--	0.15
A2	0.75	0.85	0.95
A3	0.3	0.35	0.4
b	0.28	--	0.36
b1	0.27	0.30	0.33
c	0.15	--	0.19
c1	0.14	0.15	0.16
D	2.9	3.0	3.1
E	4.7	4.9	5.1
E1	2.9	3.0	3.1
e		0.65BSC	
L	0.4	--	0.7
L1		0.95REF	
θ	0°	--	8°





10 Package Information

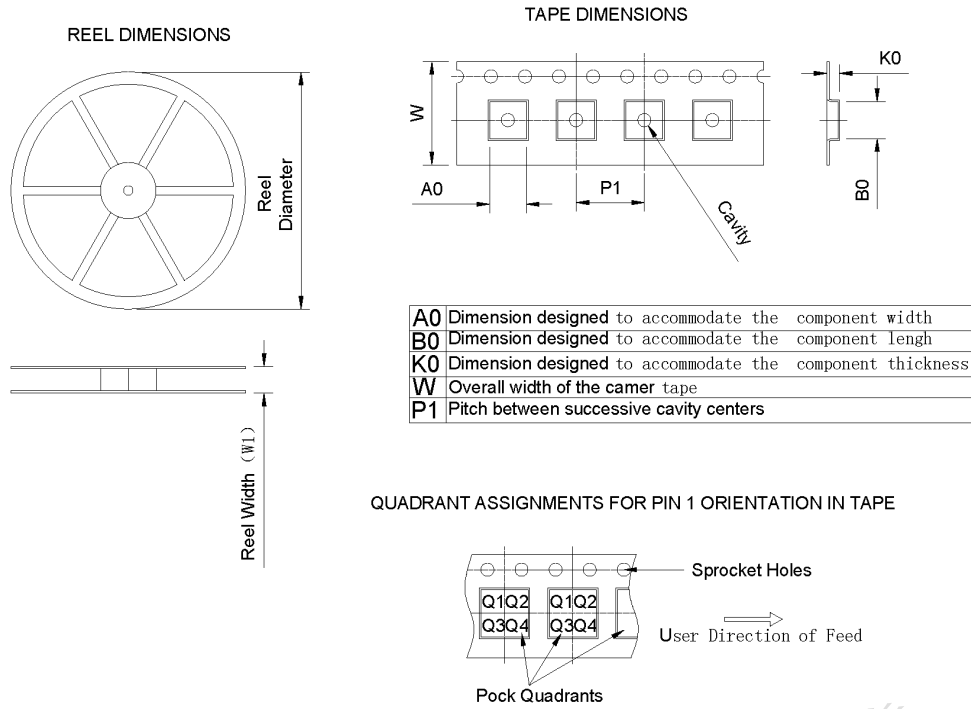


Figure 4. Package information

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	PIN1 Quadrant
INS5T8563-7CEZ000N00MA	SOP8	8	3000	330±1	12.4±0.2	6.40	5.30	2.10	8.00±0.1	12.00±0.1	Q1
INS5T8563-7CEZ000N00LA	TSSOP8	8	3000	330±1	12.4±0.2	5.3±0.1	3.3±0.1	1.25±0.1	8.00±0.1	12.00±0.1	Q1