

Customer Code: _____

DATASHEET

DAPU P/N: DSO312-32A-C13D-50M00000

DAPU			Customer Approval
Drew	Audited	Approved	
Jieshu ZHENG	Jianhua LIN	Gangtao FENG	
Date:	2024/11/6		

Stamp, please! Thanks!

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Table of amendment

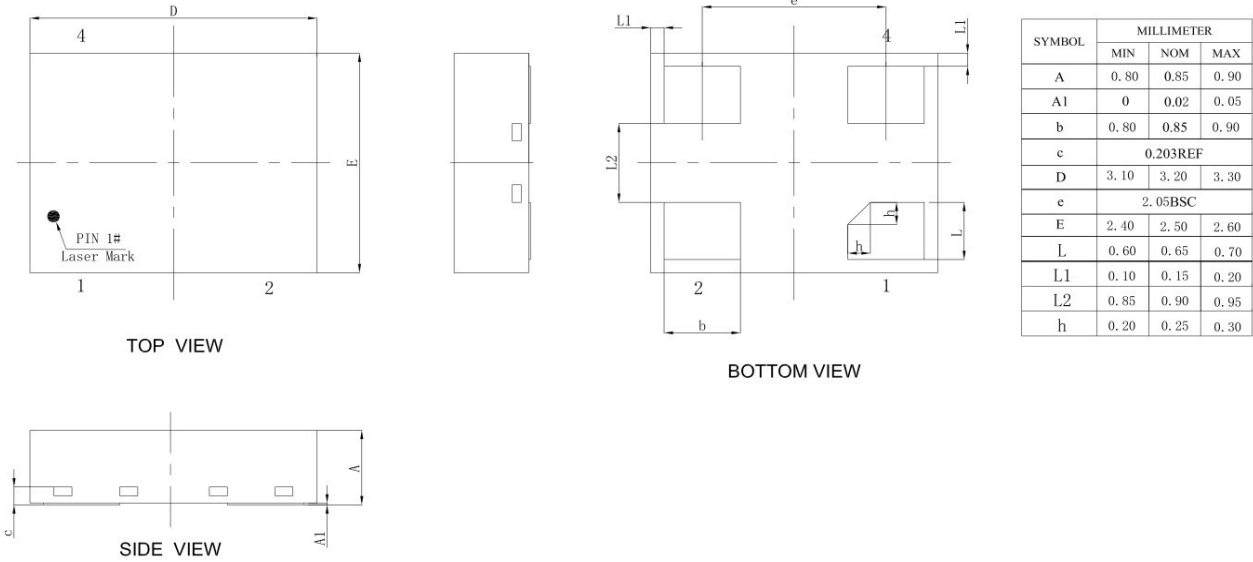
Version	Revision contents	Prepared by	Revised date
1.0	The first issued	Jieshu ZHENG	2024/11/6

1、Electrical Parameter

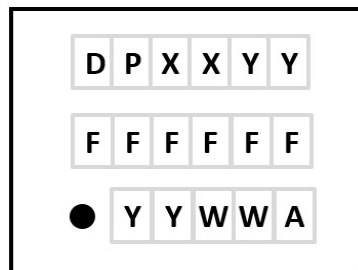
MODEL :		DSO312-32A-C13D-50M00000					
No.	Parameters	SYM.	Electrical Spec.				Notes
			Min.	Typ.	Max.	Units	
1	Nominal Frequency	F_L	50.0000			MHz	
2	Frequency Tolerance	F_T	-15		15	ppm	Inclusive of initial frequency tolerance at 25°C, 10-year aging at 25°C, and variations over supply voltage, load and humidity after soldering-reflow shift settles.
3	Frequency Stability	-	-35		35	ppm	-40°C~85°C (Reference 25°C)
4	Operating Temperature	T_{opr}	-40		85	°C	
5	Storage Temperature	T_{stg}	-55		105	°C	
6	Supply Voltage	V_{DD}	1.71		3.63	V	
7	Input Current	I_{cc}		40	55	mA	CMOS ($C_L=15$ pF)
8	Output Waveform	-	CMOS			-	
9	Output Load	C_L	15			pF	
10	Output Voltage High	V_{OH}	$0.83 \times V_{DD}$			V	$I_{OH} = 8/6/4$ mA for 3.3/2.5/1.8V V_{DD}
11	Output Voltage Low	V_{OL}			$0.17 \times V_{DD}$	V	$I_{OL} = 8/6/4$ mA for 3.3/2.5/1.8V V_{DD}
12	Rise Time	T_r		0.5	1.5	ns	20% to 80% V_{pp}
13	Fall Time	T_f		0.5	1.5	ns	
14	Input Voltage High	V_{IH}	$0.7 \times V_{DD}$			V	Frequency select (FS includes a 50 kΩ pull-up to V_{DD} and a 50 kΩ pull-down to GND.)
15	Input Voltage Low	V_{IL}			$0.3 \times V_{DD}$	V	
16	Duty Cycle	DC	45~55			%	
17	Powerup Time	T_{OSC}			4	ms	Time from $0.9 \times V_{DD}$ until output frequency (F_{CLK}) within spec
18	Phase Jitter (RMS)	Φ_J		350		fs	12kHz - 20MHz
19	Solder Temperature	T_{PEAK}	260			°C	The device is compliant with JEDEC J-STD-020.
	Solder Time at T_{PEAK}	T_P	20~40			sec	
20	Moisture Sensitivity Level 2						

2、 Mechanical Structure

2.1 Dimensions

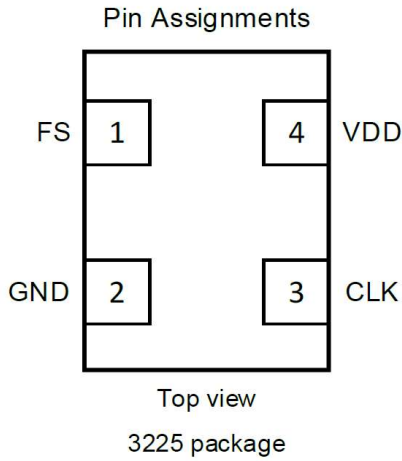


2.2 Marking



Line	Position	Description
1	Position 1-2	DP means Dapu
	Position 3-4	XX means out wave
	Position 5-6	YY means customer code
2	1-6	Frequency
3	Position 1	Pin 1 orientation mark (dot)
	Position 2-3	Year (last two digits of the year), to be assigned by assembly site
	Position 4-5	Calendar Work Week number, to be assigned by assembly site
	Position 6	A means Internal code

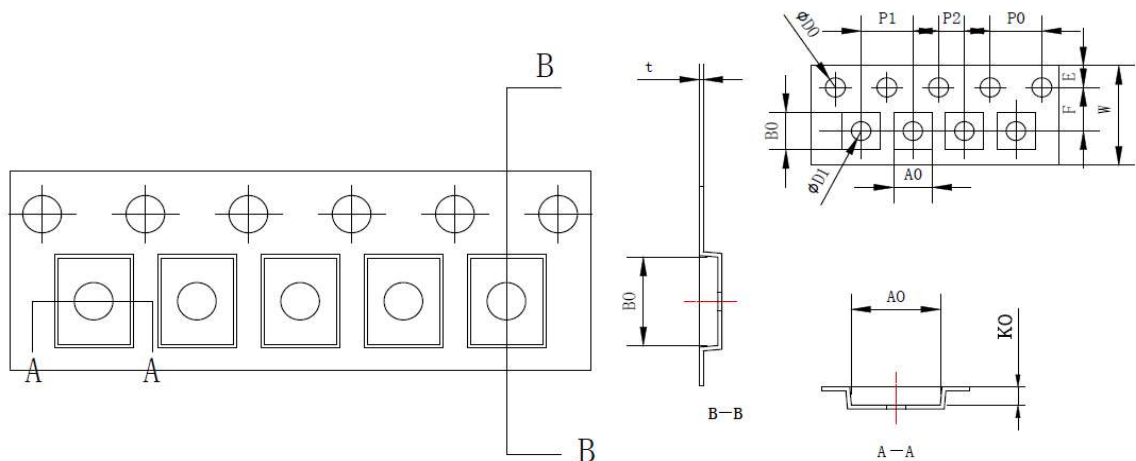
3、 Pin description



Pin#	Name	Description
1	FS	Configuration selector
2	GND	Ground
3	CLK	CMOS clock output
4	VDD	Power supply

FS	Description
Low	Driver stopped, output forced to high impedance
High	CLK output active, center spreading enabled: +/-0.5% Spread profile: Hershey-kiss Modulation frequency: 25 kHz

4、 Package: Tape & Reel (mm)



W	E	F	D0	D1	P0	P2	10P0	P1	A0	A1	B0	B1	KO	K1	t
8.00 ±0.30	1.75 ±0.10	3.50 ±0.05	1.50 +0.10	1.00 +0.10	4.00 ±0.10	2.00 ±0.10	40.00 ±0.20	4.00 ±0.10	2.80 ±0.10	/	3.60 ±0.10	/	1.10 ±0.10	/	0.30 ±0.05